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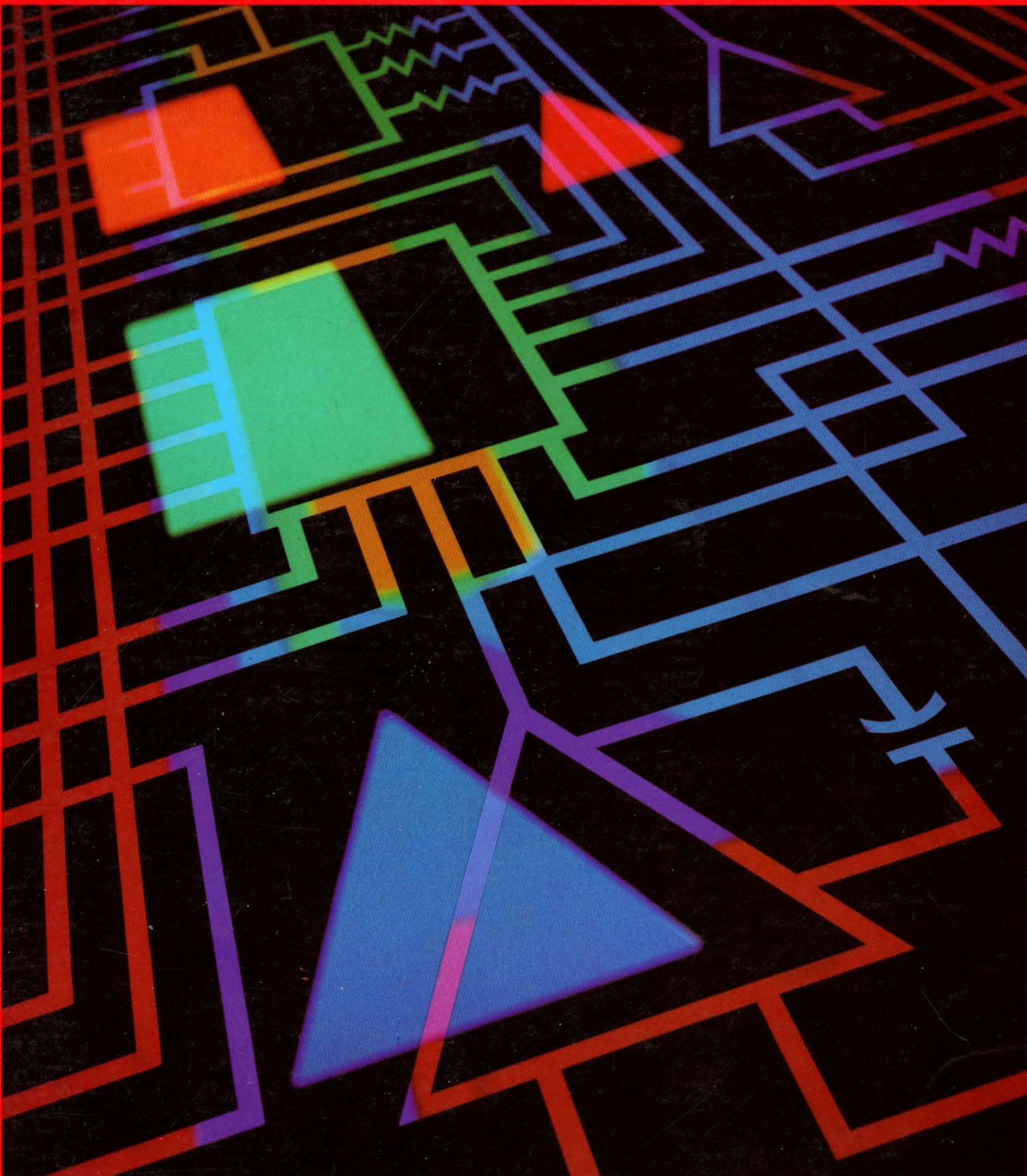
FAIRCHILD

A Schlumberger Company

Linear Data Book

1987

Linear Division



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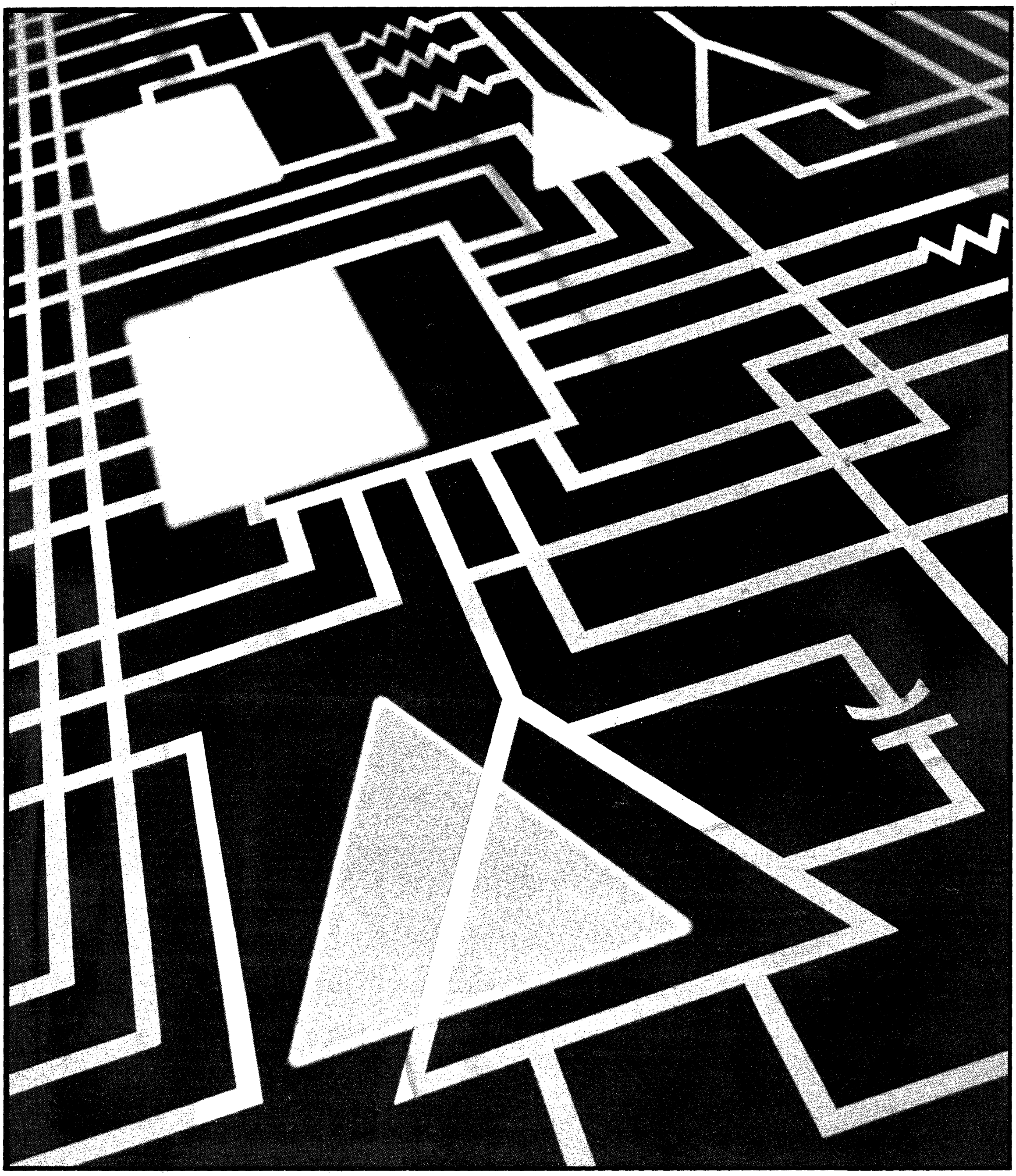

Linear Division
313 Fairchild Drive, Mountain View, CA 94043
(415) 962-4011 TWX MVLD

Introduction

The Linear Data Book includes the standard linear product line plus our new Winchester Disk Drive circuits and CLASIC™ standard cells. For ease of reference linear products are organized by sections. For example, Operational Amplifiers, Voltage Regulators and Special Functions, which includes Digital Signal Processing products such as the μA212 Single Chip Modem.

Technical information and basic product specifications, presented in data sheet form, include maximum ratings, electrical characteristics, performance curves, and packaging information. For many products, typical applications and test circuits are also included.

Package codes, included on each data sheet, indicate the specific package(s) offered for the product. Detailed packaging information, listed by package code, is included in a separate section. This section includes the new Surface Mount Devices (SMD), such as the Small Outline integrated Circuit (SOIC) packages.

A section on Aerospace and Defense precedes the Hi-Rel data sheets, which are organized in the same order as Standard Rel. These data sheets indicate the conformance to MIL-STD-883 and reference identical commercial data sheets for more complete information.

Section 1 has an alpha-numeric product listing of all Fairchild device numbers in the book. An explanation of the part numbering system appears in the "Ordering Information" portion of Section 1. In addition, there is an industry cross reference keying Fairchild Linear Products to direct replacement and function equivalents offered by major linear products manufacturers.

Other sections include information on Thermal Considerations and Quality. As added assistance, addresses and phone numbers of worldwide Field Sales Offices and Authorized Distributors have been listed.

Information on any commercial or Hi-Rel linear product may be obtained from a local sales office or by contacting:

Fairchild Linear Products
Marketing Department MS 4-370
313 Fairchild Drive
Mt. View, CA. 94039

The specifications included in this data book are as current and correct as could reasonably be determined at time of printing. Any errors noted by users, whether involving content or omissions can be directed to Linear Marketing at the above address.

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FAIRCHILD
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Industry Cross Reference Guide

Part Number	Fairchild Equivalent
AMD	
715DC	µA715DC
715HC	µA715HC
715DM	µA715DM
715HM	µA715HM
723DC	µA723DC
723DM	µA723DM
723HC	µA723HC
723HM	µA723HM
723PC	µA723PC
725HC	µA725HC
725HM	µA725HM
733DC	µA733DC
733DM	µA733DM
733HC	µA733HC
733HM	µA733HM
741FM	µA741FM
741HC	µA741HC
741HM	µA741HM
741AFM	µA741AFM
741AHM	µA741AHM
741EHC	µA741EHC
747DC	µA747DC
747DM	µA747DM
747HC	µA747HC
747HM	µA747HM
747PC	µA747PC
747ADM	µA747ADM
747AHM	µA747AHM
747EDC	µA747EDC
747EHC	µA747EHC
748HC	µA748HC
748HM	µA748HM
AM1408L6	DAC1408ADC
AM1408L7	DAC1408BDC
AM1408L8	DAC1408CDC
AM1508L8	DAC1508DM
AM26LS31DM	µA26LS31DM
AM26LS31PC	µA26LS31PC
AM26LS31DC	µA26LS31DC
AM26LS32DC	µA26LS32DC
AM26LS32PC	µA26LS32PC
AM6685DL	µA6685DV
AM6685DM	µA6685DM
AM6685HL	µA6685HV
AM6685HM	µA6685HM
AM6685LL	µA6685SV
AM6687DL	µA6687DV
AM6687DM	µA6687DM
AMD (Cont.)	
AM685DL	µA685DV
AM685DM	µA685DM
AM685HL	µA685HV
AM685HM	µA685HM
AM685LL	µA685SV
AM687DL	µA687DM
AM687DL	µA687DV
AM687DM	µA687DM
DAC-08CQ	DAC08CDC
DAC-08EQ	DAC08EDC
LM101H	µA101HM
LM101AH	µA101AHM
LM105H	µA105HM
LM108AH	µA108AHM
LM111H	µA111HM
LM124D	µA124DM
LM139D	µA139DM
LM201H	µA201HC
LM201AH	µA201AHV
LM208AH	µA208AHV
LM224D	µA224DV
LM301AH	µA301AHC
MC1488L	µA1488SC
MC1489L	µA1489SC
SN75107BJ	µA75107BDC
SN75107BN	µA75107BPC
SN75110J	µA75110DC
SN75110N	µA75110PC
SN75450BJ	µA75450BDC
SN75450BN	µA75450BPC
INTERSIL	
ICL108LNTY	µA108HM
ICL741CHSPA	µA741TC
ICL741MHSTY	µA741HM
LM101AH	µA101AHM
LM105H	µA105HM
LM108H	µA108HM
LM108AH	µA108AHM
LM111H	µA111HM
LM124J	µA124DM
LM301AH	µA301AHC
LM301AN	µA301ATC
LM305H	µA305HC
LM308H	µA308HC
LM308AH	µA308AHC
LM308AN	µA308ATC
NE555N	µA555TC
INTERSIL (Cont.)	
NE556N	µA556PC
µA723DC	µA723DC
µA723DM	µA723DM
µA723HC	µA723HC
µA723HM	µA723HM
µA723PC	µA723PC
µA733HC	µA733HC
µA733HM	µA733HM
µA741FM	µA741FM
µA741HC	µA741HC
µA741HM	µA741HM
µA741TC	µA741TC
µA748HC	µA748HC
µA748HM	µA748HM
µA748TC	µA748TC
MOTOROLA	
AM26LS31DC	µA26LS31DC
AM26LS31PC	µA26LS31PC
AM26LS32DC	µA26LS32DC
AM26LS32PC	µA26LS32PC
DAC08EP	DAC08EPC
DAC08PC	DAC08CPC
LM101AH	µA101AHM
LM105HM	µA105HM
LM108H	µA108HM
LM108AH	µA108AHM
LM111H	µA111HM
LM111J-8	µA111RM
LM117K	µA117KM
LM124J	µA124DM
LM139J	µA139DM
LM201AH	µA201AHV
LM208AH	µA208AHM
LM217K	µA217UV
LM224J	µA224DV
LM239J	µA239DC
LM301AH	µA301AHC
LM301AN	µA301ATC
LM308AH	µA308AHC
LM308AN	µA308ATC
LM311H	µA311HC
LM311J-8	µA311RC
LM311N	µA311TC
LM317K	µA317KC
LM317T	µA317UC
LM324J	µA324DC
LM339J	µA339DC

***Note**
Not exact package replacement

Part Number	Fairchild Equivalent	Part Number	Fairchild Equivalent	Part Number	Fairchild Equivalent
MOTOROLA (Cont.)		**MOTOROLA** (Cont.)		**MOTOROLA** (Cont.)	
LM348J	μA348DC	MC1711G	μA711HM	MC7805K	μA7805KM
LM348N	μA348PC	MC1711L	μA711DM	MC7805CK	μA7805KC
LM350K	μA350KC	MC1723CG	μA723HC	MC7805CT	μA7805UC
LM350T	μA350UC	MC1723CL	μA723DC	MC7812K	μA7812KM
LM710CH	μA710HC	MC1723CP	μA723PC	MC7812CK	μA7812KC
LM711CH	μA711HC	MC1723G	μA723HM	MC7812CT	μA7812UC
LM723CH	μA723HC	MC1723L	μA723DM	MC7815K	μA7815KM
LM723CJ	μA723DC	MC1733G	μA733HM	MC7815CK	μA7815KC
LM741CH	μA741HC	MC1733L	μA733DM	MC7815CT	μA7815UC
LM741CN	μA741TC	MC1733CG	μA733HC	MC7818K	μA7818KM
LM2901N	μA2901PC	MC1733CL	μA733DC	MC7818CK	μA7818KC
MC1408L7	DAC1408EDC	MC1741CG	μA741HC	MC7818CT	μA7818UC
MC1408L8	DAC1408ADC	MC1741CP1	μA741TC	MC7824K	μA7824KM
MC1408P6	DAC1408CPC	MC1741CU	μA741RC	MC7824CK	μA7824KC
MC1408P7	DAC1408BPC	MC1741G	μA741HM	MC7824CT	μA7824UC
MC1408P8	DAC1408APC	MC1747CG	μA747HC	MC78L05ACP	μA78L05AWC
MC1411P	μA9665PC	MC1747CL	μA747DC	MC78L12ACP	μA78L12AWC
MC1412P	μA9666PC	MC1747CP2	μA747PC	MC78L15ACP	μA78L15AWC
MC1413P	μA9667PC	MC1747G	μA747HM	MC78M05CG	μA78M05HC
MC1416P	μA9668PC	MC1747L	μA747DM	MC78M05CT	μA78M05UC
MC1455P1	μA555TC	MC1748CG	μA748HC	MC78M06CG	μA78M06HC
MC1458CG	μA1458CHC	MC1748CP1	μA748TC	MC78M06CT	μA78M06UC
MC1458CP1	μA1458CTC	MC1748G	μA748HM	MC78M08CG	μA78M08HC
MC1458CU	μA1458CRC	MC1776CG	μA776HC	MC78M08CT	μA78M08UC
MC1458G	μA1458HC	MC1776CP1	μA776TC	MC78M12CG	μA78M12HC
MC1458P1	μA1458TC	MC1776G	μA776HM	MC78M12CT	μA78M12UC
MC1458U	μA1458RC	MC3303P	μA3303PV	MC78M15CT	μA78M15UC
MC1488L	μA1488DC	MC3386P	μA3086PC	MC78M24CT	μA78M24UC
MC1488P	μA1488PC	MC3403L	μA3403DC	MC7905CK	μA7905KC
MC1489L	μA1489DC	MC3403P	μA3403PC	MC7905CT	μA7905UC
MC1489P	μA1489PC	MC3440AP	μA9640PC	MC7908CK	μA7908KC
MC1489AL	μA1489ADC	MC3443P	μA9640PC	MC7908CT	μA7908UC
MC1489AP	μA1489APC	MC3456P	μA556PC	MC7912CK	μA7912KC
MC1508L8	DAC1508DM	MC3458P1	μA798TC	MC7912CT	μA7912UC
MC1558G	μA1558HM	MC3486CL	μA3486DC	MC7915CK	μA7915KC
MC1558U	μA1558RM	MC3486CN	μA3486PC	MC7915CT	μA7915UC
MC1709AG	μA709AHM	MC3487CL	μA3487DC	NE592N	μA592PC
MC1709CP1	μA709TC	MC3487CN	μA3487PC	SE592F	μA592DM
MC1709CP2	μA709PC	MC3488AP	μA9636AT	SN75451BP	μA75451BTC
MC1709G	μA709HM	MC3558U	μA798TC	SN75452BP	μA75452BTC
MC1710CG	μA710HC	MC55107L	μA55107ADM	SN75453BP	μA75453BTC
MC1710CL	μA710DC	MC685B	μA685HM	TL431CLP	μA4131AWC
MC1710CP	μA710PC	MC75107L	μA75107ADC	TL494CJ	μA494DC
MC1710G	μA710HM	MC75107P	μA75107APC	TL494CN	μA494PC
MC1710L	μA710DM	MC75108CL	μA75108ADC	μA710HC	μA710HC
MC1711CG	μA711HC	MC75108CP	μA75108BPC	μA711HC	μA711HC
MC1711CL	μA711DC	MC75491P	μA75491PC	μA723DC	μA723DC
MC1711CP	μA711PC	MC75492P	μA75492PC	μA723HC	μA723HC

***Note**
Not exact package replacement

Industry Cross Reference Guide

Part Number	Fairchild Equivalent	Part Number	Fairchild Equivalent	Part Number	Fairchild Equivalent
MOTOROLA (Cont.)		**NATIONAL** (Cont.)		**NATIONAL** (Cont.)	
μA723PC	μA723PC	LM139J	μA139DM	LM710H	μA710HM
μA741HC	μA741HC	LM140K-5.0	μA7805KM	LM710CH	μA710HC
μA741TC	μA741TC	LM140K-12	μA7812KM	LM710CN	μA710PC
		LM140K-15	μA7815KM	LM711H	μA711HM
NATIONAL		LM201AH	μA201AHM	LM711CH	μA711HC
COP431I	μA431AWC	LM208H	μA208HM	LM711CN	μA711PC
CO494M	μA494DC	LM208AH	μA208AHM	LM723H	μA723HM
DS1488J	μA1488DC	LM2101AD/883	μA2101ADMQB	LM723J	μA723DM
DS1488N	μA1488PC	μA2108AD/833	μA2108ADMQB	LM723CH	μA723HC
DS1489AJ	μA1489ADC	μA2108D/883	μA2108DMQB	LM723CJ	μA723DC
DS1489AN	μA1489APC	LH2111D/883	μA2111DMQB	LM723CN	μA723PC
DS1489J	μA1489DC	LM224J	μA224DV	LM725H	μ725HM
DS1489N	μA1489PC	LM239J	μA239DC	LM725CH	μA725HC
DS26LS31C	μA26LS31PC	LM301AH	μA301AHC	LM725CN	μA725TC
DS26LS31M	μA26LS31DC	LM301AN	μA301ATC	LM733H	μA733HM
DS26LS32C	μA26LS32PC	LM305H	μA305HC	LM733CH	μA733HC
DS26LS32M	μA26LS32DC	LM305AH	μA305AHC	LM733CN	μA733PC
DS3486J	μA3486DC	LM308AN	μA308ATC	LM741H	μA741HM
DS3486N	μA3486PC	LM311J-8	μA311RC	LM741AH	μA741AHM
DS75107J	μA75107ADC	LM311N	μA311TC	LM741CH	μA741HC
DS75107N	μA75107APC	LM317K	μA317KC	LM741CJ	μA741RC
DS75108J	μA75108ADC	LM317T	μA317UC	LM741CN	μA741TC
DS75108N	μA75108APC	LM324J	μA324DC	LM747H	μA747HM
DS75150J-8	μA75150SC	LM324N	μA324PC	LM747J	μA747DM
DS75150N	μA75150PC	LM339J	μA339DC	LM747AH	μA747AHM
DS75154J	μA75154DC	LM339N	μA339PC	LM747AJ	μA747ADM
DS75154N	μA75154PC	LM340K-5.0	μA7805KC	LM747CH	μA747HC
DS75450J	μA75450DC	LM340T-5.0	μA7805UC	LM747CJ	μA747DC
DS75450N	μA75450PC	LM340K-6.0	μA7806KC	LM747CN	μA747PC
DS75491N	μA75491PC	LM340K-8.0	μA7808KC	LM747EH	μA747EHC
LF351A	μA771A	LM340K-12	μA7812KC	LM747EJ	μA747EDC
LF351B	μA771B	LM340T-12	μA7812UC	LM748H	μA748HM
LF351	μA771	LM340K-15	μA7815KC	LM748CJ	μA748RC
LF351N	μA771TC	LM340T-15	μA7815UC	LM748CH	μA748HC
LF353A	μA772A	LM340K-18	μA7818KC	LM748CN	μA748TC
LF353B	μA772B	LM340K-24	μA7824KC	LM760CH	μA760HC
LF353	μA772	LM348J	μA348DC	LM1458H	μA1458HC
LF353N	μA772TC	LM348N	μA348PC	LM1458J	μA1458RC
LF374B	μA774B	LM350K	μA350KC	LM1458N	μA1458TC
LF374	μA774	LM350I	μA350UC	LM1558H	μA1558HM
LM101AH	μA101AHM	LM555CN	μA555TC	LM1558J	μA1558RM
LM105H	μA105HM	LM556CN	μA556PC	LM2901N	μA2901PC
LM108AH	μA108AHM	LM592JD	μA592DM	LM2901J	μA2901DC
LM108H	μA108HM	LM592D	μA592D	LM3086N	μA3086PC
LM110H/883	μA110HMQB	LM709H	μA709HM	LM3302J	μA3302DC
LM111H	μA111HM	LM709CH	μA709HC	LM3302N	μA3302PC
LM117H/883	μA117HMQB	LM709CN	μA709PC	LM7805CK	μA7805KC
LM124J	μA124DM	LM709CN-8	μA709TC	LM7805CT	μA7805UC

***Note**
Not exact package replacement

Part Number	Fairchild Equivalent
NATIONAL (Cont.)	
LM7812CK	μA7812KC
LM7812CT	μA7812UC
LM7815CK	μA7815KC
LM7815CT	μA7815UC
LM78L05ACZ	μA78L05AWC
LM78L12ACZ	μA78L12AWC
LM78L15ACZ	μA78L15AWC
LM78M05CP	μA78M05UC
LM78M12CP	μA78M12UC
LM78M15CP	μA78M15UC
LM7905CK	μA7905KC
LM7905CT	μA7905UC
LM7912CK	μA7912KC
LM7912CT	μA7912UC
LM7915CK	μA7915KC
LM7915CT	μA7915UC
LM7905CH	μA79M05AHC
LM7912CH	μA79M12AHC
LM7915CH	μA79M15AHC
MC1508-8	DAC1508DM
PMI	
DAC-08C	DAC08CDC
DAC-08E	DAC08EDC
DAC1408A-6	DAC1408CPC
DAC1408A-7	DAC1408BPC
DAC1408A-8	DAC1408APC
DAC1508A-8	DAC1508DM
OP-07J	μA714HM
OP-07CJ	μA714HC
OP-07EJ	μA714EHC
PM108J	μA108HM
PM108AJ	μA108AHM
PM139AY	μA139ADM
PM139Y	μA139DM
PM208J	μA208HV
PM208AJ	μA208AHV
PM339Y	μA339DC
PM339AY	μA339ADC
PM725J	μA725HM
PM725CJ	μA725HC
PM725CP	μA725TC
PM741J	μA741HM
PM741CJ	μA741HC
PM741CZ	μA741RC
PM1458J	μA1458HC
PM1458Z	μA1458RC
PM1558J	μA1558HM
PMI (Cont.)	
PM1558Z	μA1558RM
PM4136Y	μA4136PC
PM4136CY	μA4136DC
SIGNETICS	
LM101AH	μA101AHM
LM111H	μA111HM
LM124F	μA124DM
LM139AF	μA139ADM
LM201AN	μA201AHM
LM224N	μA224PV
LM224F	μA224DV
LM301AN	μA301ATC
LM324N	μA324PC
LM324F	μA324DC
LM339N	μA339PC
LM339F	μA339DC
LM2901F	μA2901DC
LM2901N	μA2901PC
MC1458FE	μA1458RC
MC1458H	μA1458HC
MC1458N	μA1458TC
MC1488N	μA1488PC
MC1488F	μA1488DC
MC1489N	μA1489PC
MC1489F	μA1489DC
MC1489AN	μA1489APC
MC1489AF	μA1489ADC
MC1558H	μA1558HM
MC1558FE	μA1558RM
MC3302N	μA3302PC
MC3302F	μA3302DC
MC3403CF	μA3403DC
MC3403CN	μA3403PC
NE5501	μA9665PC
NE555D	μA555SC
NE555N	μA555TC
NE555N	μA555PC
NE556N	μA556PC
NE571F	μA571JJC
NE592D	μA592SC
NE592F	μA592DC
SE592F	μA592DM
NE592N	μA592PC
NE592N8	μA592TC
SE555FE	μA555RM
ULN2001N	μA9665PC
ULN2003F	μA9667DC
SIGNETICS (Cont.)	
ULN2003N	μA9667PC
ULN2004F	μA9668DC
ULN2004N	μA9668PC
μA723F	μA723DM
μA723H	μA723HM
μA723CD	μA723SC
μA723CF	μA723DC
μA723CH	μA723HC
μA723CN	μA723PC
μA733F	μA733DM
μA733H	μA733HM
μA733CF	μA733DC
μA733CH	μA733HC
μA733CN	μA733PC
μA741FE	μA741RM
μA741CFE	μA741RC
μA741CN	μA741TC
μA747F	μA747DM
μA747CF	μA747DC
μA747CN	μA747PC
SILICON GENERAL	
SG101A	μA101AHM
SG105T	μA105HM
SG111T	μA111HM
SG117K	μA117KM
SG124J	μA124DM
SG217P	μA217UV
SG224J	μA224DV
SG224N	μA224PV
SG301AM	μA301ATC
SG301AT	μA301AHC
SG305T	μA305HC
SG305AT	μA305AHC
SG311M	μA311TC
SG311T	μA311HC
SG317K	μA317KC
SG317P	μA317UC
SG324J	μA324DC
SG324N	μA324PC
SG555M	μA555TC
SG556N	μA556PC
SG710J	μA710DM
SG710T	μA710HM
SG710CN	μA710PC
SG710CT	μA710HC
SG711J	μA711DM

***Note**
Not exact package replacement

Industry Cross Reference Guide

Part Number	Fairchild Equivalent
SILICON GENERAL (Cont.)	
SG711T	μA711HM
SG711CJ	μA711DC
SG711CN	μA711PC
SG711CT	μA711HC
SG723CJ	μA723DC
SG723CT	μA723HC
SG723J	μA723DM
SG723T	μA723HM
SG723CN	μA723PC
SG733J	μA733DM
SG733T	μA733HM
SG733CJ	μA733DC
SG733CN	μA733PC
SG733CT	μA733HC
SG741F	μA741FM
SG741T	μA741HM
SG741CM	μA741TC
SG747J	μA747DM
SG747T	μA747HM
SG747CJ	μA747DC
SG747CN	μA747PC
SG747CT	μA747HC
SG748T	μA748HM
SG748CM	μA748TC
SG748CT	μA748HC
SG1488J	μA1488DC
SG1489AJ	μA1489ADC
SG1558T	μA1558HM
SG2001J	μA9665PC
SG2002J	μA9666DC
SG2003J	μA9667DC
SG3086J	μA3086DC
SG3086N	μA3086PC
SG3302J	μA3302DC
SG3302N	μA3302PC
SG75450BJ	μA75450BDC
SE75450BN	μA75450BPC
SG7805K	μA7805KM
SG7805CK	μA7805KC
SG7805CP	μA7805UC
SG7808K	μA7808KM
SG7808CK	μA7808KC
SG7808CP	μA7808UC
SG7812K	μA7812KM
SG7812CK	μA7812KC
SG7812CP	μA7812UC
SG7815K	μA7815KM

Part Number	Fairchild Equivalent
SILICON GENERAL (Cont.)	
SG7815CK	μA7815KC
SG7815CP	μA7815UC
SG7818K	μA7818KM
SG7818CK	μA7818KC
SG7818CP	μA7818UC
SG7824K	μA7824KM
SG7824CK	μA7824KC
SG7824CP	μA7824UC
SG7905K	μA7905KM
SG7905CK	μA7905KC
SG7905CP	μA7905UC
SG7908K	μA7908KM
SG7908CK	μA7908KC
SG7908CP	μA7908UC
SG7912K	μA7912KM
SG7912CK	μA7912KC
SG7912CP	μA7912UC
SG7915K	μA7915KM
SG7915CK	μA7915KC
SG7915CP	μA7915UC
SG75450BCN	μA75450BPC
SG75451BCM	μA75451BTC
SG75451BCY	μA75451BRC
SG75452BCM	μA75452BTC
SG75453BCM	μA75453BTC
SG75453BCY	μA75453BRC
SG75461CM	μA75461TC
SG75462CM	μA75462TC
SILICON SYSTEMS	
SSI117-2	μA2482RDC
SSI117-4	μA2484RDC
SSI117-6	μA2486RDC
TEXAS INSTRUMENTS	
AM26S10CJ	μA9640DC
AM26S10CN	μA9640PC
TC101AJ	μA101AHM
LM105L	μA105HM
LM124J	μA124DM
LM139J	μA139DM
LM148J	μA148DM
TC201AJG	μA201AHV
LM348J	μA348DC
LM348N	μA348PC
LM376P	μA376TC

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
MC1558JG	μA1558RM
NE555P	μA555TC
NE556N	μA556PC
RC4136D	μA4136SC
RC4136J	μA4136DC
RC4136N	μA4136PC
SA555D	μA555SC
SA555P	μA555TC
SE556N	μA556PC
SN55107AJ	μA55107ADM
SN55110AJ	μA55110ADM
SN75107AJ	μA75107ADC
SN75107AN	μA75107APC
SN75107BJ	μA75107BDC
SN75107BN	μA75107BPC
SN75108BN	μA75108BPC
SN75110AJ	μA75110ADC
SN75110AN	μA75110APC
SN75114J	μA9614DC
SN75114N	μA9614PC
SN75115J	μA9615DC
SN75115N	μA9615PC
SN75150N	μA75150PC
SN75150P	μA75150TC
SN75154J	μA75154DC
SN75154N	μA75154PC
SN75188J	μA1488DC
SN75188N	μA1488PC
SN75189J	μA1489DC
SN75189N	μA1489PC
SN75189AJ	μA1489ADC
SN75189AN	μA1489APC
SN75450BN	μA75450BPC
SN75451BJG	μA75451BRC
SN75451BP	μA75451BTC
SN75452BP	μA75452BTC
SN75453BJG	μA75453BRC
SN75453BP	μA75453BTC
SN75461P	μA75461TC
SN75462P	μA75462TC
SN75471P	μA75471TC
SN75472P	μA75472TC
SN75491N	μA75491PC
SN75492N	μA75492PC
TLC555MJG	μA555RM
TLC555CD	μA555SC
TLC555CP	μA555TC

***Note**
Not exact package replacement

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
TL071ACO	μA771BSC
TL071ACP	μA771BTC
TL071BCD	μA771ASC
TL071BCP	μA771ATC
TL071CD	μA771SC
TL071CP	μA771TC
TL071MJGB	μA771BRMQB
TL072ACD	μA772BSC
TL072ACP	μA772BTC
TL072BCD	μA772ASC
TL072BCP	μA772ATC
TL072CD	μA772SC
TL072CP	μA772TC
TL072MJGB	μA772BRMQB
TL074ACN	μA774BPC
TL074CN	μA774PC
TL074MJB	μA774BDMQB
TL081ACJG	μA771BRC
TL081ACP	μA771BTC
TL081BCJG	μA771ARC
TL081BCP	μA771ATC
TL081CJG	μA77LRC
TL081CP	μA77LTC
TL431CLP	μA431AWC
TL494CN	μA494PC
TL494CJ	μA494DC
TL494MJ	μA494DM
ULN2001AN	μA9665PC
ULN2002AJ	μA9666DC
ULN2002AN	μA9666PC
ULN2003AJ	μA9667DC

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
ULN2003AN	μA9667PC
ULN2004AJ	μA9668DC
ULN2004AN	μA9668PC
μA709MJ	μA709DM
μA709MU	μA709FM
μA709AMJ	μA709ADM
μA709AMU	μA709AFM
μA709CP	μA709TC
μA710CJ	μA710DC
μA710CN	μA710PC
μA710MJ	μA710DM
μA711CJ	μA711PC
μA711CN	μA711PC
μA711MJ	μA711DM
μA711MV	μA711FM
μA723CJ	μA723DC
μA723CN	μA723PC
μA723MJ	μA723DM
μA733CJ	μA733DC
μA733CN	μA733PC
μA733MJ	μA733DM
μA741CJG	μA741RC
μA741CD	μA741SC
μA741CP	μA741TC
μA741MJ	μA741DM
μA741MJG	μA741RM
μA741MU	μA741FM
μA747C	μA747DC
μA747CN	μA747PC
μA747MJ	μA747DM
μA748CP	μA748TC

Part Number	Fairchild Equivalent
TEXAS INSTRUMENTS (Cont.)	
μA2240CJ	μA2240DC
μA2240CN	μA2240PC
μA7805CKC	μA7805UC
μA7808CKC	μA7808UC
μA7812CKC	μA7812UC
μA7815CKC	μA7815UC
μA7818CKC	μA7818UC
μA7824CKC	μA7824UC
μA7885CKC	μA7885UC
μA78L05CLP	μA78L05AWC
μA78L12CLP	μA78L12AWC
μA78L15CLP	μA78L15AWC
μA78M05CKC	μA78M05UC
μA78M06CKC	μA78M06UC
μA78M08CKC	μA78M08UC
μA78M12CKC	μA78M12UC
μA78M15CKC	μA78M15UC
μA78M24CKC	μA78M24UC
μA7905CKC	μA7905UC
μA7908CKC	μA7908UC
μA7912CKC	μA7912UC
μA7915CKC	μA7915UC
μA79M05CKC	μA79M05AUC
μA79M08CKC	μA79M08AUC
μA79M12CKC	μA79M12AUC
μA79M15CKC	μA79M15AUC
μA9637AC	μA9637RC
9614CJ	μA9614DC
9614CN	μA9614PC
9615CJ	μA9615DC
9615CN	μA9615PC

***Note**
Not exact package replacement

Ordering Information

Standard Rel. and Hi-Rel. Ordering Code

Three basic units of information are contained in the ordering code.

μA741	T	C
Device Type	PackageType	Temperature Range

Device Type

This group of alpha numeric characters defines the device including functional and electrical characteristics, alpha suffixes are added to further delineate electrical options.

Package Type

One alpha suffix represents the basic package style.

D = Dual In-Line (Hermetic, Ceramic)
F = Flatpak (Hermetic)
G = Flatpak (Brazed)
H = Metal package
J = Dual In-Line (Side Brazed)
K = Metal Power Package (TO-3)
L = LCC Leadless Ceramic Chip Carrier
P = Dual In-Line (Molded)
Q = PLCC Plastic Leaded Chip Carrier
R = 8 Lead Dual In-Line (Hermetic, Ceramic)
S = SOIC Small Outline Integrated Circuits
T = 8 Lead Dual In-Line (Molded)
U = Power Package (Molded, TO-220)
W = Molded Package (TO-92 Outline)

Different outlines exist within each package style to accommodate various die sizes and number of leads. Specific dimensions for each package can be found in the Package Outline section of this catalog, listed by online code. These specific codes are referenced on each data sheet.

Temperature Range

One alpha suffix represents one of the following three basic temperature grades in common use. Exact values and conditions are specified on the device data sheets.

C = Commercial	0°C to +70°C
M = Extended	−55°C to +125°C
V = Industrial	−25°C to +85°C
	−40°C to +85°C

QB/883 Processing

A two alpha suffix of QB indicates conformance to Class "B" process requirements of MIL-STD-883 to Fairchild MIL temperature range data sheet electricals.

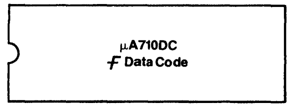
Examples

μA741FM This number code indicates a μA741 Operational Amplifier in a flatpak with military temperature rating capability.

μA725EHC This number code indicates a μA725 Instrumentation Operational Amplifier, electrical option E, in a metal package with a commercial temperature rating capability.

Device Identification

All Fairchild standard catalog linear circuits will be marked as shown in the following example.



JAN Part Ordering Code*

J M 38510/ 101 01 B G C

JAN Designator (J)
Cannot be marketed with "J" unless qualified on Part I or Part II of the QPL

General Procurement Spec (M 38510/)

Refers to Detail Spec (101)
101 Op Amps
102 Voltage Regulators
103 Comparators
104 Interface
106 Voltage Followers
107 Positive Fixed Voltage Regulators
108 Transistor Arrays
109 Timers
110 Quad Op Amps
112 Voltage Comparator
113 D to A Converter
115 Negative Fixed Voltage Regulators
117 Positive Adjustable Voltage Regulators
118 Negative Adjustable Voltage Regulators
119 Low Power, Low Noise, Bi-Fet Op Amps

Defines Device Type (01)

Processing Level (B)
S
B

Package Type (G)
A 14-lead 1/4 x 1/4 Flatpak
B 14-lead 1/4 x Flatpak
C 14-lead 1/4 x 3/4 Dip
D 14-lead 1/4 x 3/8 Flatpak
E 16-lead 1/4 x 7/8 Dip
F 16-lead 1/4 x 3/8 Flatpak
G 8-lead Can
H 10-lead 1/4 x 1/4 Flatpak
I 10-lead Can
J 24-lead 1/2 x 1 1/4 Dip
K 24-lead 3/8 x 5/8 Flatpak
L 24-lead 3/8 x 1/2 Flatpak
X 3-lead TO-5 Can
Y 2-lead TO-3 Can
Z 24-lead 1/4 x 3/8 Flatpak
Z 20 Terminal LCC

Lead Finish (C)
A Hot Solder Dip
B Tin Plate
C Gold Plate
X Any Finish Above

*See Section 12 Aerospace & Defense

Thermal Considerations

Thermal Management

An effective and safe performance of various IC or transistor packages is attained by proper heat removal and maintenance of their junction temperatures below the specified maximum values. In order to achieve efficient thermal management, the user must rely upon important parameters, provided by the manufacturer (junction-to-ambient and junction-to-case thermal resistances and maximum operating junction temperature).

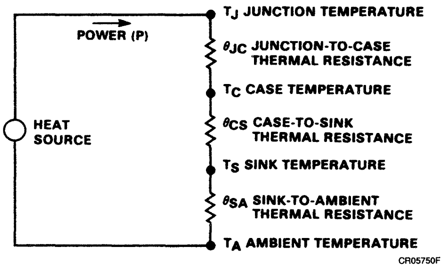
Thermal resistance is considered as the temperature gradient between two reference points in the package or the total system, per unit of power dissipation through the device encapsulated in the package, under steady state conditions. It is expressed as θ_{XY}, in degrees centigrade per Watt (°C/W) — where X and Y are the two reference points.

Equations

A simple thermal circuit for a semiconductor device in equilibrium is *shown in Figure 1*. The reference points in this case are

J — Device junction
C — Package case
S — Heat sink
A — Ambient

Figure 1 Simplified Thermal Circuit



The power dissipation, which is analogous to current flow in electrical terms, is caused by a heat source similar to a voltage source. Temperature is analogous to voltage potential and thermal resistance to ohmic resistance. The junction-to-ambient thermal resistance, θ_{JA}, is then expressed as a sum of thermal resistances in series, as shown:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$$= \frac{T_J - T_C}{P_D} + \frac{T_C - T_S}{P_D} + \frac{T_S - T_A}{P_D}$$

$$= \frac{T_J - T_A}{P_D} \ (°C/W)$$

Where
P_D = Power dissipation

Measurements

Substrate or isolation diode method is used to determine the device junction temperature, T_J. The other reference temperatures are measured using thermocouples attached to required points. There are standard procedures available for θ_{JA} and θ_{JC} measurements, details of which could be referred from MIL-STD-883 Method 1012, SEMI-STD Document #1341 and 1342.

The package thermal characterization is best performed using 'Test Chips'. The chip specification conforms to SEMI-STD NO. G 32-86. These chips consist of transistors or resistor strips (as the heat source) covering 85 percent of the active device area. Temperature sensing diodes and associated metallization runs are electrically isolated from the heat source. Such a test chip is considered a basic cell. Heat dissipating through a large size chip could be simulated by using an array of such basic cells. The device, and thus the package, is heated while being powered. The diode forward voltage (V_F) is simultaneously monitored using an independent low current source. T_J is determined from a V_F vs T_J calibration curve. This very reliable thermal resistance data could be correlated with the die size (= heat dissipating area).

The thermal resistance measurement of specific device plus package combination differs from the above described test chip method. In this case, a substrate diode is selected for determining T_J. Special electrical equipment is required for pulsing power in the forward direction of the device under test while measuring voltage drop across the substrate diode in between the pulses. This measurement technique has its shortcomings, since it is more prone to experimental errors.

In order to maintain the junction temperature below a specific level, at times it is necessary to use an external heat sink. The following is devoted to selection of proper heat sinks, with special relevance to voltage regulators.

Thermal Considerations Using Voltage Regulators as an Example

Heat Sink Requirements

When is a heat sink necessary, and what type of a heat sink should one use? The answers to these questions depend on reliability and cost requirements. Heat sinking is necessary to keep the operating junction temperature (T_J) of the regulator below the specified maximum value. Since semiconductor reliability improves as operating junction temperature is lowered, a reliability/cost compromise is usually made in the device design.

Thermal characteristics of voltage regulator chips and packages determine that some form of heat sinking is mandatory whenever the power dissipation exceeds the following.

0.67 W for the TO-39 package
0.69 W for the TO-92 package
1.56 W for the Mini Batwing and Power Watt (similar to TO-202) packages
1.8 W for the TO-220 package
2.8 W for the TO-3 package

at 25°C ambient or lower power levels at ambients above 25°C.

To choose or design a heat sink, the designer must determine the following regulator parameters.

$P_{D\ Max}$ — Maximum power dissipation: $(V_I - V_O)\ I_O + V_I\ I_Q$
T_A — Ambient temperature the regulator will encounter during operation.
$T_{J\ Max}$ — Maximum operating junction temperature, specified by the manufacturer.
θ_{JC}, θ_{JA} — Junction-to-case and junction-to-ambient thermal resistance values, also specified by the regulator manufacturer.
θ_{CS} — Case-to-heat sink thermal resistance which, for large packages, can range from about 0.2°C/W to about 1°C/W depending on the quality of the contact between the package and the heat sink.
θ_{SA} — Heat sink-to-ambient thermal resistance, specified by heat sink manufacturer.

Maximum permissible dissipation without a heat sink is determined by

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JA}}$$

If the device dissipation P_D exceeds this figure, a heat sink is necessary. The total required thermal resistance may then be calculated.

$$\theta_{JA(tot)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_{J\ Max} - T_A}{P_D}$$

Case-to-sink and sink-to-ambient thermal resistance information on commercially available heat sinks is normally provided by the heat sink manufacturer. A summary of some commercially available heat sinks is shown in *Table 1*. However, if a chassis or other conventional surface is used as a heat sink, *Figure 2* can be used as a guide to estimate the required surface area.

How to Choose a Heat Sink — Example

Determine the heat sink required for a regulator which has the following system requirements:

Operating ambient temperature range: 0°C to 60°C
Maximum junction temperature: 125°C
Maximum output current: 800 mA
Maximum input to output differential: 10 V

The TO-220 package is sufficient (lower cost, better thermal resistance).

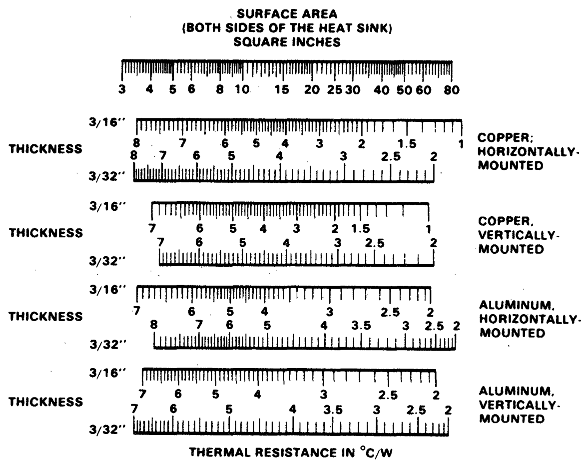
$$\theta_{JC} = 5°C/W \text{ maximum (from data sheet)}$$

$$\theta_{JA(tot)} = \theta_{JC} + \theta_{CS} + \theta_{SA} = \frac{T_J - T_A}{PD}$$

$$\theta_{CS} + \theta_{SA} = \frac{125 - 60}{0.8 \times 10} - 5 = 3.13°C/W$$

Assuming $\theta_{CS} = 0.13°C/W$ then $\theta_{SA} = 3°C/W$

Figure 2 Heat Sink Material Selection Guide



To determine either area required or thermal resistance of a given area, draw a vertical line between the top (or area) line down to the material of interest.

This thermal resistance value can be achieved by using either 22 square inches of 3/16 inch thick vertically mounted aluminum (*Figure 2*) or a commercial heat sink (*Table 1*).

Tips for Better Regulator Heat Sinking
Avoid placing heat-dissipating components such as power resistors next to regulators.

When using low dissipation packages such as TO-5, TO-39, and TO-92, keep lead lengths to a minimum and use the largest possible area of the printed board traces or mounting hardware to provide a heat dissipation path for the regulator.

When using larger packages, be sure the heat sink surface is flat and free from ridges or high spots. Check the regulator package for burrs or peened-over corners. Regardless of the smoothness and flatness of the package and heat sink contact, air pockets between them are unavoidable unless a lubricant is used. Therefore, for good thermal conduction, use a thin layer of thermal lubricant such as Dow Corning DC-340, General Electric 662 or Thermacote by Thermalloy.

In some applications, especially with negative regulators, it is desirable to electrically insulate the regulator case from the heat sink. Hardware kits for this purpose are commercially available for such packages as the TO-3 and TO-220. They generally consist of a 0.003 to 0.005 inch thick piece of mica or bonded fiberglass to electrically isolate the two surfaces, yet provide a thermal path between them. As expected, the thermal resistance will increase but, as in the direct metal-to-metal joint, some improvement can be realized by using thermal lubricant on each side of the mica.

If the regulator is mounted on a heat sink with fins, the most efficient heat transfer takes place when the fin is in a vertical plane, as this type of mounting forces the heat transfer from fin to air in a combination of radiation and convection.

If it is necessary to bend any of the regulator leads, handle them carefully to avoid straining the package. Furthermore, lead bending should be restricted since repeated bending will fatigue and eventually break the leads.

Table 1 Heat Sink Selection Guide

This list is only representative. No attempt has been made to provide a complete list of all heat sink manufacturers. All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

θ_{SA} Approx. (°C/W)	Manufacturer[3] and Type
TO-3 Packages	
0.4 (9" length)	Thermalloy (Extruded) 6590 Series
0.4 – 0.5 (6" length)	Thermalloy (Extruded) 6660, 6560 Series
0.56 – 3.0	Wakefield 400 Series
0.6 (7.5" length)	Thermalloy (Extruded) 6470 Series
0.7 – 1.2 (5 – 5.5" length)	Thermalloy (Extruded) 6423, 6443, 6441, 6450 Series
1.0 – 5.4 (3" length)	Thermalloy (Extruded) 6427, 6500, 6123, 6401, 6403, 6421, 6463, 6176, 6129, 6141, 6169, 6135, 6442 Series
1.9	IERC E2 Series (Extruded)
2.1	IERC E1, E3 Series (Extruded)
2.3 – 4.7	Wakefield 600 Series
4.2	IERC HP3 Series
4.5	Staver V3-5-2
4.8 – 7.5	Thermalloy 6001 Series
5 – 6	IERC HP3 Series
5 – 10	Thermalloy 6013 Series
5.6	Staver V3-3-2
5.9 – 10	Wakefield 680 Series
6	Wakefield 390 Series
6.4	Staver V3-7-224
6.5 – 7.5	IERC UP Series
8	Staver V1-5
8.1	Staver V3-5
8.8	Staver V3-7-96
9.5	Staver V3-3
9.5 – 10.5	IERC LA Series
9.8 – 13.9	Wakefield 630 Series
10	Staver V1-3
11	Thermalloy 6103, 6117 Series
TO-220 Packages (See Note 1)	
4.2	IERC HP3 Series
5 – 6	IERC HP1 Series
6.4	Staver V3-7-225
6.5 – 7.5	IERC VP Series
7.1	Thermalloy 6070 Series
8.1	Staver V3-5
8.8	Staver V3-7-96
9.5	Staver V3-3

Table 1 Heat Sink Selection Guide (Cont.)

θ_{SA} Approx. (°C/W)	Manufacturer[3] and Type
10	Thermalloy 6032, 6034 Series
12.5 – 14.2	Staver V4-3-192
13	Staver V5-1
15	Thermalloy 6030 Series
15.1 – 17.2	Staver V4-3-128
16	Thermalloy 6072, 6106 Series
18	Thermalloy 6038, 6107 Series
19	IERC PB Series
20	Staver V6-2
20	Thermalloy 6025 Series
25	IERC PA Series
TO-92 Packages	
30	Staver F2-7
46	Staver F5-7A, F5-8-1
50	IERC RUR Series
57	Staver F5-7D
65-5	IERC RU Series
72	Staver F1-7
85	Thermalloy 2224 Series
TO-5 and TO-39 Packages	
12	Thermalloy 1101, 1103 Series
12 – 16	Wakefield 260-5 Series
15	Staver V3A-5
22	Thermalloy 1116, 1121, 1123 Series
22	Thermalloy 1130, 1131, 1132 Series
24	Staver F5-5C
25	Thermalloy 2227 Series
26 – 30	IERC Thermal Links
27 – 83	Wakefield 200 Series
28	Staver F5-5B
34	Thermalloy 2228 Series
35	IERC Clip Mount Thermal Link
39	Thermalloy 2215 Series
41	Thermalloy 2205 Series
42	Staver F5-5A
42 – 65	Wakefield 296 Series
46	Staver F6-5, F6-5L
50	Thermalloy 2225 Series
50 – 55	IERC Fan Tops
53	Thermalloy 2211 Series
55	Thermalloy 2210 Series
56	Thermalloy 1129 Series
58	Thermalloy 2230, 2235 Series
60	Thermalloy 2226 Series
68	Staver F1-5
72	Thermalloy 1115 Series
Power Watt (similar to TO-202) **Packages** (See Note 2)	
12.5 – 14.2	Staver V4-3-192
13	Thermalloy 6063 Series
13	Staver V5-1
15.1 – 17.2	Staver V4-3-128
19	Thermalloy 6106 Series
20	Staver V6-2
24	Thermalloy 6047 Series
25	Thermalloy 6107 Series
37	IERC PA1-7CB with PVC-1B Clip
40 – 42	Staver F7-3
40 – 43	Staver F7-2
42	IERC PA2-7CB with PVC-1B Clip
42 – 44	Staver F7-1

Notes

1. Most TO-3 heat sinks can also be used with TO-220 packages with appropriate hole patterns.
2. Most TO-220 heat sinks can be used with the Power Watt package.
3. IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
   Staver Co., Inc.: 41-51 N. Saxon Ave., Bay Shore, N.Y. 11706
   Thermalloy Inc.: 2021 W. Valley View Lane, Dallas, TX 75234
   Wakefield Engineering, Inc.: Audubon Rd., Wakefield, MA 01880

FAIRCHILD
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Testing, Quality and Reliability

Testing

For proper interpretation and understanding of published data sheet parameters, one must understand the philosophy used by Fairchild in testing its linear products.

All Fairchild products are tested during various phases of the manufacturing process to ensure the shipment to the customer of a reliable product that meets or exceeds the guaranteed specifications. Fairchild tests its finished products, at room ambient, with automated equipment that operates at relatively high speeds. It is not unusual to perform more than a hundred tests on a simple product; each test normally takes a few milliseconds and testing of one device is normally completed in a matter of a few hundred milliseconds. Parameter variations due to internal heating of the device are minimized during factory testing. During normal operation of the device, the effects of the internal heating on the device performance must be kept in mind by the user as well as the person performing incoming testing in the laboratory. Internal power dissipation and thermal resistance numbers supplied in each data sheet will be helpful in determining temperature rise due to internal heating.

Except for Aerospace and Defense products or customers that specifically request it, normally no temperature testing is done on production devices. How does Fairchild then guarantee the parameters it specifies over the temperature extremes? We do this by thorough characterization of the product. Prior to release to production of a new product, or a product modification, a representative sample from three production runs is tested in temperature chambers over the operating temperature range of the device. This characterization testing, normally done on automated testers, is supplemented by bench testing and covers all of the "guaranteed", "typical", as well as parameters not normally specified on the product data sheet. The results of this characterization are thoroughly analyzed and from them, the "minimum", "typical" and "maximum" data sheet values are determined. In addition, room temperature guardbands are established and yield enhancements are identified. The characterization is an on-going process and normally the correlation between room temperature and operating temperature extremes are very good. Product integrity and compliance to data sheet parameters are checked periodically by Quality Asssurance by sample testing outgoing material at temperature extremes.

In summary then:

a. Production testing is done at high speeds and normally at room temperature only.
b. Compliance to temperature specifications is accomplished through on-going characterization and room temperature guardbands.
c. Periodic sample testing at temperature extremes is done by Quality Assurance on outgoing material to ensure compliance.

Quality and Reliability

It is the policy of Fairchild Semiconductor Corporation that every employee be committed to pursuing excellence by producing zero defect products and services in conformance with customer requirements. Prevention, detection, and control methodologies are applied throughout the manufacturing and administrative processes to strive for zero defects and continual quality improvement.

Specific programs for quality improvement include, but are not limited to, the following:

- **Quality training. A formal nationally-recognized program involving all engineering and management personnel. Operators are formally trained and certified for all production operations.**
- **Statistical Process Control (SPC). A formal program of characterization and control limit setting.**
- **Electrostatic Damage (ESD) control and measurement. A program to contain the effects of ambient static and to reduce device sensitivity.**
- **Design control. A program to assure adequate rules and implementation, process control, and demonstrated conformance of processes, materials, and products.**
- **Measurement. In-process and outgoing attributes. Reconciliation of internal versus customer results.**
- **Reliability hazard prevention. In-process monitors for the prevention of hazards such as moisture, pinholes, step coverage, contamination, and passivation integrity.**
- **Reliability monitor. Outgoing reliability as measured by operating life in dry and moisture environments and other stress tests.**

For continual product improvement the Linear division maintains failure analysis capability, return material system, and specification review to provide customer assistance and to focus factory actions for response to fitness for use issues. The failure analysis laboratory contains fundamental tools for optical and electrical definitions, for decapsulation, for specimen preparation, for SEM, EDAX, and electrical microprobe. Expert diagnosis is provided by internal personnel and augmented with outside consultation.

Reliability is product performance in time, stress, and environment. The science of reliability is to define those attributes and controls necessary to assure and improve time/stress/environment performance. Finished product reliability is measured periodically to assure conformance with life requirements, and data is available quarterly for operating life and moisture life attributes.

Quality is performance now, conformance to specification, and fitness for use. Basic elements of the Linear division quality system are controlled documents and in-process inspections. Outgoing quality is measured for all lots to assure conformance to specification, and data is available monthly for electrical, visual, and mechanical attributes.

Commercial Product Flow

Wafer fab must begin with controlled raw materials such as silicon, gasses, and chemicals. Post alloy sample probes and other monitors assure built-in quality. Automated electrical testing is performed at wafer level. The fabricated wafer is processed with automated die preparation that includes saw and pick and place.

The die (or chip) itself is assembled with automated die attach and wire bond, molded, and finished with automated handling at trim, form, test, and lead scan operations. In-process controls assure die attach, wire bond, molding, trim, and form. Emphasis on automation has reduced variability and enhances our ability to control quality and reliability.

Finished product is inspected on a lot basis for electrical, visual, and mechanical parameters. Records are maintained for all inspections, and deviations from conformance are reviewed monthly for trend analysis and corrective improvements. Accept number for all inspections is zero.

Standard Cell Design with Fairchild CLASIC Approach

Introduction

The Fairchild CLASIC (Customizable Linear Applications Specific Integrated Circuits) approach brings to the systems designer a level of sophistication that will enable VLSI solutions requiring analog and mixed analog/digital functions to be integrated cost effectively. The CLASIC approach offers:

- **Bipolar and CMOS Technologies**
- **Standard Cell and Array Methodologies**
- **Customer CAD Tools That Allow Design and Simulation with Higher Level Building Blocks**

By offering a cell library of pre-designed commonly identified function blocks such as op amps, comparators, DAC's, VCO, PLL, gates, flip flops, counters, etc., and CAD tools to combine them, the CLASIC system considerably reduces the time and the risks associated with VLSI designs. The designers task is somewhat more complicated, but similar to designing a printed circuit board using standard IC's. Most importantly, however, with the CLASIC approach the customer can select the level of design participation desired. At the lowest level the customer can simply provide a functional description of the desired design and a CLASIC applications engineer will translate this into a standard cell schematic. As the user gains experience and confidence with the CLASIC approach, any level of design up through layout can be accomplished with the appropriate CAD tools at the users location if desired. The user has a choice of options best suited to his needs and experience.

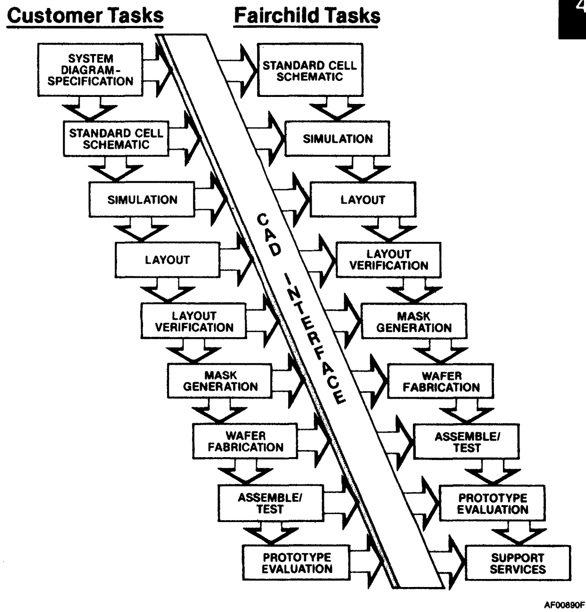
The Cell Library

There are presently over 150 cells in the CLASIC library covering a broad range of linear and digital function with additional cells being added on a continual basis. The following is a partial list of the type of cells available:

Linear

- **Amplifiers** — **Op Amps, General Purpose**; **Op Amps, Low Offset**; **Op Amps, Programmable**; **Norton Amp**; **AGC Amp**; **Video Amp**; **Control Amp**
- **Comparators** — **ECL Output**; **TTL Output**; **General Purpose**
- **Data Converters** — **A/D**; **D/A**
- **Line Drivers/Receivers** — **422**; **485**

Selecting a Design Entry Level



- **Peak Detectors**
- **PLL**
- **Programmable Current Sources**
- **VCO's**
- **Wave Generators**
- **Zero Crossing (Detectors)**
- **555 Timer**

Digital

- **Gates**
- **Flip Flops**
- **One Shots**
- **Edge Detectors**
- **MUX's**
- **Counters**
- **Registers**
- **Decoders**
- **Delay Cells**
- **Drivers**
- **Translators (ECL/TTL)**

The linear performance offered by Bipolar CLASIC cells is based on NPN f_t of 2.5 GHz and PNP f_t of 40 MHz. The logic cells are based on high performance ECL offering gate delays of 1.5 ns at fanout of 3 and D flip flop toggle frequencies better than 100 MHz.

The CMOS cell library is presently based on a 3 micron double poly process providing offset voltages of less than 5 mV, unity gain BW of 2 MHz, gate delays of 5 ns at fan out of 3 and D flip flop toggle frequencies at better than 50 MHz. A new generation of cells is presently in design for a 2 micron CMOS double poly process which will provide gate delays of 1.5 ns and D flip flop toggle frequencies better than 200 MHz.

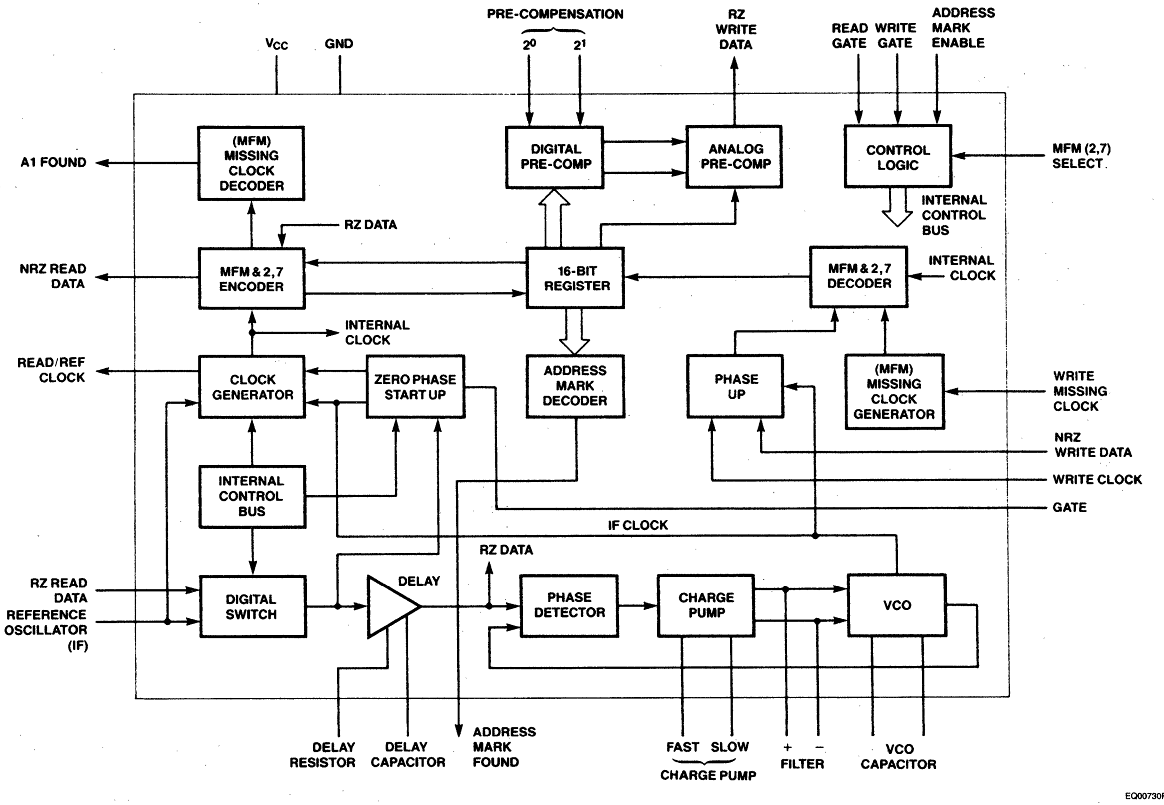
CLASIC CAD

An important feature of the CLASIC system is to provide comprehensive CAE packages for PC's, workstations and mainframes. Using these software tools the customer can perform all of the design steps from schematic capture to circuit simulation and verification in their own laboratory.

A CLASIC software package for VAX mainframe systems will also be offered. If desired, customers can also work through Fairtech centers which are a worldwide design center network.

In any case, the starting point for the customer is to describe the required system function in terms of the CLASIC cells. Where a requirement is not met with an existing cell, either the customer can create a new cell by using the macro level components such as transistors, resistors and capacitors which are available and described in the library or the special requirements can be described to Fairchild's CLASIC applications engineers who can design the cell for incorporation into the IC design. New cells are being continually added to the library to serve the vast majority of the customers needs.

Figure 1 Data Separator/Encoder Block Diagram — A CLASIC Example



CLASIC CAD I (PC Based)
- **Fairchild Cell Libraries**
- **Schematic Capture**
- **Simulation Software**
- **Net List Post Processor**
- **Test Generation**
- **Documentation**
  - **Installation Manual**
  - **Design Applications Manual**
  - **Simulation Manual**

CLASIC CAD II (Workstation Based)
For those customers who own or plan to purchase one of the popular workstations, CLASIC cell libraries with simulation models will be offered.

CLASIC CAD III (VAX based)
The CAD system used internally by the CLASIC groups which includes complete capability from cell schematic through layout verification, can be made available for those customers desiring this level of performance.

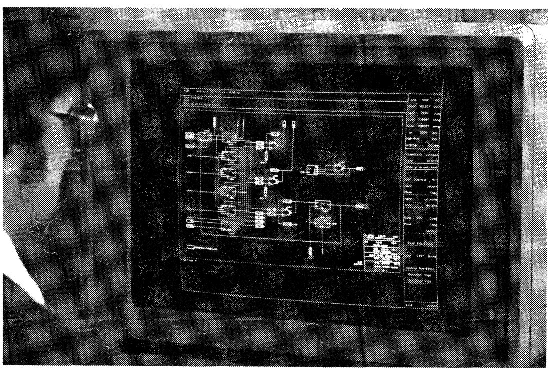
Design Example:

Task: To design a disk drive data separator/encoder decoder on a single chip. Original design required 25 IC packages plus numerous discretes.

Approach: Use CLASIC Standard Cell Methodology.

Step 1: Translate system level functional diagram into standard cell schematic. Create new cells if required. *See Figure 1.* Search cell library for required functions.

Step 2: Perform Schematic Capture on desired CAD tool. Net list generation



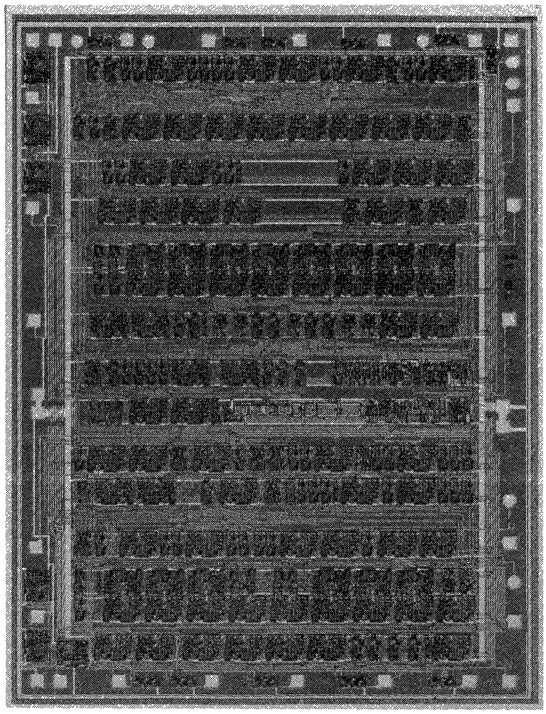
Step 3: Run simulation on schematic from Step 2. Redesign and/or reselect cells as appropriate to achieve desired performance. If breadboarding is desired for critical areas, kit parts of various standard cells are available in packaged form. This permits breadboarding to be accomplished with relative ease and accuracy.

Step 4: Auto route and place run on desired CAD tool.

Step 5: Layout verification run on desired CAD tool.

Step 6: Mask generation.

Step 7: Wafer Fabrication.



Step 8: Assemble/Test (Fast turnaround prototype assembly; 1 day service).

Step 9: Evaluate prototypes.

Fairchild can perform all the steps outlined 1 through 9, however with entry level CAD tools steps 1 through 3 can be achieved by the customer with minimal training and investment resulting in rapid payback and improved communications and efficiency.

CLASIC™

Available Packages:
set from attachment

No. of Pins	Plastic Dip	SOIC	Side Brazed & Ceramic Dip	PLCC	LCC	Flat Pak
8	●	●	●			
14	●	●	●			●
16	●	●	●			●
20	●		●		●	
24	●		●	●	●	●
28	●		●	●	●	●
32					●	●
40	●		●		●	
44				●	●	
68			●	●	●	
132						●

FAIRCHILD

A Schlumberger Company

µA24H80 Winchester Disk Servo Preamplifier

Description

The µA24H80 provides termination, gain, and impedance buffering for the servo read head in Winchester disk drives. It is a differential input, differential output design with fixed gain of approximately 100. The bandwidth is guaranteed greater than 30 MHz.

The internal design of the µA24H80 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-lead DIP, 10-lead flatpak, or SO-8 package suitable for surface mounting.

- **Low Input Noise Voltage**
- **Wide Power Supply Range (8.0 V To 13 V)**
- **Internal Damping Resistors (1.3 kΩ)**
- **Direct Replacement For SSI 101A, With Improved Performance**

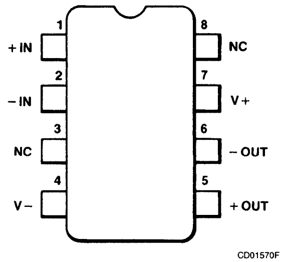
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP and Flatpak (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
10L-Flatpak	0.79 W
Supply Voltage	15 V
Output Voltage	15 V
Differential Input Voltage	±1.0 V

Notes

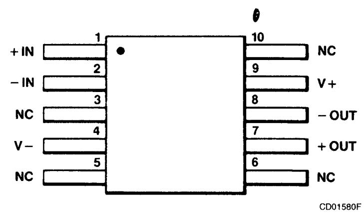
1. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Ceramic DIP and Flatpak.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, the SO-8 at 6.5 mW/°C, and the Flatpak at 5.3 mW/°C.

Connection Diagram 8-Lead DIP and SO-8 Package (Top View)



Device Code	Package Code	Package Description
µA24H80RC	6T	Ceramic DIP
µA24H80SC	KC	Molded Surface Mount
µA24H80TC	9T	Molded DIP

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Device Code	Package Code	Package Description
µA24H80FC	3F	Flatpak

Description of Lead Functions

Name	Description of Functions
V+	Positive Differential Supply with respect to V−
V−	Negative Differential Supply with respect to V+
+IN	Positive Differential Input
−IN	Negative Differential Input
+OUT	Positive Differential Output
−OUT	Negative Differential Output
NC	No connection

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 8.0$ V to 13.2 V, unless otherwise specified.

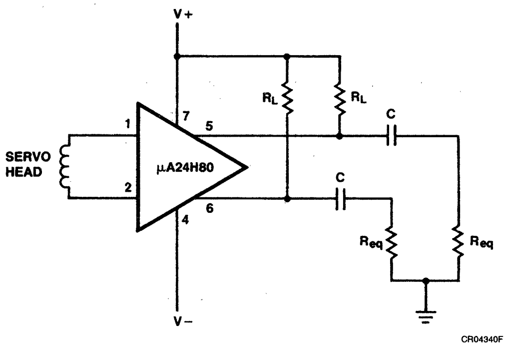
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
G	Gain (differential)[4]	$R_p = 130\ \Omega$, $V_{CC} = 12$ V	80	100	120	
		$R_p = 130\ \Omega$, $V_{CC} = 12$ V $T_A = 0°C$ to $70°C$	70		130	
BW	Bandwidth (3.0 dB)[2]	$V_I = 0.5\ mV_{p-p}$	30	65		MHz
R_I	Input Resistance		1040	1300	1560	Ω
C_I	Input Capacitance			3.0		pF
V_I	Input Dynamic Range (differential)	$R_p = 130\ \Omega$, $V_{CC} = 12$ V	3.0			mV_{p-p}
I_s	Supply Current	$V_{CC} = 12$ V		20	25	mA
ΔV_O	Output Offset (differential)	$R_p = 130\ \Omega$, $R_s = 0\ \Omega$			200	mV
V_n	Equivalent Input Noise[2, 3]	$R_s = 0\ \Omega$, BW = 4.0 MHz		1.5	2.0	μV
PSRR	Power Supply Rejection Ratio[1]	$R_s = 0\ \Omega$, f = 5.0 MHz	55	70		dB
$\Delta G/\Delta V$	Gain Sensitivity (Supply)	$R_p = 130\ \Omega$, $\Delta V_{CC} = \pm 10\%$			±0.5	%/V
$\Delta G/\Delta T$	Gain Sensitivity (Temp)	$R_p = 130\ \Omega$, $T_A = 25°C$ to $70°C$		−0.1		%/°C
CMR	Common Mode Rejection[1] (Input)	f = 5.0 MHz	60	75		dB

Notes

1. Tested at DC, guaranteed at frequency
2. Guaranteed, but not tested in production
3. Equivalent input noise (additional specification):

TYP	MAX	UNIT	CONDITION
3	4	μV	BW = 15 MHz[2]
0.85	1.0	$nV/\sqrt{Hz}$	BW = 15 MHz[2]

Typical Applications



Notes

1. Leads shown for 8-lead DIP.
2. R_{eq} is equivalent load resistance.
3. $R_P = \dfrac{R_L \cdot R_{eq}}{R_L + R_{eq}}$
4. $G = 0.77\ R_P$
   Where R_P = value from Note 3 (above) in ohms.

μA2460 • μA2461 Servo Control Chips

Description

The μA2460 and μA2461 provide the analog signal processing required between a drive resident microprocessor and the servo power amplifier for Winchester disk closed loop head positioning. The μA2460 and μA2461 receive quadrature position signals from the servo channel; and from these, derive actual head seek velocity as well as position-mode off-track error. In the seek mode, the Digital to Analog Converter (DAC) is used to command velocity, while actual velocity is obtained by differentiating the quadrature position signals provided at V1 for external processing. The velocity signal (V2), obtained by integrating the motor current, is also available for extra damping, if desired. Further, the DAC may be used for detenting the head off-track for any purpose such as thermal compensation or soft-error retrys.

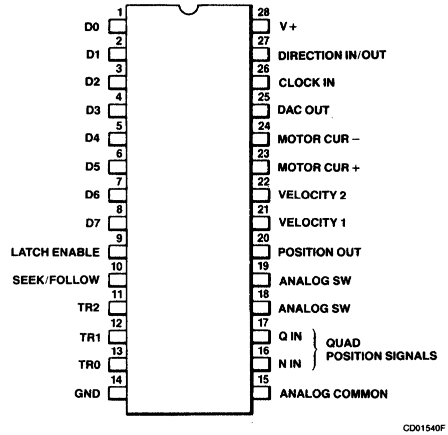
- **Microprocessor Compatible Interface**
- **Quadrature Di-Bit Compatible**
- **On Board DAC**
- **Velocity V1 Derived From Position Signal**
- **Velocity V2 Derived From Motor Current**
- **Quarter-Track-Crossing Signal Outputs**
- **Minimal External Components**
- **Compatible With μA2470 Demodulator**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
PLCC	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
PLCC (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
28L-Ceramic DIP	2.50 W.
28L-PLCC	1.39 W.
Supply Voltage	15 V Max
Analog Common Voltage	8.0 V Max
All inputs	V supply Max

Notes
1. $T_{J\ Max}$ = 150°C for the PLCC, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C, and the 28L-PLCC at 11.2 mW/°C.

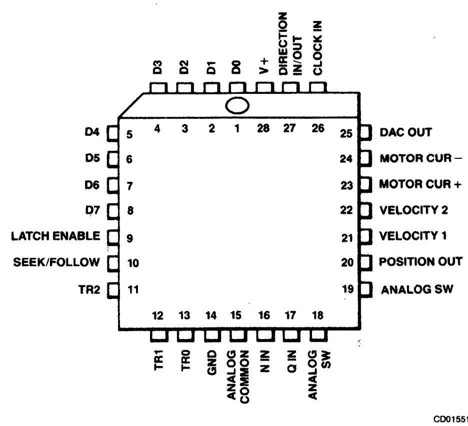
Connection Diagram
28-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA2460DC	FM	Ceramic DIP
μA2461DC	FM	Ceramic DIP

Connection Diagram
28-Lead PLCC (Top View)



Order Information

Device Code	Package Code	Package Description
μA2460QC	KH	Plastic Leaded Chip Carrier
μA2461QC	KH	Plastic Leaded Chip Carrier

Description of Lead Functions

Lead	Name	Description of Function
Inputs		
1 – 8	DAC Input Word ($D_0 - D_7$)	Programs DAC output, 00000000 = Analog Command Lead 1 = LSB Lead 8 = MSB
9	Latch Enable	Allows present DAC input word to be latched
10	Seek/Follow Mode	Configures the feedback loop for either seeking or track-following. (High = Seek, Low = Follow)
14	Ground	
15	Analog Common	Analog signal reference input level (5.0 V)
16	N	Normal position input signal.
17	Q	Quadrature position input signal.
23	Motor Current +	Motor current sense input to motor current integrator.
24	Motor Current –	
26	Clock	4.0 MHz (maximum) input square wave.
27	Direction In/Out	Changes the polarity of DAC output from positive to negative consistent with the desired direction of head motion.
28	V+	12 V supply
Outputs		
11	Track 2^2 (TR2)	TTL signal indicating N > Q (for μA2460) TTL signal whose frequency is 2 times N (or Q) (for μA2461).
12	Track 2^1 (TR1)	TTL signal indicating $\overline{N}$ > Q (for μA2460) TTL signal whose frequency is 4 times N (or Q) (for μA2461).
13	Track 2^0 (TR0)	TTL signal whose frequency is 8 times N (or Q).
18	Analog Switch	Analog switch to be used externally for changing from seek to follow.
19	Analog Switch	
20	Position Output	Analog signal representing sensed off track amplitude
21	Velocity 1	Analog output representing velocity processed from position signals N and Q.
22	Velocity 2	Analog output representing the integral of motor current.
25	DAC Output	Used to command velocity and position.

Figure 1 Head Actuator Control System

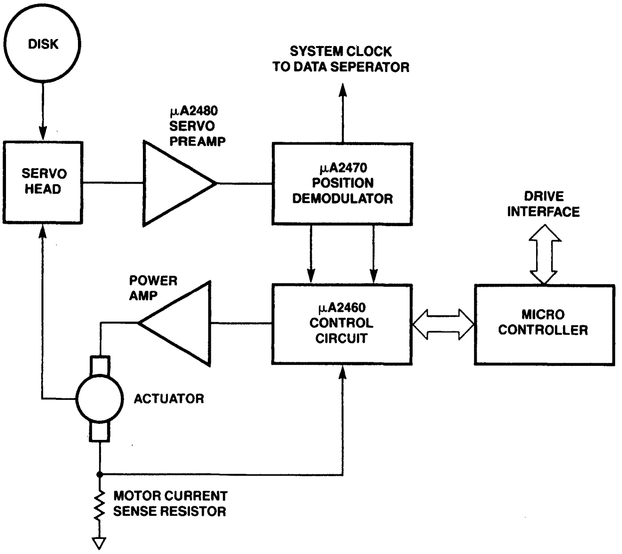
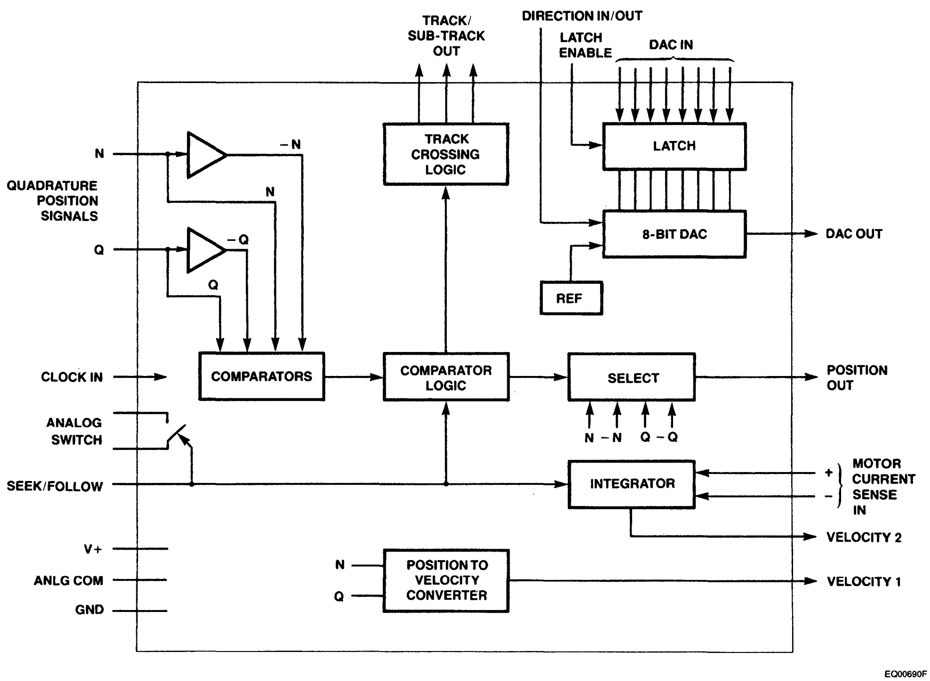


Figure 2 Block Diagram



5

Functional Description

Figure 2 shows a block diagram of the μA2460/μA2461 Servo Controller.

Power Supply And Reference Requirements

The μA2460/μA2461 is designed to operate from a single supply of 10 V to 12 V. Also required is a reference voltage of 5.0 V called Analog Common which serves two functions; all analog signals will be referenced to this voltage and in addition the internal DAC will use it to set full scale.

A clock signal must be provided as a reference for the internal switched capacitor position differentiator and motor current integrator. The clock signal should be a sine or square wave between Analog Common and ground at a maximum frequency of 4.0 MHz.

All digital inputs and outputs are TTL compatible levels referenced to ground.

Input Signals And Track Crossing Outputs

The input format selected for position feedback is consistent with a large class of sensors that generate two cyclical output signals displaced in space phase by 90 degrees (quadrature signal pairs). These sensors include resolvers, inducto-syns, optical encoders, and most importantly, servo demodulators designed for rigid disk head position sensing.

The input signals N and Q are quadrature quasi triangular waveforms with amplitudes of ±2.5 V nominal referenced to Analog Common. The periods of the input signals are subdivided by internal comparators and logic and sent to the Track Crossing outputs T_0, T_1, and T_2. The relationship of these outputs to the inputs N and Q is shown in *Figure 3a* (for μA2460) and *Figure 3b* (for μA2461).

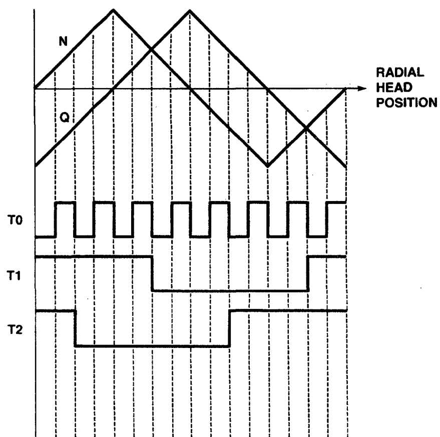
Note that different servo patterns may yield different numbers of track centerlines for each period of the quadrature signal pair. The relationship of T_0, T_1, and T_2 to N and Q is independent of track centerlines, leaving the correct interpretations to the microcontroller.

DAC

The DAC is an 8-bit, buffered input, voltage output digital to analog converter. The output voltage with an input code of all zeros is equal to Analog Common. Full scale is equal to Analog Common ±2.35 V. The polarity depends on the Direction In Signal; Direction In High will result in a positive DAC output.

The DAC enable line when high will cause the DAC's input buffer to become transparent, i.e. input data will affect the output voltage immediately. When DAC enable is brought low the data present on the input lines will be latched and any further changes to the input data will not change the output voltage. The DAC functions in both Seek and Follow Mode. During Seek Mode the DAC out-

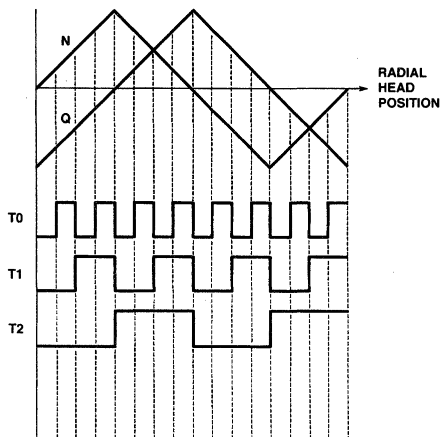
Figure 3a Track Crossing Outputs (for μA2460)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1
T2	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1

CR04850F

Figure 3b Track Crossing Outputs (for μA2461)



T0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
T1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
T2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

CR04190F

put is used as a velocity reference. In Follow Mode the DAC output can be summed into the position reference signal to offset the heads from track center.

Analog Switch
An uncommitted single pole single throw analog switch with an ON resistance of approximately 100 Ω is provided. This switch is ON during Follow Mode.

Mode Select
The two major intended operating modes for the μA2460 are controlled by the microcontroller via the SEEK/FOLLOW input. Mode Select input high enables Seek Mode, low enables Track Follow Mode.

SEEK, when asserted by the microcontroller along with DIRECTION and a non-zero VELOCITY value as inputs, causes the actuator system to accelerate in the requested direction. During the ensuing motion, the actuator system will come under velocity feedback control. The velocity feedback signal is created by differentiation of the quadrature position signals and, additionally, by integration of motor current.

FOLLOW, the negation of SEEK, changes the feedback loop to a track-following or position mode. Position servos are typically second order systems and without loop compensation are potentially unstable. External components are used, along with the μA2460, to achieve stable track following performance. Velocity information (V1) is made available as an output in this mode as an aid in stabilizing certain loops. If non-zero data is supplied to the velocity latches in this mode, it will result in a track offset in the direction indicated by DIRECTION IN/OUT. *Figure 4* shows typical seek operation.

Position Output
When the μA2460/μA2461 is set to Seek Mode the signal from Position Output lead is shown in *Figure 5.* This signal is made by switching the position inputs, (N and Q) through an inverter if required, ($\overline{N}$ and $\overline{Q}$) to the output using the track crossing signals. It can be used, if desired, to interpolate between DAC steps by attenuating it and summing it with the DAC output.

Track Follow Mode is entered when the heads are near the end of a seek, usually within one half to one track away from the target track centerline. The final setting to the track center is done by the position loop.

When the device is switched to Follow Mode, the position input signal (N, $\overline{N}$, Q or $\overline{Q}$) that is currently selected to the output is latched and the Position Out signal follows the selected position input signal until the device is switched back to Seek Mode. This implies that the switch to Follow Mode must not be made until the signal that will be the correct Position error signal for the target track is present at the output. If track centers are defined as the zero crossings of both N and Q this means that the switch to Follow Mode must be made less than one-half track away from the target track. (This is with respect to a convention of 4 track per encoder cycle, so switching must be done within 90° of the period of N or Q).

Figure 4 Typical Seek

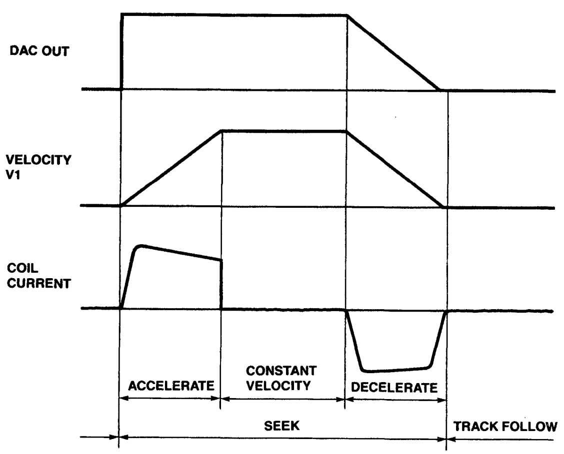
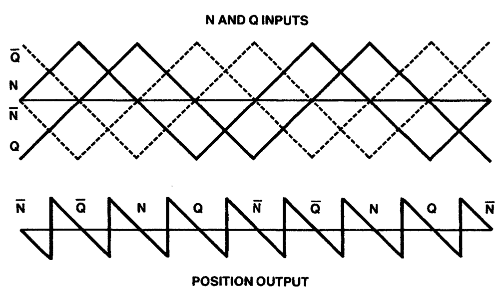


Figure 5 Position Output During Seek Mode



Velocity Outputs
There are two analog signal outputs representing velocity. The first (V1) is derived by differentiating the position input signals. The entire differentiator is on-chip, using switched capacitor techniques and requires no external components.

The transfer function of the differentiator is:

$$V_O = dv/dt \text{ (input)} \times 14.3/f \text{ (clock) Hz}$$

As an example; a 10 kHz triangular signal pair into N and Q of 6.0 V peak-to-peak amplitude (dv/dt = 120 kv/sec) would result in a velocity voltage output of 1.716 volts referenced to Analog Common with a clock of 1.0 MHz. The polarity will be positive if N is leading Q by 90 degrees and negative if Q is leading N. This block functions during both Seek and Follow modes.

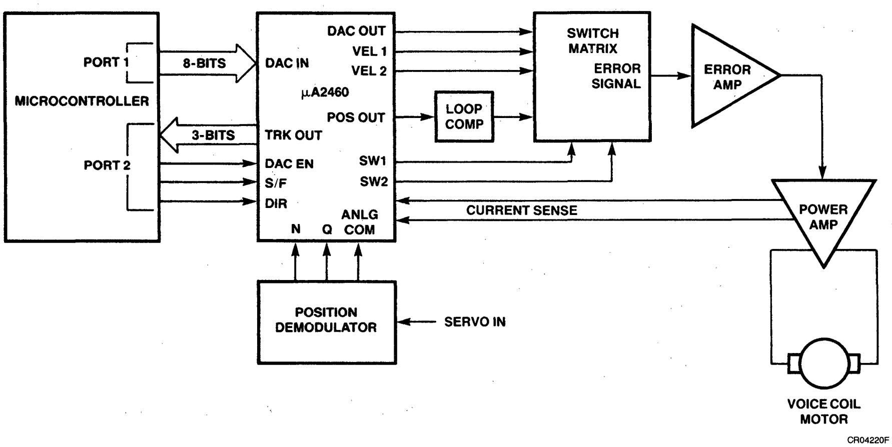
The second velocity output is obtained by integrating a voltage proportional to the current in the motor using the following function:

$$dv/dt \text{ (out)} = V\ (+I_{in} - -I_{in}) \times 2 \times 10^{-4}\ f \text{ (clock) Hz.}$$

The motor current integrator output is clamped to Analog Common during Follow Mode and is released at the initiation of a seek.

Figure 6 shows a typical application set up for the Servo Control chip.

Figure 6 Typical Application Setup



μA2460, μA2461
Electrical Characteristics T_A = 0°C to 70°C, V_{CC} = 12 V, f_{clk} = 2.0 MHz, Analog Common = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Digital I/O	Input Voltage LOW				0.8	V
	Input Voltage HIGH		2.0			
	Output Voltage LOW	I_{OL} = 2.5 mA			0.45	
	Output Voltage HIGH	I_{OH} = 40 μA	2.4			
	Input Load Current	V_I = 0 V to V_{CC}			0.2	mA
Clock Input	Input Comparator Reference Level		2.0	2.5	3.0	V
	Input Impedance		15	20		kΩ
DAC	Linearity[1]		−1		+1	LSB
	Resolution			8.0		bits
	Differential Nonlinearity		Monotonicity Guaranteed			
	Full Scale Output Voltage	Direction In High	7.25	7.35	7.45	V
		Direction In Low	2.55	2.65	2.75	
	Zero Scale Voltage			5.0		
	Output Offset Voltage				±10	mV
	Settling Time[2, 4]	To ½ LSB All bits ON or OFF				μs
Position Inputs	Input Voltage Range		1.0		9.0	V
	Input Impedance		15	20		kΩ
Analog Switch	On Resistance	V_{CM} = 0 V to 12 V		100	200	Ω
	Off Leakage[3]			2.0	100	nA
Position Output	Output Voltage Swing	R_L = 15K Follow Mode	1.0		9.0	V
	Voltage Gain		0.9		1.1	—
	Output Offset Voltage				±20	mV
Velocity Outputs	Output Voltage Swing	R_L = 15K	1.0		9.0	V
	Output Offset Voltage V2				±20	mV
	Output Offset Voltage V1				+15	

μA2460, μA2461 (Cont.)
Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 12$ V, $f_{clk} = 2.0$ MHz, Analog Common = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{CC}	Positive Supply	$V_{CC} = 13.2$ V		10	15	mA
I_{SS}	Negative Supply	$V_{CC} = 13.2$ V	−15	−10		mA
I_{AC}	Analog Common I		−2.0	0	+2.0	mA
V1 — Differentiator	Linearity	$f_{clk} = 1.0$ MHz to 4.0 MHz; $f_{N/Q} \leqslant 10$ kHz		0.25		%
V2 — Integrator	Linearity	$f_{clk} = 1.0$ MHz to 4.0 MHz		1.0		%

Notes
1. DAC Linearity is a function of the Clock frequency; Linearity at 1.0 MHz is typically ± ½ LSB.
2. DAC Settling Time is approx 5.0 μs, plus a delay of maximum 32 x Clock period i.e., 5 + 32 μs at Clock = 1.0 MHz Minimum could be 5.0 μs.
3. Equivalent to 50 MΩ.
4. Guaranteed, but not tested in production.

μA2470 Winchester Disk Position Demodulator

Preliminary

Linear Division Disk Drives

5

Description

The μA2470 is a monolithic analog/digital integrated circuit which decodes a quadrature di-bit pattern from the dedicated servo surface of a disk file into head position, track data and timing components. The μA2470 accepts this signal after it has been amplified by a μA2480 type of preamp and processes the various components for input to a μA2460 type servo controller. These three circuits and their external components form a disk servo control system for closed loop applications.

- **Quadrature Position Signals**
- **Programmable Charge And Discharge In Peak Detectors**
- **Sync Lock By PLL With Lock Detection Output**
- **NRZ Track Data And Clock Output**
- **Band Gap 5.0 V Reference Provided**
- **AGC Amplifier With 36 dB Range**
- **Servo Frame Rates To 400 kHz**
- **Compatible With μA2480 Servo Preamp And μA2460 Servo Control Chip**
- **Standard 5.0 V And 12 V Power Supplies**

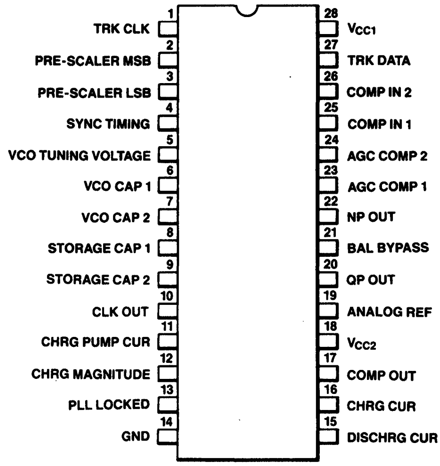
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Internal Power Dissipation[1, 2]	
28L-Ceramic DIP	2.50 W
Supply Voltage, V_{CC1}	6.0 V
Supply Voltage, V_{CC2}	15 V

Notes

1. $T_{J\ Max} = 175°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 16.7 mW/°C.

Connection Diagram
28-Lead DIP
(Top View)

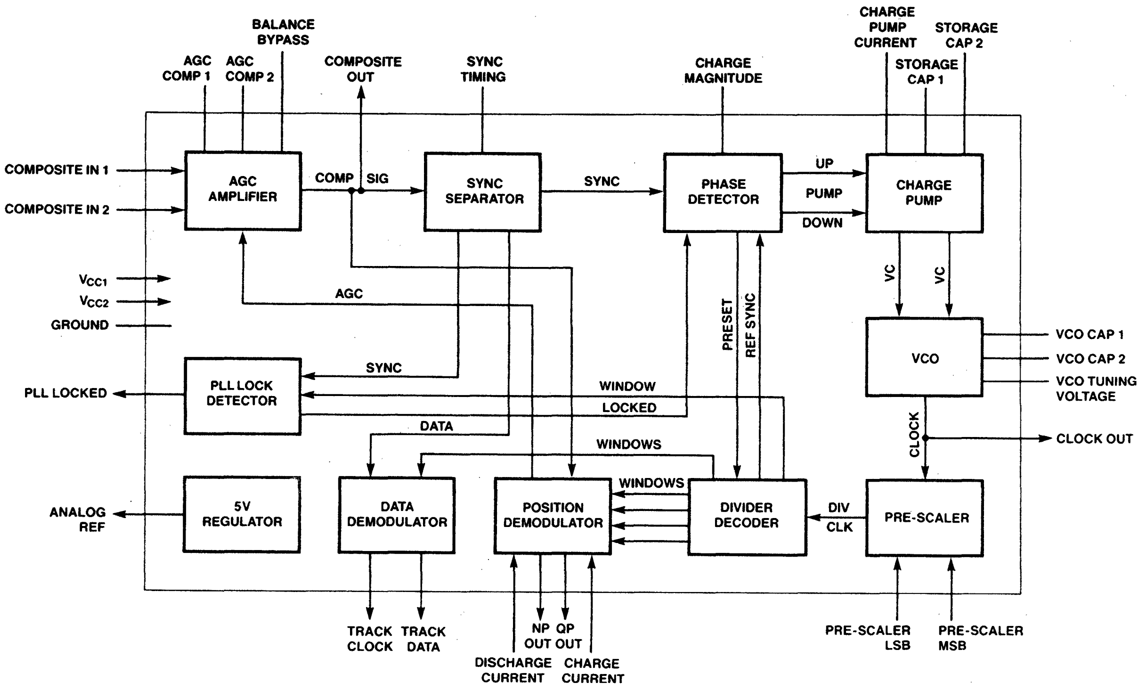


CD01560F

Order Information

Device Code	Package Code	Package Description
μA2470DC	FM	Ceramic DIP

Block Diagram



EQ00700F

Description Of Lead Functions

Lead	Name	Function
Input Signals		
2 3	Pre-scaler LSB Pre-scaler MSB	Programs the Pre-scaler for VCO frequency relative to the frame rate. Divide ratios of 32, 64, 96, and 128 are available. Inputs are TTL levels.
5	VCO Tuning Voltage	Voltage input sets the VCO Current.
11	Charge Pump Current	Voltage input sets the current level into the Loop Filter.
14	Ground	
18	V_{CC2}	12 V supply input.
25 26	Composite IN 1 Composite IN 2	Composite signal inputs.
28	V_{CC1}	5.0 V supply input.
Outputs		
1	Track Clock OUT	Clock output derived from the Sync signal. Used as reference for Track Data; TTL.
10	Clock OUT	VCO output; TTL.
13	PLL Locked	Logic high when PLL is locked; TTL.
17	Composite OUT	AGC Amplifier output.
19	Analog Reference	5.0 V reference output. Used as reference for N and Q outputs.
20	QP OUT	Quadrature position output.
21	NP OUT	Normal position output.
27	Track Data	NRZ data from missing Sync pulses; TTL.
External Components		
4	Sync Timing	Oneshot timing RC network. Sets length of window used in Sync Separator.
6-7	VCO Capacitor	VCO Timing Capacitor. Sets VCO center frequency.
8-9	Storage Capacitor	PLL Loop Filter.
12	Charge Magnitude	Oneshot timing RC network. Sets length of current pulse out of the Phase Detector.
15	Peak Detector Discharge Current	Resistor to Ground. Sets the internal peak detector discharge current.
16	Peak Detector Charge Current	Resistor to Ground. Sets the internal peak detector charge current.
21	Balance Bypass	Bypass capacitor for the offset cancelling circuit in the AGC Amplifier. Sets the low frequency roll off of the Amplifier.
23	AGC 1	Loop Filter capacitor for AGC Amplifier.
24	AGC 2	Bypass Capacitor for AGC Amplifier.

Theory Of Operation

The purpose of the μA2470 is to demodulate both analog and digital information from the composite servo signal as *shown in figure 1*. This signal contains the digital signals Data and Sync and the analog quadrature di-bit signals N, $\overline{N}$, Q, and $\overline{Q}$.

Data The track data is presented as NRZ with a companion clock signal for latch control. The track data is decoded from the first pulse in each servo cell. This data permits identification of index position, guardband etc. The codes and schemes are entirely at the user's option as no decoding is done on-chip.

Sync The sync pulse is the one pulse in the frame which is always present in every frame on every track. This pulse is used to synchronize the PLL and makes decoding the rest of the information in the frame possible.

Quadrature Position Signals The four position pulses are analog signals whose amplitude encodes the position of the disk file heads with respect to the data track centers. N and Q are in a quadrature relationship, i.e. when N and $\overline{N}$ are equal in magnitude the difference between Q and $\overline{Q}$ is at maximum and vice versa. Equal magnitudes of N and $\overline{N}$ represent odd tracks and Q and $\overline{Q}$ the even tracks.

AGC Amplifier The μA2470 AGC Amplifier is a fully differential design with a typical bandwidth of 20 MHz and active offset cancelling. The composite signal input level must be between 30 mV and 300 mV to be within the Amplifier's active AGC range. The offset cancelling circuit requires an external filter capacitor which provides control of the low frequency response. An external capacitor is used to control the AGC bandwidth. The AGC Amplifier output amplitude is typically 3.5 Vp-p and is available at an output lead on the device for monitoring.

Sync Separator The Sync Separator *shown in Figure 2* operates on the composite signal as it appears at the output of the AGC Amplifier. The hysteresis comparator has thresholds of +0.7 V and 0 V and produces pulses whose trailing edges are at the zero crossings of the composite signal. The trailing edges of these pulses trigger the oneshot. The output of the oneshot is AND-gated with the pulse stream from the hysteresis comparator to produce the sync pulse. The pulse length from the oneshot should only be long enough to enclose the sync bit as the next pulse in the stream. Sync separator timing is *shown in Figure 3*.

TRACK DATA DEMODULATOR The track data encoding flip-flop changes state whenever there is a data pulse present producing NRZ data for the user.

PHASE LOCK LOOP When a disk sync pulse is sensed by the Sync Separator, the PLL compares the phase of disk sync with the phase of a reference sync pulse generated by the window decoder. *Refer to Figure 4 and 5.* Every other sync pulse from the Sync Separator causes the window decoder counter to preset. This forces the decoder into phase alignment with the disk sync. Starting from a known condition allows a phase comparison to be made on the next frame by comparing the trailing edges of the reference sync with the disk sync pulses and outputing a correction signal to the charge pump to increase or decrease the VCO frequency to correct the phase error. On the next frame the cycle is repeated.

LOCK DETECTOR When the frequency and phase of the VCO are correct, the trailing edge of the sync pulse will coincide with the trailing edge of count 4 from the counter/decoder. The decoder generates a window from the end of count 3 to the end of count 5, so that the sync edge will ideally fall in the middle. Whenever the sync falls inside the window four consecutive times, lock is detected and the lock signal goes true. In order for the lock signal to be reset the sync pulse must be outside the window for four consecutive frames.

POSITION DEMODULATOR *Figure 6* shows the position signals as a function of servo head position. The Position Demodulator consists of four digitally enabled peak detectors, two summing amplifiers and a precision band gap reference. Each of the four peak detectors is enabled by the window decoder during one of the position pulses as *shown in Figure 7*. The N position output is derived by taking the difference between the first two peak detector outputs. The Q output is similarly obtained from the second pair. The outputs are referenced to the 5 V reference which is available as an output to be used as an analog baseline. The charging and discharging slew rates in the peak detectors are programmable by external resistors. The charging slew rate is associated with acquisition of the peak and the discharge slew rate controls the droop rate between peaks.

Figure 1 Composite Servo Signal

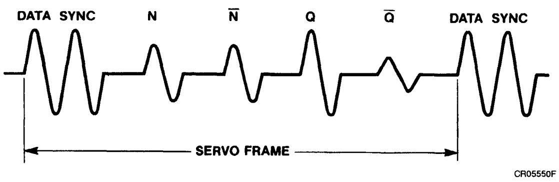


Figure 2 Sync Separator

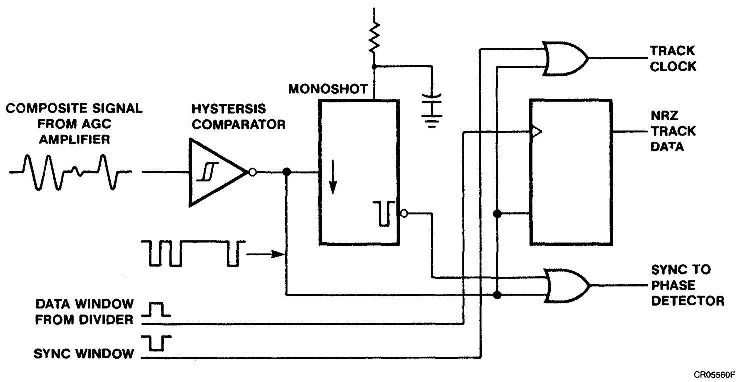


Figure 3 Sync Separator Timing

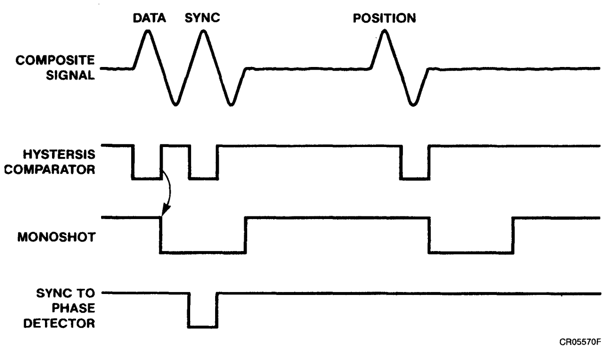


Figure 4 Phase Lock Loop Block Diagram

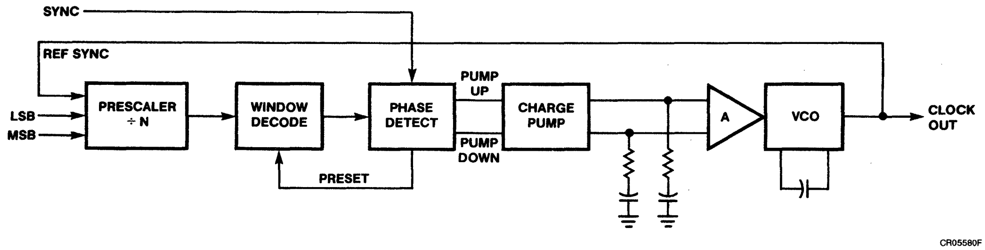
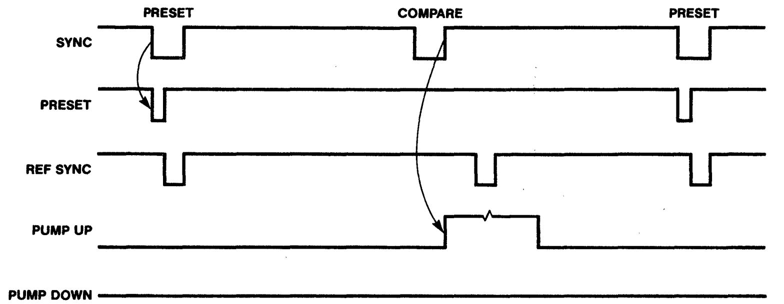
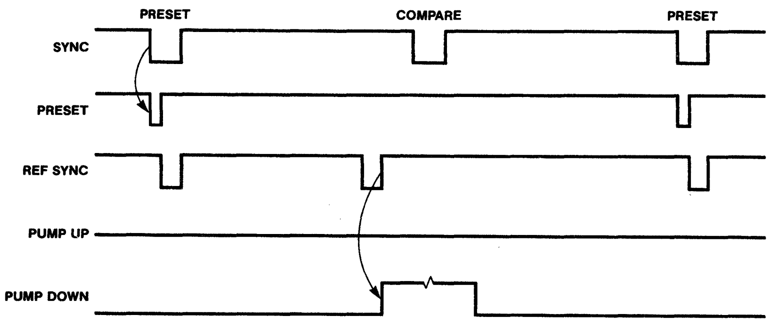


Figure 5 VCO Fast/Slow Timing Diagram



VCO SLOW



VCO FAST

Figure 6 Magnetized Pattern of Quadrature Di-Bit Servo Signal and Read Signal

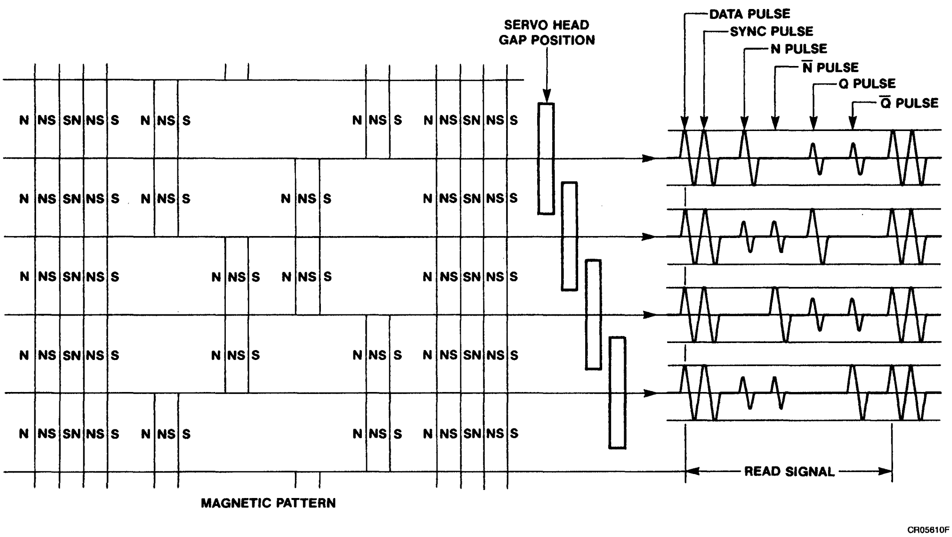


Figure 7 Position Pulse

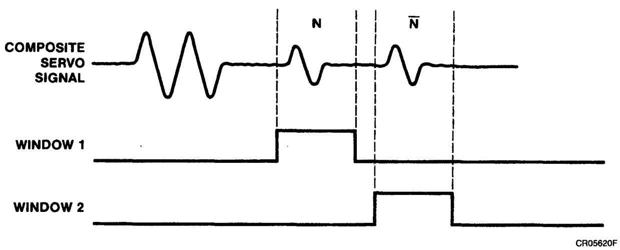
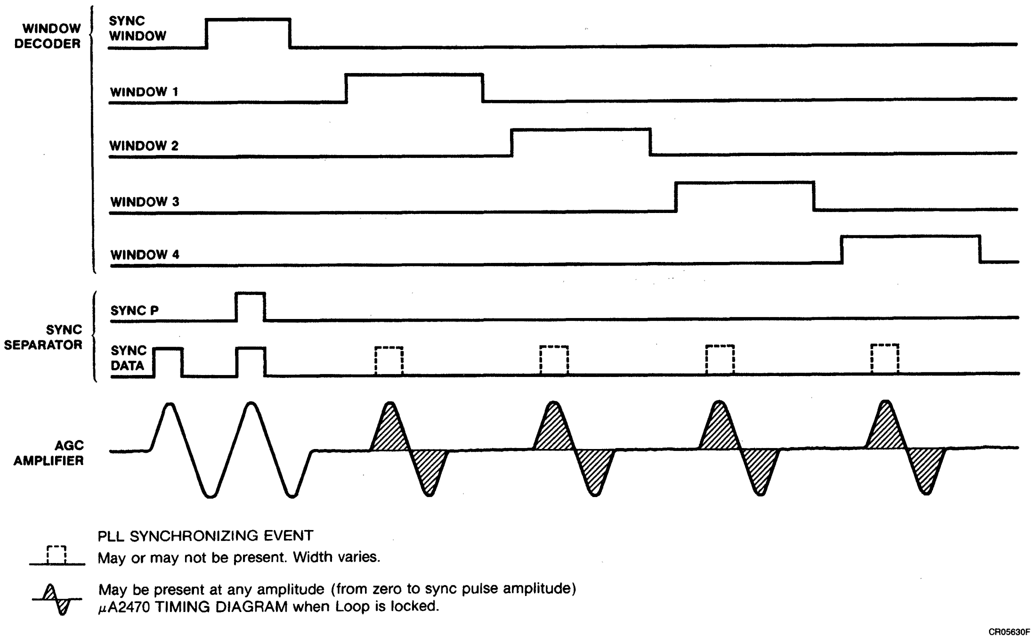


Figure 8 PLL Synchronizing Event



μA2470

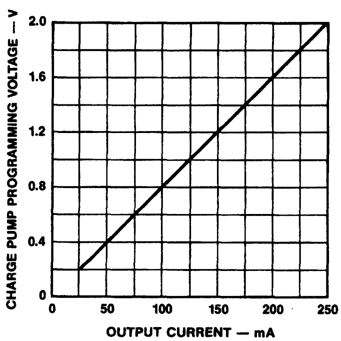
Electrical Characteristics $T_A = 25°C$, $V_{CC2} = 12$ V, $V_{CC1} = 5.0$ V, unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Units
AGC Amplifier					
Max Voltage Gain	Input Freq = 1.0 MHz		46		dB
AGC Range	Input Freq = 1.0 MHz		40		dB
Frequency Response			15		MHz
Input Voltage Range		30		300	mV
Output Voltage			5.0		V_{p-p}
N and Q Outputs					
Output Voltage	$R_L = 20K$		5.0		V_{p-p}
Output Impedance			100		Ω
Output Offset Voltage			20		mV
Voltage Reference					
Output Voltage		4.8	5.0	5.2	V
Output Current				5.0	mA

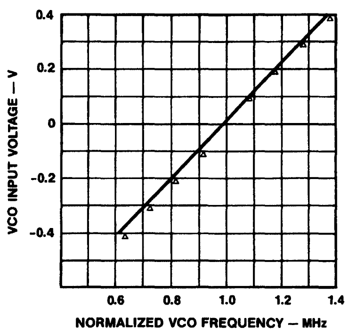
μA2470 (Cont.)
Electrical Characteristics T_A = 25°C, V_{CC2} = 12 V, V_{CC1} = 5.0 V, unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Units
VCO					
Max Frequency	C_{VCO} = 20 pF		20		MHz
Tuning Range		−60		+140	%
Digital Outputs	(R pull-up = 2.0K to V_{CC})				
V_{OL}			0.4		V
Rise Time	0.8 to 2.4 V		20		ns
Fall Time	2.4 to 0.8 V		5.0		ns
Supply Current					
V_{cc1}			140		mA
V_{cc2}			12		mA

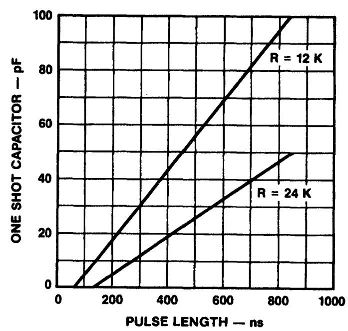
Program Voltage vs Charge Pump Current



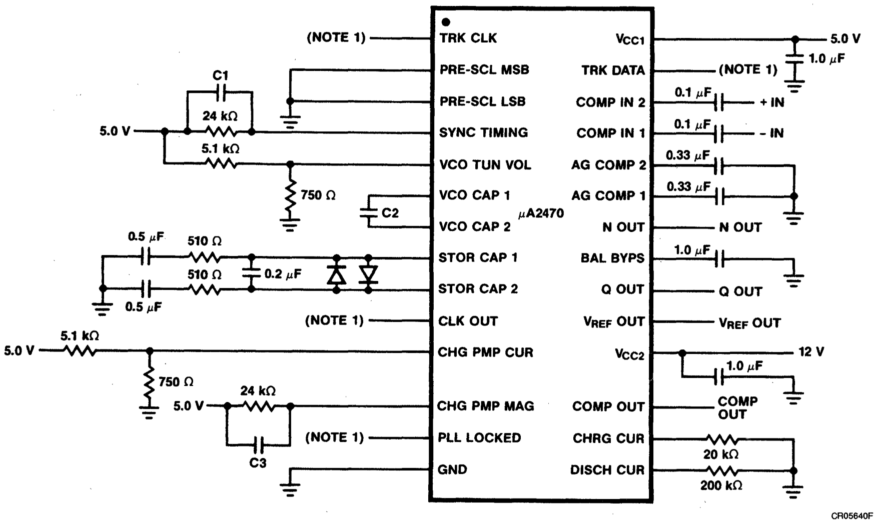
Control Voltage vs VCO Frequency



Capicator Value vs Sync Pulse Demodulator And Charge Pump Oneshot Pulse Length



Test Circuit (Note 2)



Notes
1. Open collector digital outputs
2. C1 = 33 pF
   C2 = 100 pF
   C3 = 15 pF
   Values are for a frame frequency of 150 kHz.
   Scale linearly for other frame notes.

FAIRCHILD

A Schlumberger Company

μA248X • μA248XR Series Winchester Disk Read/Write Preamplifiers

Linear Division Disk Drives

Description

The μA248X/μA248XR Series High Performance Read/Write Preamplifiers are intended for use in Winchester disk drives which employ center tapped ferrite or manganese-zinc read/write heads. The circuit can interface with up to eight read/write heads which makes it ideal for multi-platter disk drive designs. Designed to reside in the Head/Disk Assembly (HDA) of Winchester disk drives, the Read/Write Preamplifiers provide termination, gain, and output buffering for the disk heads as well as switched write current. Certain write fault conditions are detected and reported to protect recording integrity. The parts are available with internal damping resistor (μA248XR) and without internal damping resistor. (μA248X)

- **Wide Bandwidth, High Gain, Low Noise**
- **Up To Eight Read/Write Channels**
- **Internal Write Fault Condition Detection**
- **5.0 V & 12 V Power Supply Voltages**
- **Independent Read & Write Data Lines**
- **TTL Control And Data Logic Levels**
- **Externally Programmable Write Current**
- **Available With Internal Damping Resistor**
- **Compatible With SSI 117 Family**

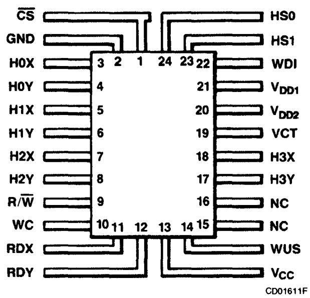
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic	-65°C to +175°C
Plastic	-65°C to +150°C
Operating Junction Temperature Range	25°C to 135°C
Lead Temperature	
Ceramic (soldering, 60 s)	300°C
Plastic (soldering, 10 s)	265°C
Internal Power Dissipation,[1, 2]	
28L-Ceramic DIP	2.50 W
24L-Ceramic DIP	1.95 W
18L-Ceramic DIP	1.58 W
32L-Brazed Flatpak	1.88 W
24L-Brazed Flatpak	0.97 W
24L-Ceramic Flatpak	0.90 W
44L-PLCC	1.92 W
28L-PLCC	1.39 W
Supply Voltage, V_{CC1}	6.0 V
Supply Voltage, V_{CC2}	15 V
Write Current (IWC)	70 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Plastic, and 175°C for the Ceramic.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C the 24L-Ceramic DIP at 13 mW/°C, the 18L-Ceramic DIP at 10.5 mW/°C, the 32L-Brazed Flatpak at 12.5 mW/°C, the 24L-Brazed Flatpack at 6.5 mW/°C, the 24L Ceramic Flatpak at 6.0 mW/°C, the 44L-PLCC at 15.3 mW/°C, and the 28L-PLCC at 11.2 mW/°C.

Connection Diagram 24-Lead Flatpak (Top View)



Order Information

Device Code	Package Code	Package Description
μA2484GC	FR	Brazed Flatpak
μA2484RGC	FR	Brazed Flatpak

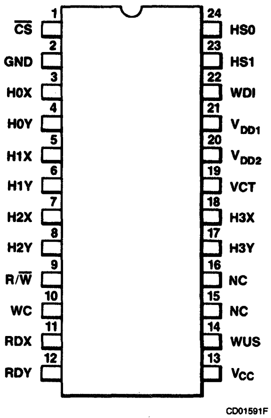
Input Voltages

Head Select (HS0, HS1, HS2)	−0.4 V to V_{CC1} +0.3 V
Write Current (WC) Voltage in read and idle modes. (Write mode must be current limited to −70 mA)	−0.3 V to V_{CC1} +0.3 V
Chip Select (CS)	−0.4 V to V_{CC1} +0.3 V
Read/Write (R/W)	−0.4 V to V_{CC1} +0.3 V

Part Selection

Device Code	Channels
μA2482X	2
μA2484X	4
μA2485X	5
μA2486X	6
μA2488X	8

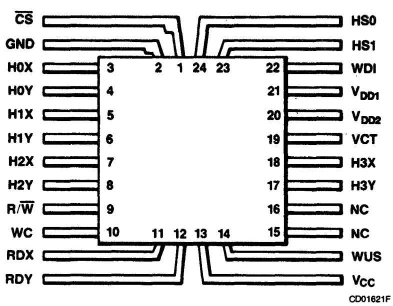
Connection Diagram
24-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2484DC	7L	Ceramic DIP
μA2484RDC	7L	Ceramic DIP

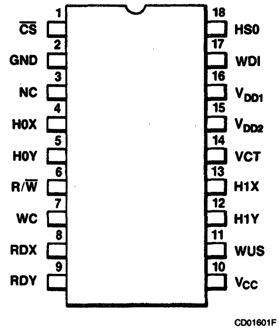
Connection Diagram
24-Lead Cerpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2484FC	FN	Ceramic Flatpak
μA2484RFC	FN	Ceramic Flatpak

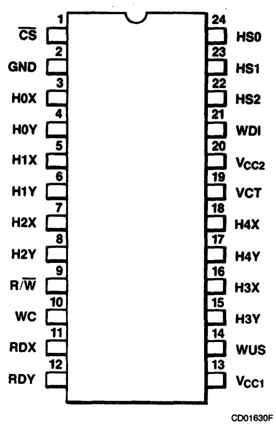
Connection Diagram
18-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2482DC	FU	Ceramic DIP
μA2482RDC	FU	Ceramic DIP

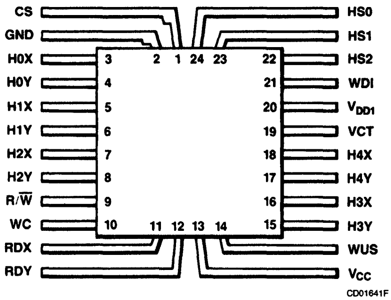
Connection Diagram
24-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485DC	7L	Ceramic DIP
μA2485RDC	7L	Ceramic DIP

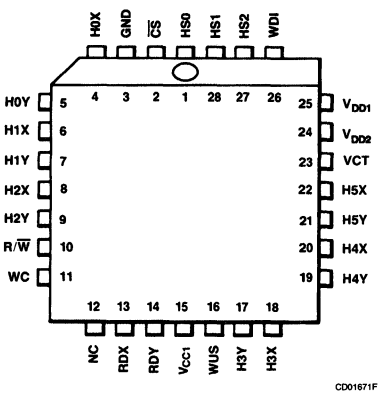
Connection Diagram
24-Lead Cerpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485FC	FN	Ceramic Flatpak
μA2485RFC	FN	Ceramic Flatpak

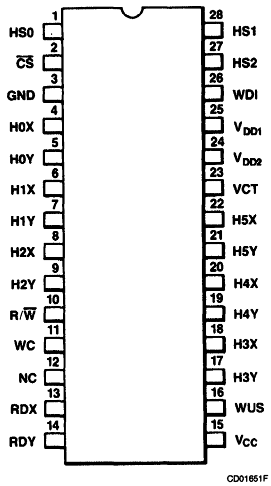
Connection Diagram
28-Lead PLCC (Top View)



Order Information

Device Code	Package Code	Package Description
μA2486QC	KH	Plastic Leaded Chip Carrier
μA2486RQC	KH	Plastic Leaded Chip Carrier

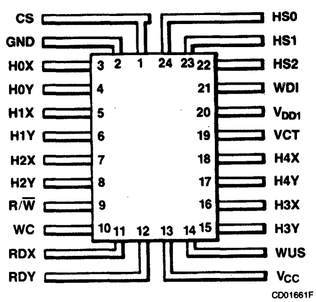
Connection Diagram
28-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2486DC	FM	Ceramic DIP
μA2486RDC	FM	Ceramic DIP

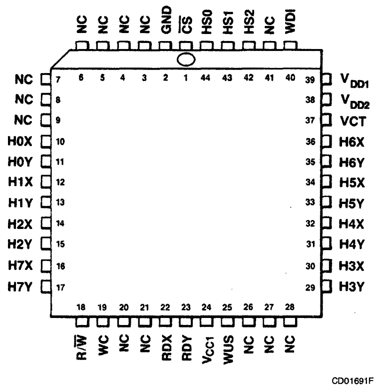
Connection Diagram
24-Lead Flatpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485GC	FR	Brazed Flatpak
μA2485RGC	FR	Brazed Flatpak

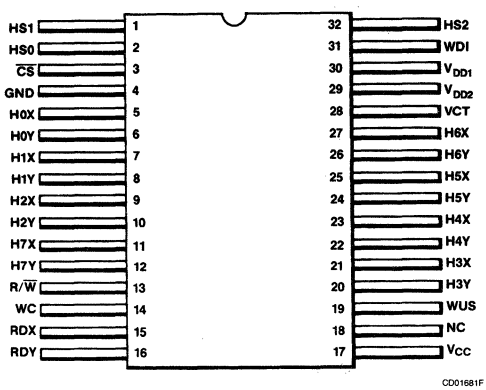
Connection Diagram
44-Lead PLCC (Top View)



Order Information

Device Code	Package Code	Package Description
μA2488QC	KI	Plastic Leaded Chip Carrier
μA2488RQC	KI	Plastic Leaded Chip Carrier

Connection Diagram
32-Lead Flatpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2488GC	FS	Brazed Flatpak
μA2488RGC	FS	Brazed Flatpak

Functional Description

In the Write mode, the μA248X/μA248XR Series accepts TTL compatible write data pulses on the WDI lead. On the falling edge of each write data pulse, a current transition is made in the selected head. Head selection is accomplished via TTL input signals: HS0, HS1, HS2 (*see Table 2*). Internal circuitry senses the following conditions:

1. Absence of data transitions.
2. Open circuit head connection.
3. Absence of write current.
4. Short circuit head connection.
5. Idle or read mode.

Any or all of the above conditions would result in a high level on the write unsafe (WUS) output signal.

During read operations, the μA284X amplifies the differential voltages appearing across the selected R/W head lead and applies the amplified signal differentially to data lines RDX and RDY.

Description of Lead Functions

Lead	Name	Description of Functions
$\overline{CS}$	Chip Select	Chip Select High disables the read/write function of the device and forces idle mode. (TTL)
R/$\overline{W}$	Read/Write Select	A Logic High places the devices in read mode and a Logic Low forces write mode. *Refer to Table 1.* (TTL)
H0X, Y through H7X, Y	Read/Write Head Connections	The μA2488 has eight pairs of read/write connections. The X and Y phases are made consistent with the read output, RDX and RDY, phases. (Differential)
RDX, Y	Read Data Outputs	The chip has one pair of read data outputs which is multiplexed to the appropriate head connections. (Differential)
HS0 through HS2	Head Select Inputs	The eight read/write heads are addressed with the head select inputs. *Refer to Table 2.* (TTL)
WC	Write Current Input	This lead sets the current level for the write mode. An external resistor is connected from this lead to ground, and write current is determined by the value of this resistor divided into the write current constant K, which is typically 140 V.
WDI	Write Data Input	The write data input toggles the write current between the X and Y selected head connections. Write current is switched on the negative edge of WDI. The initial direction for write current is the X side of the switch and is set upon entering read or idle mode. (TTL)
V_{DD2}	Resistor Center Tap	In some versions (determined by lead availability) of the μA248X series, a resistor may be connected between RCT and V_{DD1} to reduce internal power dissipation. If this resistor is not used, RCT must be connected externally to V_{DD1}.
VCT	Center Tap Voltage	The center tap output provides bias voltage for the head inputs in read and write mode. It should be connected to the center tap of the read/write heads.
WUS	Write Unsafe	A high logic level at the write unsafe output indicates a fault condition during write. Write unsafe will also be high during read and idle mode. (Open collector)

Table 1 Read/Write Select

Operating Modes

Chip Select $\overline{CS}$	Read/Write R/$\overline{W}$	Mode
1	X	Idle
0	1	Read
0	0	Write

Table 2 Head Select Inputs

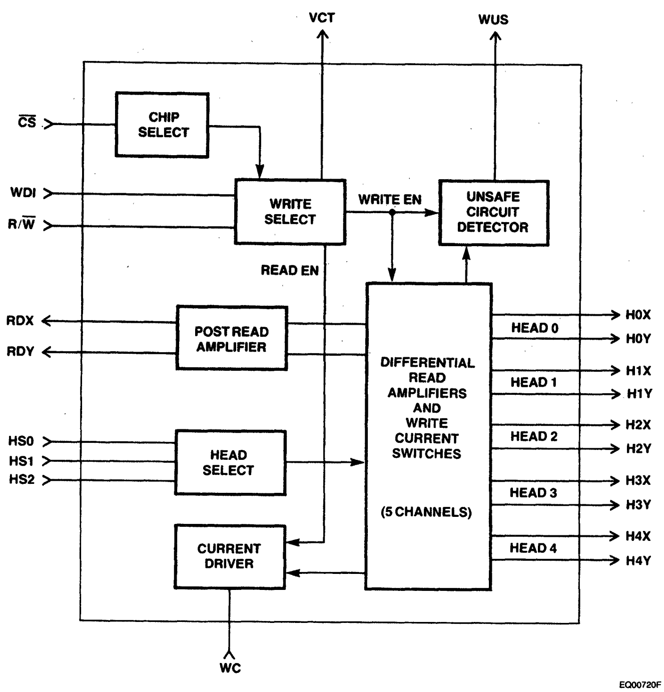
Head Selection

HS0	HS1	HS2	Head Selected[1]
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Note

1. If selected head is beyond the capacity of the μA248X model, the open input condition on the selected input will be reported as an unsafe level at the WUS output.

Block Diagram (Typical, μA248X)



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Absolute Maximum Ratings All voltages referenced to GND

Symbol	Characteristic		Value	Unit
V_{DD1}	DC Supply Voltage		−0.3 to +14	V
V_{DD2}			−0.3 to +14	V
V_{CC}			−0.3 to +6.0	V
V_{in}	Digital Input Voltage Range		−0.3 to V_{CC} +0.3	V
V_H	Head Port Voltage Range		−0.3 to V_{DD} +0.3	V
V_{wus}	WUS Port Voltage Range		−0.3 to +14	V
I_W	Write Current		60	mA
I_O	Output Current	RDX, RDY	−10	mA
		VCT	−60	
		WUS	+12	

Recommended Operating Conditions

Symbol	Characteristic	Value	Unit
V_{DD1}	DC Supply Voltage	12 ±10%	V
V_{DD2}		6.5 to V_{DD1}	V
V_{CC}		5.0 ±10%	V
Lh	Head Inductance	5.0 to 15	μH
RD	Damping Resistor (External)	500 to 2000	Ω
RCT	RCT Resistor	90 ±5.0% (½ watt)	Ω
I_W	Write Current	25 to 50	mA
I_O	RDX, RDY Output Current	0 to 100	μA

DC Characteristics $25°C \leq T_J \leq 125°C$ $V_{DD1} = 12$ V, $V_{CC} = 5.0$ V, unless otherwise specified.

Symbol	Characteristic		Condition		Min	Max	Unit
I_{CC}	Supply Current		Read/Idle Mode			25	mA
			Write Mode			30	
I_{DD}	Supply Current		Idle Mode			25	mA
			Read Mode			50	
			Write Mode			$30 + I_W$	
P_C	Power Consumption		$T_J = 125°C$	Idle Mode		400	mW
				Read Mode		600	
				Write Mode, $I_W = 50$ mA, RCT = 90 Ω		850	
				Write Mode, $I_W = 50$ mA, RCT = 0 Ω		1050	
V_{IL}	Digital Inputs:	Input Voltage LOW			−0.3	0.8	V
V_{IH}		Input Voltage HIGH			2.0	$V_{CC} + 0.3$	V
I_{IL}		Input Current LOW	$V_{IL} = 0.8$ V		−0.4		mA
I_{IH}		Input Current HIGH	$V_{IH} = 2.0$ V			100	μA
V_{OL}	WUS Output		$I_{OL} = 8.0$ mA			0.5	V
I_{OH}			$V_{OH} = 5.0$ V			100	μA
V_{CT}	Center Tap Voltage		Read Mode		4.0 (typ)		V
			Write Mode		6.0 (typ)		V

Write Characteristics $V_{DD1} = 12$ V, $V_{CC} = 5.0$, $I_W = 45$ mA, Lh = 10 μH, f(Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, $R_{D\ EXT} = 750$ Ω or $R_{D\ INT}$, unless otherwise specified.

Characteristic	Condition	Min	Max	Unit
Write Current Range		10	50	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7		V (pk)
Unselected Diff. Head Current			2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10K		Ω
	With Internal Resistors	538	1.0K	
WDI Transition Frequency	WUS = LOW	400 (typ)		kHz
I_{wc} to Head Current Gain		18 (typ)		mA/mA

5

Read Characteristics V_{DD1} = 12 V, V_{CC} = 5.0 V, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ⩽ 20 pF, (V_{in} is referenced to V_{CT}), $R_{D\ EXT}$ = 750 Ω or $R_{D\ INT}$, unless otherwise specified.

Characteristic	Condition		Min	Max	Unit
Differential Voltage Gain	V_{in} = 1.0 mV_{p-p} at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ		80	120	V/V
Dynamic Range	Input Voltage, V_I, Where Gain Falls by 10%. V_{in} = V_I + 0.5 mV_{p-p} at 300 kHz		-2.0	+2.0	mV
Bandwidth (-3db)	I Zs I < 5.0 Ω, V_{in} = 1.0 mV_{p-p}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			2.1	nV/$\sqrt{Hz}$
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz	Without Internal Resistors	2K		Ω
		With Internal Resistors	440	850	
Input Bias Current				45	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{p-p} at 5.0 MHz		50		db
Power Supply Rejection Ratio	100 mV_{p-p} at 5.0 MHz on V_{DD1}, V_{DD2}, or V_{CC}		45		db
Channel Separation	Unselected Channels: V_{in} = 100 mV_{p-p} at 5.0 MHz and Selected Channel: V_{in} = 0 mV_{p-p}		45		db
Output Offset Voltage			-480	+480	mV
Common Mode Output Voltage			5.0	7.0	V
Single Ended Output Resistance	f = 5.0 MHz			35	Ω
Internal Damping Resistor			560	1070	Ω

Switching Characteristics V_{DD1} = 12 V, V_{CC} = 5.0 V, T_J = 25°C, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, $R_{D\ EXT}$ = 750 Ω or $R_{D\ INT}$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		1.0	μs
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz Read Signal Envelope or to 90% Decay of Write Current		1.0	
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV 10 MHz Read Signal Envelope		1.0	μs
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		1.0	
HS0 HS1 HS2	to any Head	Delay to 90% of 100 mV to 10 MHz Read Signal Envelope		1.0	μs
WUS	Safe to Unsafe — TD1	I_W = 50 mA	1.6	8.0	μs
	Unsafe to Safe — TD2	I_W = 20 mA		1.0	
Head Current	Prop. Delay - TD3, TD4	Lh = 0 μH, Rh = 0 Ω From 50% Points		25	nS
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time		2	
	Rise/Fall Time	10% - 90% Points		20	

Figure 1 Head Current Timing

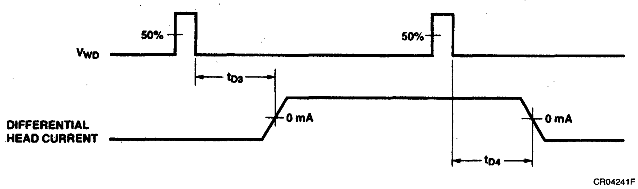


Figure 2a Unsafe to Safe Timing

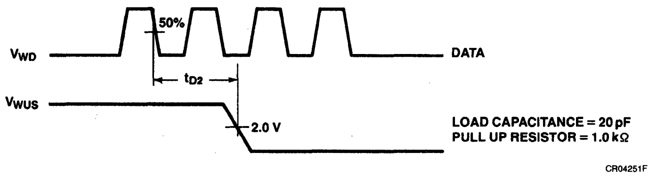
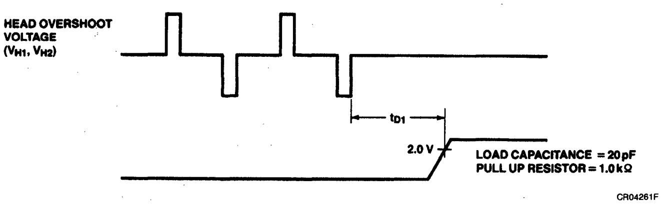


Figure 2b Safe to Unsafe Timing



FAIRCHILD

A Schlumberger Company

μA2480 Winchester Disk Servo Preamplifier

Linear Division Disk Drives

Description

The μA2480 provides termination, gain, and impedance buffering for the servo read head in Winchester disk drives. It is a differential input, differential output design with fixed gain of approximately 100. The bandwidth is guaranteed greater than 10 MHz.

The internal design of the μA2480 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-lead DIP (plastic) or 10-lead flatpak.

- **Low Input Noise Voltage**
- **Wide Power Supply Range (8.0 V To 13 V)**
- **Internal Damping Resistors (1.0 kΩ)**
- **Functionally Compatible with SSI 101**

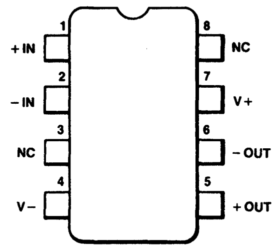
Absolute Maximum Ratings

Storage Temperature Range	
Flatpak	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Flatpak (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Molded DIP	0.93 W
10L-Flatpak	0.79 W
Supply Voltage	15 V
Output Voltage	15 V
Differential Input Voltage	±1.0 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Flatpak.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Flatpak at 5.3 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.

Connection Diagram
8-Lead DIP
(Top View)



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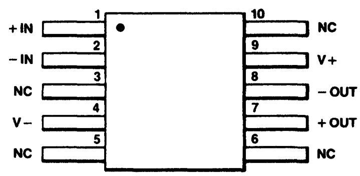
Order Information

Device Code	Package Code	Package Description
μA2480TC	9T	Molded DIP

Connection Diagram
10-Lead Flatpak
(Top View)



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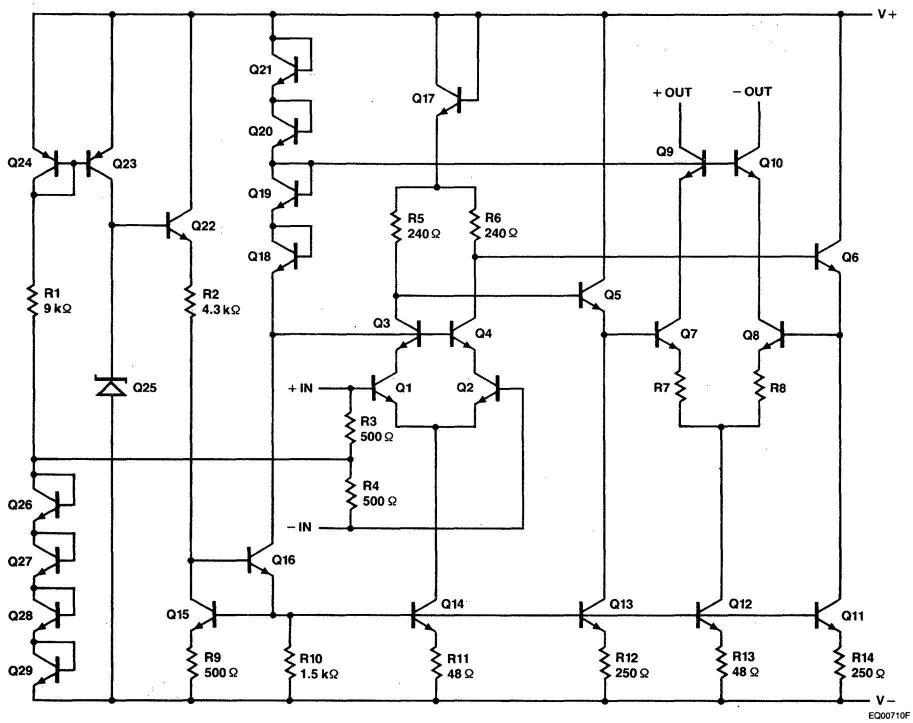
Order Information

Device Code	Package Code	Package Description
μA2480FC	3F	Flatpak

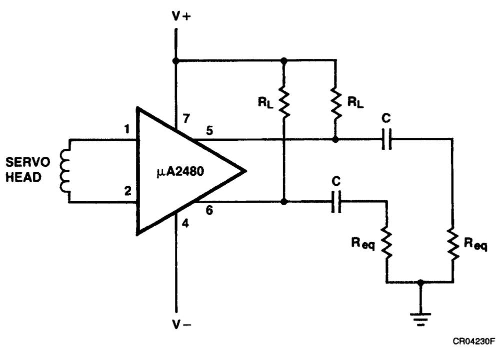
Equivalent Circuit



Electrical Characteristics $T_A = 25°C$, $(V+) - (V-) = 8.0$ V to 13.2 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
G	Gain (differential)	$R_p = 130\ \Omega$, $V_{CC} = 12$ V	92	115	138	
		$R_p = 130\ \Omega$, $V_{CC} = 12$ V, $T_A = 0°C$ to $70°C$	80		150	
BW	Bandwidth (3.0 dB)	$V_I = 2.0\ mV_{p-p}$	10	30		MHz
R_I	Input Resistance		800	1000	1200	Ω
C_I	Input Capacitance			3.0		pF
V_I	Input Dynamic Range (differential)	$R_p = 130\ \Omega$, $V_{CC} = 12$ V	3.0			mV_{p-p}
I_s	Supply Current	$V_{CC} = 12$ V		30	40	mA
ΔV_O	Output Offset (differential)	$R_s = 0\ \Omega$, $R_p = 130\ \Omega$			600	mV
V_n	Equivalent Input Noise	BW = 4.0 MHz, $R_S = 0\ \Omega$		1.5	10	μV
PSRR	Power Supply Rejection Ratio	$R_s = 0\ \Omega$, f < 5.0 MHz	50	65		dB
$\Delta G/\Delta V$	Gain Sensitivity (Supply)	$\Delta V_{CC} = \pm 10\%$, $R_p = 130\ \Omega$		±1.3		%/V
$\Delta G/\Delta T$	Gain Sensitivity (Temp)	$T_A = 25°C$ to $70°C$, $R_p = 130\ \Omega$		-0.2		%/°C
CMR	Common Mode Rejection (Input)	f < 5.0 MHz	55	70		dB

Typical Applications



Notes
1. Leads shown for 8-lead DIP.
2. R_{eq} is equivalent load resistance.
3. $R_P = \dfrac{R_L \cdot R_{eq}}{R_L + R_{eq}}$
4. $G = .88\ R_P$
   Where R_P = value from Note 3 (above) in ohms.

FAIRCHILD

A Schlumberger Company

μA2490 MFM/2,7 Data Separator/ Encoder-Decoder

Linear Division Disk Drives

Description

The μA2490 Data Separator/Encoder-Decoder chip provides a convenient, high performance means of converting MFM or 2,7 encoded data derived from magnetic media to an NRZ digital bit stream. Also included is an MFM or 2,7 encoder which converts NRZ data to MFM or 2,7 encoded serial formal suitable for recording on magnetic media. The μA2490 provides both MFM and 2,7 modes of operation selectable with a select pen.

The Data Separator chip provides the complete oscillator synchronization and data decode function required on controllers in the ST506 format, and disk drives in the ESDI format. The chip also allows selectable precompensation for those drives that may require it.

- **Data Rates To 25 Mbps**
- **ESDI And ST506 Compatible Signal Definitions**
- **Can Be Used In Drive Or Controller**
- **Selectable MFM Or 2,7 Encoding/Decoding**
- **Internal Generation/Detection Of MFM And 2,7 Address Marks**
- **Internal Write Precompensation With Externally Programmed Value**

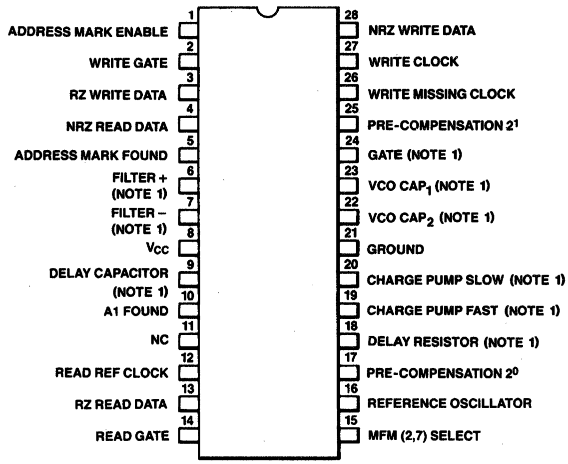
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
PLCC	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
PLCC (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
28L-Ceramic DIP	2.50 W
44L-PLCC	1.92 W
Supply Voltage	6.0 V
TTL Inputs	6.0 V
Output Voltage	6.0 V

Notes

1. $T_{J\ Max}$ = 150°C for the PLCC, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the Ceramic DIP at 16.7 mW/°C, and the PLCC at 15.3 mW/°C.

Connection Diagram
28-Lead DIP
(Top View)



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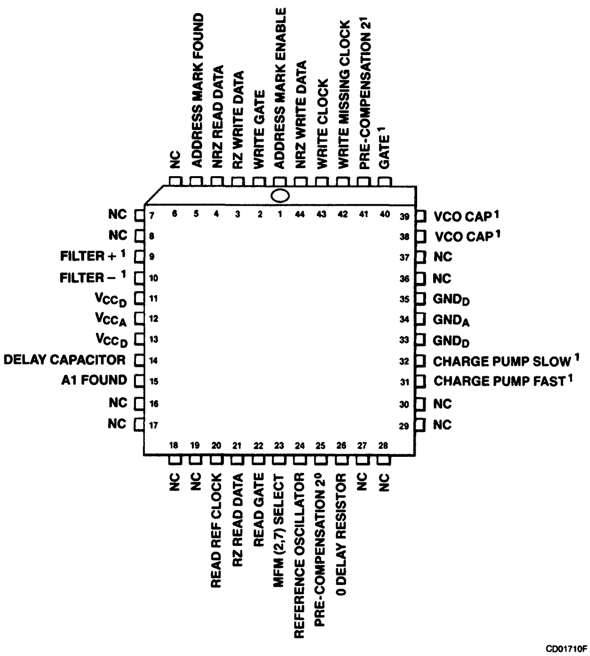
Note

1. Passive compensation node.

Order Information

Device Code	Package Code	Package Description
μA2490DC	FM	Ceramic DIP

Connection Diagram
44-Lead PLCC
(Top View)



Note
1. Passive compensation node.

Order Information

Device Code	Package Code	Package Description
μA2490QC	KI	Plastic Leaded Chip Carrier

Description of Lead Functions

Name	Description of Functions
Input Leads — All inputs are TTL	
Address Mark Enable	This lead has two functions depending on the state of the WRITE GATE input lead. If ADDRESS MARK ENABLE is enabled (LOW) and WRITE GATE IS DISABLED (HIGH), then the μA2490 will go into an address mark search mode. The address mark is the DC erased gap. If ADDRESS MARK ENABLE is enabled (LOW) and WRITE GATE is enabled (LOW), then the μA2490 will not allow the RZ WRITE DATA output to change state. This allows the writing of DC erased gaps (address marks).
Write Gate	When enabled (LOW) this lead will allow the μA2490 to output encoded RZ data on the Write Data lead. Its function is tabulated as shown:

Address Mark Enable	Write Gate	Resultant Function
Enabled (LOW)	Enabled (LOW)	Write DC Erased Gap
Enabled (LOW)	Disabled (HIGH)	Search for DC Erased Gap
Disabled (HIGH)	Enabled (LOW)	Write RZ Data
Disabled (HIGH)	Disabled (HIGH)	Disabled

Name	Description of Functions
RZ Read Data	This lead receives the encoded RZ data pulses from the Read Channel in the disk drive. This input is what the phase lock loop (PLL) locks up to when decoding read data, and is also what will restart the internal VCO clock after READ GATE switches from HIGH to LOW.
Read Gate	When enabled (LOW) this lead will allow the μA2490 to lock up to and read RZ data from the disk. When this lead changes states, the internal VCO clock is turned off. When this lead changes from HIGH to LOW (enabled), the first RZ READ DATA INPUT will restart the internal VCO clock. When this lead changes from LOW to HIGH (disabled), the first REFERENCE OSCILLATOR input pulse will restart the internal VCO clock.
MFM/2,7 Select	This lead allows the user to select the desired code. A TTL low selects MFM and a TTL high selects the 2,7 code.
Reference Oscillator	This is the reference clock input that the μA2490 phase lock loop syncs to when in the write mode and the idle state. This input also restarts the VCO clock after READ GATE switches from LOW to HIGH. The frequency of the reference oscillator should be the same as the data rate. During write, the WRITE CLOCK input must be phase locked to the signal on this lead.
Precompensation 2^0	When this lead is enabled (HIGH) and PRECOMPENSATION 2^1 lead is disabled (LOW), the precompensation value will be 5% of the 2f clock period.
Precompensation 2^1	When this lead is enabled (HIGH) and PRECOMPENSATION 2^0 lead is disabled (LOW), the precompensation value will be 10% of the 2f clock period. If both PRECOMPENSATION 2^0 and PRECOMPENSATION 2^1 leads are enabled (HIGH), the precompensation value will result in a 15% correction of 2f clock period.
Write Missing Clock	This lead receives the signal (active low) from the controller to drop the clock pulse out of bit 6 in the MFM "A1" pattern. This lead should be enabled (LOW) only when the "A1" pattern is present at the NRZ WRITE DATA input.
Write Clock	This lead receives the clock from the controller which clocks the NRZ WRITE DATA (lead 28) input.

Description of Lead Functions (Cont.)

Name	Description of Functions
Input Leads — All inputs are TTL (Cont.)	
NRZ Write Data	This lead receives NRZ data from the controller along with WRITE CLOCK, for encoding and subsequent writing on the disk. Data is valid at the rising edge of WRITE CLOCK. This input assumes "0s" are a TTL low level.
Output Leads — All outputs are TTL	
RZ Write Data	This lead is the RZ write data output to be written on the disk. This output is active low. It is clocked out with the PLL oscillator (which is locked to the REFERENCE OSCILLATOR).
NRZ Read Data	This lead is the NRZ decoded data output to the controller. This output assumes "0s" are a TTL low level. NRZ Read Data is valid at the rising edge of Read/Reference Clock.
Address Mark Found	A negative pulse output on this lead will indicate the presence of a DC erased gap. If the μA2490 is able to count 16 clock intervals without a flux change being sensed from the disk, then a "zero" will be clocked out at the first rising edge of a flux change and will last for one clock period. The address mark signal will occur at the beginning of the sync field since that is usually where the first flux change occurs after the DC gap.
"A1" Found	A negative pulse at this lead indicates that a missing clock has been found in the MFM code. This pulse lasts for one VCO clock period and is associated with the missing clock that was written in the "A1" pattern.
Read/Reference Clock	This lead will output the reference oscillator when READ GATE is disabled (HIGH), or the internal μA2490 clock when READ GATE is enabled (LOW) and 16 consecutive zeros have been decoded (in sync field). This allows the phase lock loop to lock up to the incoming RZ READ DATA before switching the READ/REFERENCE CLOCK output from the REFERENCE OSCILLATOR INPUT to the internal PLL's oscillator.
External Connection Leads	
Filter +	This lead is the output of the charge pump and one of the differential inputs to the VCO. A negative pulse here will increase the VCO frequency.
Filter −	This lead is the output of the charge pump and the other (differential) input to the VCO. A negative pulse here will decrease the VCO frequency.
V_{CC}	This lead is the +5.0 V supply — DIP only.
V_{CCA}	This lead is the +5.0 V supply for analog circuitry — PLCC only.
V_{CCD}	This lead is the +5.0 V supply for digital circuitry — PLCC only.
Delay Capacitor	The external capacitor that sets the delay time of the RZ READ DATA to one half of a clock (VCO) period is attached here. Varying the capacitor value will vary the centering of the incoming data in its phase-error window. The other side of the capacitor should be tied to the +5.0 V supply.
Delay Resistor	An external resistor tied from this lead to GROUND will set the delay time (in conjunction with the capacitor on lead 9) of the internal delay network. A variable resistor can be used to accurately adjust the centering of the phase margin window.

Description of Lead Functions (Cont.)

Name	Description of Functions
External Connection Leads (Cont.)	
Charge Pump Fast	An external resistor from this lead to ground will determine the current that is added to the CHARGE PUMP SLOW current that will be used by the charge pump to drive the filter. This current is switched in, only during the sync fields, to decrease the sync-up time of the phase lock loop. It is turned off when 16 consecutive zeros have been decoded in the sync field, indicating a proper phase lock to data.
Charge Pump Slow	An external resistor from this lead to ground sets the operating current in the Charge Pump for normal data reading. This current is always ON. The CHARGE PUMP FAST and CHARGE PUMP SLOW current values are selected in conjunction with the FILTER + and FILTER – component values to insure proper stability of the phase lock loop during its operation.
Ground	This lead is the GROUND return for the chip — DIP only.
Ground A	This lead is the GROUND return for the analog circuit on the chip — PLCC only.
Ground D	This lead is the GROUND return for the digital circuit on the chip — PLCC only.
VCO Cap 1	One side of the VCO frequency-setting capacitor connects to this lead. A negative sloping transition on this lead corresponds to an "up" level of the VCO clock. The other side of the capacitor connects to lead 23.
VCO Cap 2	One side of the VCO frequency-setting capacitor connects to this lead. A negative sloping transition on this lead corresponds to an "up" level of the VCO clock. The other side of the capacitor connects to VCO CAP 1 lead. This lead can be connected to GATE lead if an in-phase start up is desired during the sync-up mode.
Gate	This lead can be tied to the adjacent VCO CAP 2 lead for an in-phase start up of the VCO. The internal CLOCK GENERATOR (see block description) will always turn off the internal VCO clock when the READ GATE changes state. The VCO will continue to free-run unless this lead is connected to VCO CAP 2 lead. The in-phase start up can be used in those situations where a servo clock is available for accurate frequency prediction of the anticipated incoming RZ READ DATA stream.

Detailed Block Description

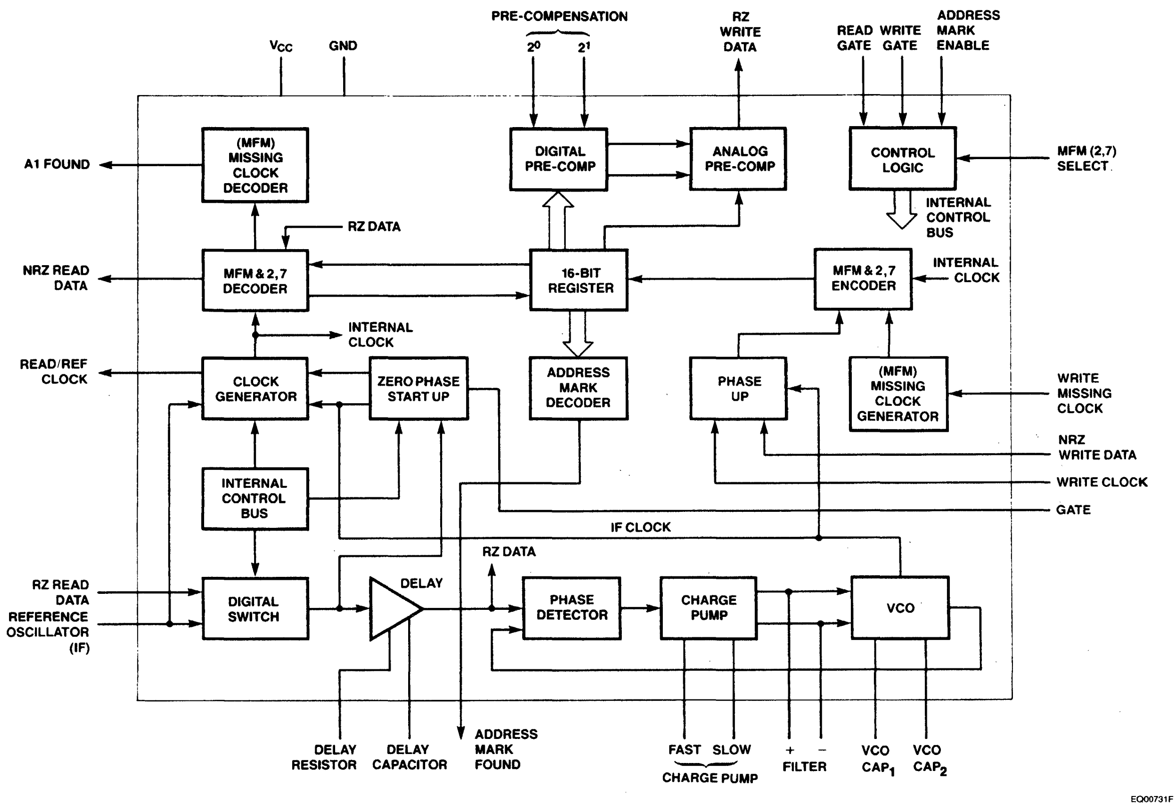
The following description gives a brief outline of the blocks contained in the block diagram of the μA2490 Data Separator. *See Figure 1.*

SWITCH — Connects either incoming read data (from the disk drive read electronics) or a reference oscillator to the phase lock loop for synchronizing the phase lock loop's oscillator (VCO). When not reading data the SWITCH block connects the reference oscillator to the PLO's input.

PHASE DETECTOR — Has two modes of operation — harmonic for read mode and non-harmonic for write and idle mode. In the harmonic mode, the phase detector is enabled by the rising edge of the incoming pulse. In the non-harmonic mode, the phase detector is constantly enabled. The phase detector generates pulses to control the CHARGE PUMP. The pulse width will correspond to the phase error between the occurrence of an incoming pulse (from the SWITCH block) and the phase lock loop's oscillator (VCO). One output will control charge-up current to the filter and the other output will control the discharge current to the filter.

SINGLE SHOT DELAY — Provides a delay to allow the phase detector to set up for a phase comparison between incoming pulses and the phase lock loop's oscillator. The timing of this delay should be one half the VCO's clock period (quarter of the data rate) to assure a properly centered pulse in the Phase Lock Window. This delay circuit has absolutely no effect on the Data Window and the Data pulse phase relationships. The rising edges of the Delayed Data pulse and the VCO clock pulse are inherently in phase at the phase detector input, no matter how much the delay circuit is delaying the data. Since the Data Window is set by inverting the VCO clock waveform, the

Figure 1 Block Diagram



Delayed Data input will always be centered in the Data Window.

CHARGE PUMP — Provides either a charging or discharging current, as directed by the phase comparator, to the externally connected loop filter. The value of the current is internally switched between CHARGE PUMP FAST (a high current) and CHARGE PUMP SLOW (a low current). The higher current is used in the "sync-up" mode during the reading of sync-fields, and the lower current is used during reading data or ID fields.

VCO — The Voltage Controlled Oscillator generates a continuous stream of clock pulses at a frequency rate that is determined by the input voltage provided from the charge-pump/filter combination, and an externally connected capacitor. The VCO output is continually being phase compared to the pulse stream selected by the SWITCH block. The input controlling voltage to the VCO is caused to vary in such a way as to maintain phase lock with the input pulses.

CLOCK GENERATOR — Provides the output of the VCO to the rest of the chip. The output of the CLOCK GENERATOR switches off at a change of state of the READ GATE input, and turns back on at the first occurrence of the RZ READ DATA (if READ GATE is enabled), or the REFERENCE OSCILLATOR (if READ GATE is disabled). The GATE lead can be tied to the VCO CAP lead to start the VCO in-phase with incoming RZ DATA or REFERENCE OSCILLATOR.

ZERO PHASE START UP — This block turns off all internal clocks whenever the READ GATE input changes state, and also toggles the GATE lead. This lead can be tied to one of the VCO capacitor leads to turn off the VCO at the same time. The first incoming bit that is to be fed into the phase lock oscillator (RZ READ DATA for READ GATE enabled, the REFERENCE OSCILLATOR for READ GATE disabled) will disable the gate function and allow the VCO to start in-phase with the incoming data, and will enable all internal clocks. This provides the capability for an in-phase start up for PLL. *See Figure 2.*

CONTROL LOGIC — Decodes the input control lines from the controller to provide internal control signals to the μA2490. It indicates to the rest of the chip when reading or writing is being requested, and whether the MFM or 2,7 code is being used. During WRITE, it also presets the encoders to an encoded zero pattern.

READ/WRITE CONTROL — This block controls the switching of the μA2490 between READ and WRITE modes of operation.

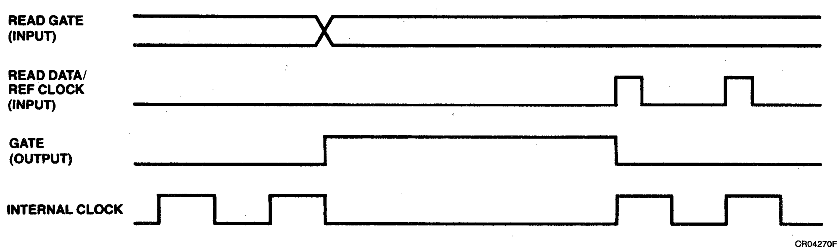
MFM & 2,7 ENCODER — This block is controlled by the MFM/2,7 select lead. The MFM/2,7 select input will cause incoming WRITE DATA IN to be encoded into either MFM format or 2,7 format before it is clocked out as NRZ WRITE DATA.

16 BIT REGISTER — The incoming data stream for both read and write functions is shifted into this register for processing purposes. During sync-up time this register is used to count the number of incoming zeros to insure proper synchronization to the RZ READ DATA. During WRITE this register is used to enable precompensation time-shifts at the appropriate time in the write data stream. DC erased gaps in the RZ READ DATA stream are also detected by using this shift register.

ADDRESS MARK DECODE — During read mode, when address mark enable is active this block finds DC erased gaps in the incoming bit-stream that are at least 16 bits wide. A signal is sent to the controller to indicate a gap has been found (ADDRESS MARK FOUND).

MISSING CLOCK DECODER (MFM) — Immediately following the sync-field in an MFM encoded bit stream there is a pattern written that is not allowed in the MFM encode process. The byte written is generally "A1," and the CLOCK transition that should have occurred on the sixth bit is not written. On read-back this missing CLOCK bit is

Figure 2 In-Phase Start up Timing for GATE Output Tied to Lead 23 (VCO CAP)



detected by the Missing Clock Decoder and a pulse is generated. This pulse is used for timing alignment in the controller.

PHASE UP — This block lines up the μA2490's clock with the WRITE CLOCK input to assure proper phasing to clock out the WRITE DATA. The WRITE CLOCK input must be synchronized with the REFERENCE OSCILLATOR.

MFM & 2,7 DECODER — Translates the encoded RZ READ DATA into decoded NRZ DATA OUT before sending it on to the controller. The CONTROL LOGIC block will determine if the MFM decode or 2,7 decode algorithm is to be used.

MISSING CLOCK GENERATOR (MFM) — In MFM mode, this block allows the CLOCK transition in the 6th bit of the ID byte "A1" to be stripped out before being sent out as write data to the disk. This block is controlled by the controller.

DIGITAL PRECOMP — Four values of precompensation delays can be selected through two digital inputs. The precompensation written is dependent on the bit position in the write data stream. Its purpose is to cause a bit to be written early or late to offset the effects of bit-crowding (peak shifting) of closely spaced flux transitions on the disk. The four values of precompensation allowed are selectable between 0%, 5%, 10% and 15% of the VCO clock period.

ANALOG PRE-COMP — Works with the Digital Precomp block to actually inject the early or late write-time for a given WRITE DATA transition.

Functional Description

The μA2490 can reside in either the disk controller or the drive itself. When it resides in the controller, the interface signals are compatible with the industry standard ST506 signals and levels. When utilized within the drive, the interface becomes compatible with ESDI (Enhanced Small Disk Interface) the proposed industry standard for higher capacity drive.

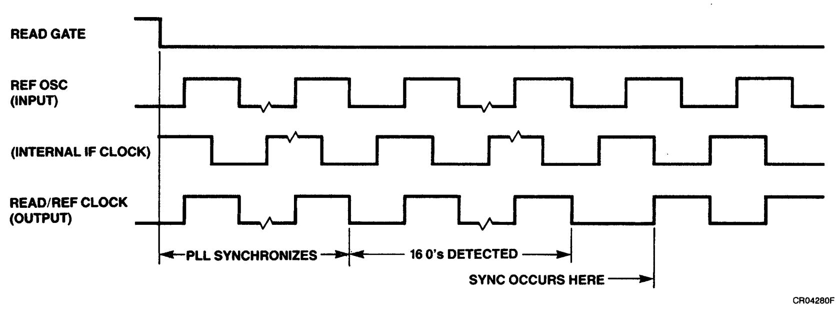
Operation of the μA2490 is dependent on the format in which the sectors of the disk are written. The principal requirement is the provision of an adequately long synchronization field prior to valid data. For the μA2490, this field must contain an all "zeros" (NRZ) data pattern for a minimum of 32 data bit intervals (NRZ) between assertion of READ GATE and the beginning of valid data (including address marks). Such a format as is suggested in the ST506 interface specifications is suitable. With the exception of the provision for leading "address marks," the format suggested in ESDI interface documents is also suitable.

Read

When not writing, the internal PLL remains phase and frequency locked to the REFERENCE OSCILLATOR input until the READ GATE input is asserted by the controller. When ADDRESS MARK enable is asserted without asserting READ GATE or WRITE GATE, the μA2490 looks for the DC erased gap which should be at least 16 bits long. After detecting 16 bits of DC erased gap, a pulse appears at ADDRESS MARK FOUND lead at the first flux transition on the READ DATA lead. This pulse disappears with the arrival of the second pulse on the READ DATA lead. It is assumed, that this flux transition is the first bit of the encoded zero sync-field. ADDRESS MARK ENABLE should be disabled at this point and READ GATE should be asserted. ADDRESS MARK ENABLE and READ GATE should not be asserted at the same time.

As discussed before, assertion of READ GATE is presumed to occur during the PLO sync portion of the track format. At the assertion of READ GATE, the PLL changes to phase lock mode. It enters a "fast acquisition" mode

Figure 3 READ/REF Clock Output Timing During Read Sync-up at the Time 16 Zeros Have Been Decoded in the Preamble Sync Field.



and attempts to lock on to the incoming MFM (or 2,7) RZ READ DATA pulses using pattern sensitive phase discrimination and fast loop dynamics. The μA2490 makes the important assumption that the pattern written in this field represents encoded zero data bits.

When lock is achieved and 16 successive zero data bits have been decoded, the internal PLL switches to "slow track" mode in preparation for encountering the unique address mark byte. NRZ READ DATA OUT lead (which was high until now) switches to the decoded output pattern and READ/REFERENCE CLOCK output is switched from the READ/REFERENCE CLOCK to the PLL's clock. *See Figure 3.*

For MFM, the address mark is fixed internally as "A1" (HEX) or 10100001 where the clock pulse associated with bit 6 is not present. "A1" FOUND, a pulse from the μA2490 to the controller, is asserted at the rise of the VCO CLOCK associated with bit 6 of the address mark byte and is reset at the fall of the VCO CLOCK.

NRZ DATA OUT and CLOCK are supplied continuously thereafter by the μA2490 until negation of the READ GATE signal by the controller. At that point the PLL is resynchronized with the REFERENCE OSCILLATOR and the reference clock is presented at the READ/REFERENCE output.

Write

Write operations are begun at the assertion of WRITE GATE by the controller. The PLL remains phase and frequency locked to the REFERENCE OSCILLATOR input all the time during the WRITE MODE. WRITE CLOCK must be synchronized to the READ/REFERENCE CLOCK and the jitter should be less than ± 1/4 of a period for reliable data transfer. The internal clock will be realigned to the write clock to assure reliable data transfer. WRITE DATA is sampled for processing on the first rising edge of WRITE CLOCK following the assertion of WRITE GATE. Prior to clocking out the first encoded data bit, an encoded zero pattern (preset internally) is clocked out for an integral number of WRITE CLOCK intervals (associated with internal processing, 7 clock periods for MFM and 9 clock periods for 2,7). *See Figure 4.*

The alignment of encoded RZ WRITE DATA pulses with respect to the internal VCO clock is modified by the μA2490 according to precompensation rules shown in Table 1a. The amount of precompensation is one of four values (including zero) set by the state of the two PRECOMPENSATION SELECT inputs. The actual precompensation value is given in Table 1b as a percent of the oscillator period. The percentages are ±0%, ±5%, ±10%, and ±15% of the 2f clock.

For MFM, unique address mark bytes may be written by supplying an NRZ data stream representing "A1" (HEX) and asserting the WRITE MISSING CLOCK line at the fall of WRITE CLOCK for bit 1. *See Figure 5.* WRITE MISSING CLOCK must be negated at the fall of WRITE CLOCK for bit 8 of the "A1" byte. This suppresses the normal "clock" transition for bit cell 6. The assertion or deassertion of WRITE MISSING CLOCK line does not have to be synchronous with the WRITE CLOCK. The level of WRITE MISSING CLOCK SIGNAL does not have any effect on the operation of μA2490 in 2,7 mode.

Writing proceeds continuously until negation of WRITE GATE. Only the transitions (or lack thereof) associated with the WRITE DATA bit valid at the last rise of WRITE CLOCK will be written. Note that because of the aforementioned internal processing delays the writing of the last flux transitions will occur seven clock intervals for MFM (or nine clock intervals for 2,7) after the negation of WRITE GATE. Null bits appended to the controller write data stream allow for the finite turn-off time of write current.

Figure 4 Write Data Transfer Timing

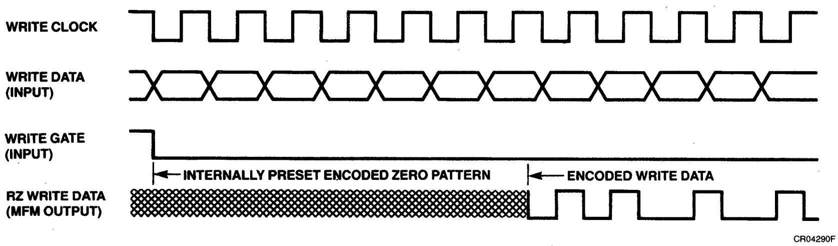
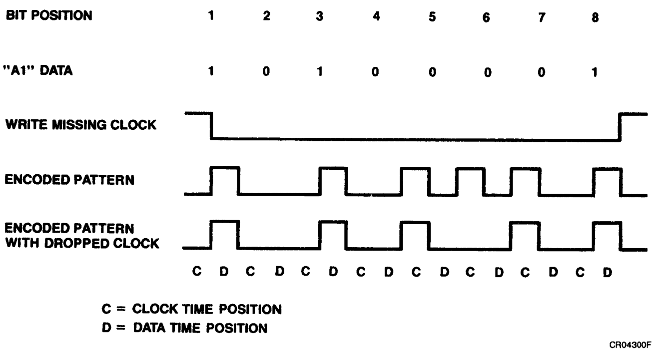


Figure 5 Missing Clock Generation



Recommended Operating Conditions

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_{CC}	Supply Current	V_{CC} = 5.0 V		200		mA
T_A	Ambient Temperature		0	25	70	C
f_{DATA}	Input Data Rate				25	Mbps
T_{REF}	Reference Oscillator Clock Period		40			ns
W_{REF}	Width of Reference Oscillator Clock		10			ns
T_{WFD}	Width of Encoded RZ Data Pulse			½T_{ref}		
T_{RZD}	Pulse Width of RZ Read Data		10			ns

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = Max	$V_{CC} - 2.0$	$V_{CC} - 1.6$		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = Max			0.5	V
I_{IH}	Input Current HIGH	$V_{IH} = 2.7$ V		80		μA
I_{IL}	Input Current LOW	$V_{IL} = 0.4$ V		195		μA
I_{OH}	Output Current HIGH		−800			μA
I_{OL}	Output Current LOW				10	μA
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V

AC Characteristics

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$T_{Lock\ R}$	Positive input transitions after Read Gate goes LOW	Gate not connected to VCO capacitor		32		TBD	Ref Clock Period
$T_{Lock\ W}$	Positive input after Read Gate goes HIGH until PLL locks to reference oscillator	Gate not connected to VCO capacitor		16		TBD	Ref Clock Period
Decode MFM	Number of clock cycles required until output RZ_{in} NRZ_{out}	MFM			1		Ref Clock Period
Decode 2,7	Number of clock cycles required until output	(2,7)			5		Ref Clock Period
Encode MFM	Number of clock cycles accompanying input data to encoded write data NRZ_{in} RZ_{out}	MFM			7		Ref Clock Period
Encode 2,7	Number of clock cycles accompanying input data to encoded write data	(2,7)			9		Ref Clock Period
K_I	Charge Pump and Filter Gain	n = number of VCO cycles between Data Bits, MFM: $1 \leqslant n \leqslant 3$ 2,7: $2 \leqslant n \leqslant 7$	Slow		$\frac{5}{2\pi n C_f R_{cps}}$		Amps/ radian
			Fast		$\frac{5}{2\pi n C_f R_{cps} \| R_{cpf}}$		
$V_{Control}$	Differential Voltage Swing of Charge Pump				±400		mV

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Electrical Characteristics (Cont.) T_A = 25°C, V_{CC} = 5.0 V, unless otherwise specified.

AC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
K_{VCO}	VCO Gain Constant	Measured from filter output		0.5 ω_{VCO}		Radians/ sec-volt
$f_{MAX\ VCO}$	Maximum VCO Frequency			70		MHz
f_{VCO}	VCO Center Frequency Tolerance			±30		%
f_{TEMPCO}	VCO Center Frequency Temperature Coefficient			−5		%/°C

External Component Selection

Symbol	Characteristic	Min	Typ	Max	Unit	Components
C_{VCO}	VCO Frequency Set Capacitor[1]	5.0			pF	
R_{CPS}	Charge Pump Slow Resistor	0.7	5.0	50	kΩ	
R_{CPF}	Charge Pump Fast Resistor	0.7	5.0	50	kΩ	
C_{ss}	Delay Capacitor[2]	10			pF	
R_{ss}	Delay Current Setting Resistor[2]	0.1	1.5		kΩ	

Notes

1. $C_{VCO} = 1/(2K)\ (f_{VCO})$
2. Delay Time = $T_{VCO}/2 = (0.673)R_{ss}C_{ss}$

Table 1a Precompensation Patterns

2,7 Precompensation Patterns

Past			Present	Future		
+3	+2	+1	Write Bit	−1	−2	−3
0	0	0	ON TIME	0	0	0
1	0	0	ON TIME	0	0	1
1	0	0	EARLY	0	0	0
0	0	0	LATE	0	0	1

MFM Precompensation Patterns

Past		Present	Future	
+2	+1	Write Bit	−1	−2
0	0	ON TIME	0	0
1	0	ON TIME	0	1
1	0	EARLY	0	0
0	0	LATE	0	1

Table 1b Precompensation Values

Precomp. MSB	Value LSB	Bit Interval Shift % Of 2f Clock
0	0	±0%
0	1	±5%
1	0	±10%
1	1	±15%

Table 2 2,7 Code Pattern

Data				Code							
A	B	C	D	8	7	6	5	4	3	2	1
0	1			0	1	0	0				
0	0			1	0	0	0				
1	1	1		0	0	0	1	0	0		
1	0	0		0	0	1	0	0	0		
1	0	1		1	0	0	1	0	0		
1	1	0	1	0	0	1	0	0	1	0	0
1	1	0	0	0	0	0	0	1	0	0	0

Table 3 Tabulated Values for VCO and Single Shot

Data Rate Mbps	VCO Freq MHz	C_{VCO} VCO Cap	C_{ss} Delay Cap	R_{ss} Delay Res
25	50	12 pF	10 pF	1.5 kΩ
20	40	18 pF	12 pF	1.5 kΩ
15	30	25 pF	16 pF	1.5 kΩ
10	20	39 pF	24 pF	1.5 kΩ
5	10	85 pF	49 pF	1.5 kΩ

Recommended Charge Pump and Filter Component Values for 10 Mbps Operation.

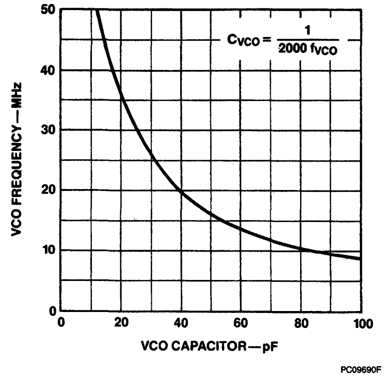
$C_f = 0.47\ \mu F$ $R_f = 220\ \Omega$ $R_{cpf} = 5.1\ k\Omega$
$C_p = 0.0047\ \mu F$ $R_{cps} = 5.1\ k\Omega$

Layout Precautions

A careful layout is required when attaching the critical timing components to the Data Separator. Connect the VCO capacitor and the Single Shot capacitor as close to the chip as possible. This will help cut down on the amount of noise picked up from other switching components nearby on the board that will affect the timing. The filter components should also be placed as close to the chip as the layout will allow, with the returns making as short a path as possible to the chip supply or ground. The chip itself should be well decoupled with the decoupling capacitors placed close to the chip. All leads on the timing and filter components should be kept as short as possible.

A good ground plane should be used in the vicinity of the Data Separator chip. Digital signals should be kept away from the vicinity of the chip. Wire wrap configurations should be avoided for best performance. All filter capacitors and single shot delay capacitors should be connected to the V_{CC} lead.

VCO Capacitor



Delay Circuit Values

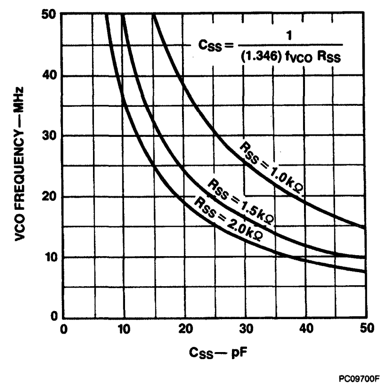


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Figure 6 ST506

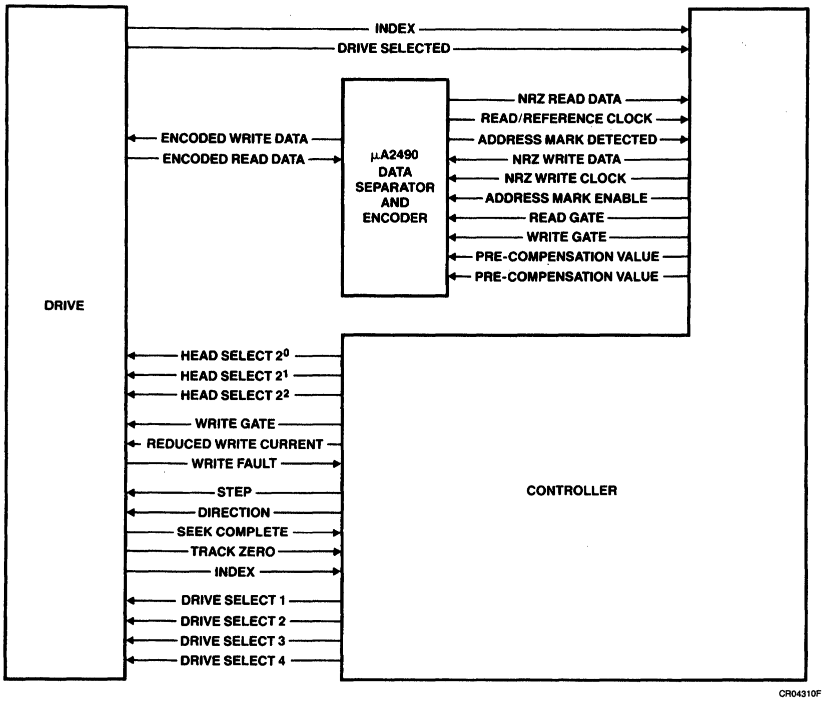
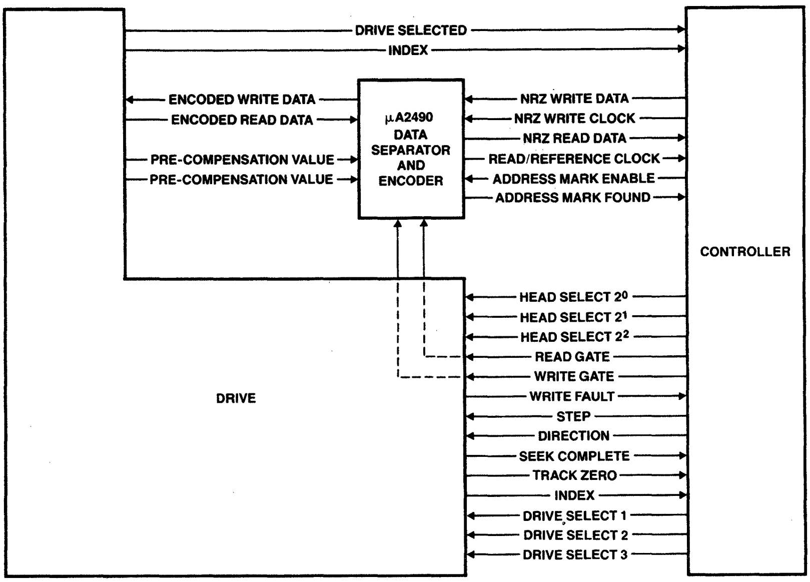


Figure 7 ESDI



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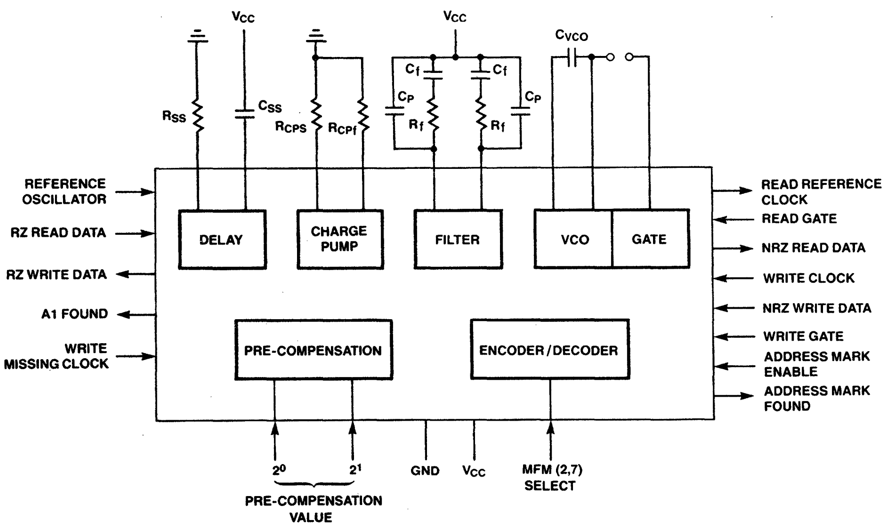
Typical Hook-up Diagram



CR04330F

FAIRCHILD

A Schlumberger Company

μA2580 Winchester Disk Servo Preamplifier

Preliminary

Linear Division Disk Drives

Description

The μA2580 provides termination, gain, and impedance buffering for the thin film servo read head in Winchester disk drives. It is a differential output design with fixed gain of approximately 250. The bandwidth is guaranteed greater than 30 MHz.

The internal design of the μA2580 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-lead ceramic DIP, 10-lead Flatpak, and an SO-8 package suitable for surface mounting.

- **Low Input Noise Voltage, Typ 0.5 nV/$\sqrt{Hz}$**
- **Wide Power Supply Range (8.0 V to 13 V)**
- **Internal Damping Resistors (1.0 kΩ)**

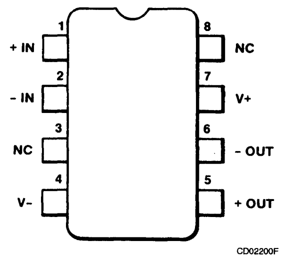
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP and Flatpak	−65°C to +175°C
SO-8	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP and Flatpak (soldering, 60 s)	300°C
SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
10L-Flatpak	0.79 W
SO-8	0.81 W
Supply Voltage	15 V
Output Voltage	15 V
Differential Input Voltage	±1.0 V

Notes

1. $T_{J\,Max}$ = 150°C for the SO-8, and 175°C for the Ceramic DIP and Flatpak.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 10L-Flatpak at 5.3 mW/°C, and the SO-8 at 6.5 mW/°C.

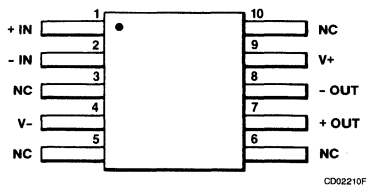
Connection Diagram 8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA2580DC	6T	Ceramic DIP
μA2580SC	KC	Molded Surface Mount

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Device Code	Package Code	Package Description
μA2580FC	3F	Flatpak

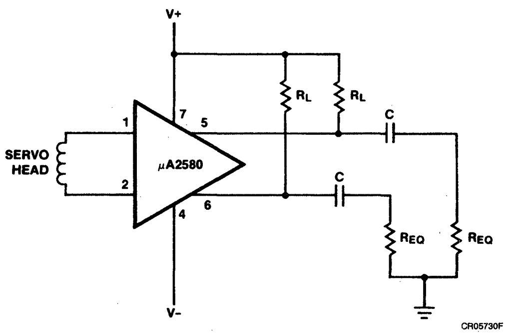
Description Of Lead Functions

Name	Description of Functions
+IN	Positive Differential Input
−IN	Negative Differential Input
NC	
V−	Negative Differential Supply with respect to Vcc.
+OUT	Positive Differential Output
−OUT	Negative Differential Output
V+	Positive Differential Supply with respect to Vcc
NC	No Connection

μA2580
Electrical Characteristics T_A = 25 C, (V+) – (V–) = 8.0 to 13.2 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
G	Gain (differential)	R_P = 100 Ω, (V+) – (V–) = 12 V		250		
BW	Bandwidth (3 dB)	V_I = 0.5 mV_{p-p}	30	65		MHz
R_I	Input Resistance			300		Ω
C_I	Input Capacitance			35		pF
V_I	Input Dynamic Range (Differential)	R_P = 100 Ω, (V+) – (V–) = 12 V			1.0	mV p-p
I_S	Supply Current	(V+) – (V–) = 12 V		28	40	mA
ΔV_O	Output Offset (Differential)	R_s = 0, R_P = 100 Ω	600		600	mV
V_n	Equivalent Input Noise	BW = 4.0 MHz		0.6		nV/√Hz
PSRR	Power Supply Rejection Ratio	R_s = 0, f = 5.0 MHz	50	65	0.90	dB
ΔG/V	Gain Sensitivity (Supply)	Δ (V+) – (V–) ± 10%, R_P = 100 Ω			0.5	%/V
ΔG/T	Gain Sensitivity (Temp)	T_A = 25°C to 70°C, R_P = 100 Ω		0.16		%/°C
CMR	Common Mode Rejection (Input)	f = 5.0 MHz	60	70		dB

Typical Application (Notes 1-4)



Notes
1. Leads shown for 8-lead DIP.
2. R_{EQ} is equivalent load resistance.
3. $R_P = \frac{R_L \cdot R_{EQ}}{R_L + R_{EQ}}$
4. G = 2.5 R_P
   Where R_P = value from Note 3 (above) in ohms.

FAIRCHILD
A Schlumberger Company

μA105 • μA305 μA305A • μA376 Voltage Regulators

Linear Division Voltage Regulators

6

Description

The μA105/305/305A/376 are monolithic positive voltage regulators constructed using the Fairchild Planar Epitaxial process. Applications for these devices include both linear and switching regulator circuits with output voltages greater than 4.5 V. These devices will not oscillate when confronted with varying resistive and reactive loads and will start reliably regardless of the load within the ratings of the circuit. They also feature fast response to both load and line transients. Used independently, the μA105/305 will supply 12 mA, the μA305A, 45 mA and μA376, 25 mA. The μA105 is specified for the extended temperature range of −55°C to +125°C. The μA305/376/305A are specified for 0°C to +70°C operation. The μA105/305/305A are in an 8-lead TO-5 package and the μA376 is available in the space and cost saving DIP.

- **Low Standby Current Drain**
- **Adjustable Output Voltage From 4.5 To 40 V**
- **High Output Currents Exceeding 10 A With External Components**
- **Load Regulation Better Than 0.1%, Full Load With Current-Limiting**
- **DC Line Regulation Guaranteed At 0.03%/V**
- **Ripple Rejection Of 0.01%/V**
- **Available In Extended Temperature Range**

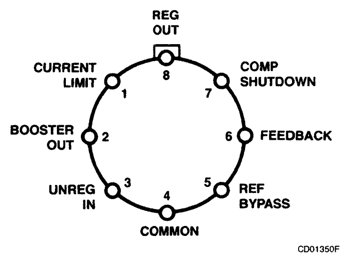
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA105)	−55°C to +125°C
Commercial (μA205, μA305A, μA376)	0°C to 70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
Input Voltage	
μA105, μA305A	50 V
μA305, μA376	40 V
Input/Output Voltage Differential	40 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.

Connection Diagram
8-Lead Metal Package
(Top View)

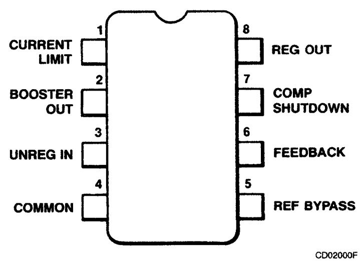


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA105HM	5W	Metal
μA305HC	5W	Metal
μA305AHC	5W	Metal

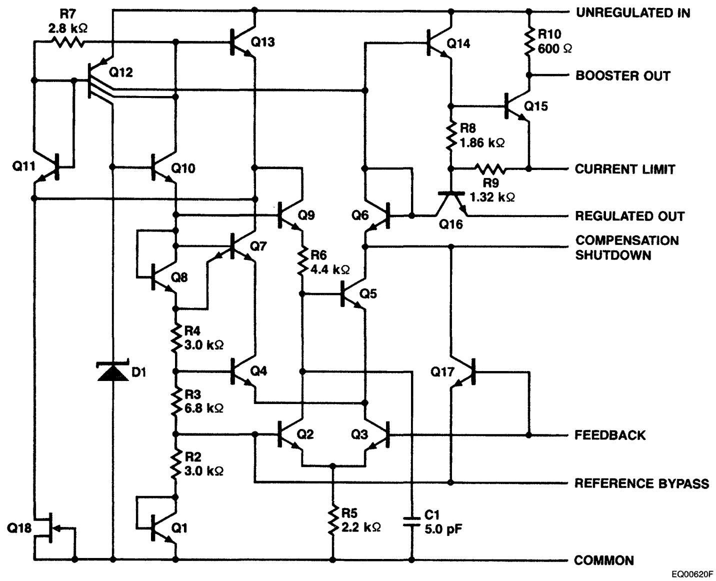
Connection Diagram
8-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA376TC	9T	Molded DIP

Equivalent Circuit



μA105
Electrical Characteristics $T_A = 25°C$ unless otherwise specified[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range			8.5		50	V
V_{OR}	Output Voltage Range			4.5		40	V
$V_I - V_O$	Input/Output Voltage Differential			3.0		30	V
$V_{R\ LINE}$	Line Regulation	$V_I - V_O \leqslant 5.0$ V			0.025	0.06	%/V
		$V_I - V_O > 5.0$ V			0.015	0.03	
$V_{R\ LOAD}$	Load Regulation[2]	$0 \leqslant I_L \leqslant 12$ mA	$R_{SC} = 10\ \Omega$, $T_A = 25°C$		0.02	0.05	%
			$R_{SC} = 10\ \Omega$, $T_A = 125°C$		0.03	0.1	
			$R_{SC} = 10\ \Omega$, $T_A = -55°C$		0.03	0.1	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.02	%/V
T_S	Temperature Stability[4] of FBSV	$-55°C \leqslant T_A \leqslant +125°C$			0.3	1.0	%
FBSV	Feedback Sense Voltage			1.63	1.7	1.81	V
N_O	Noise	10 Hz $\leqslant f \leqslant$ 10 kHz	$C_{REF} = 0$		0.005		%
			$C_{REF} > 0.1\ \mu F$		0.002		
V_{CLS}	Current Limit Sense Voltage[3]	$R_{SC} = 10\ \Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV

μA105 (Cont.)
Electrical Characteristics $T_A = 25°C$ unless otherwise specified[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
I_{SCD}	Standby Current Drain	$V_I = 50$ V			0.8	2.0	mA
S	Long Term Stability of FBSV	$T_J = 125°C$	$T_A = 25°C$ For End Point Measurement		0.1	1.0	%/1000 hrs

μA305A
Electrical Characteristics $T_A = 25°C$ unless otherwise specified[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range			8.5		50	V
V_{OR}	Output Voltage Range			4.5		40	V
$V_I - V_O$	Input/Output Voltage Differential			3.0		30	V
$V_{R\ LINE}$	Line Regulation	$V_I - V_O \leq 5.0$ V			0.025	0.06	%/V
		$V_I - V_O > 5.0$ V			0.015	0.03	
$V_{R\ LOAD}$	Load Regulation	$0 \leq I_L \leq 45$ mA	$R_{SC} = 0\ \Omega$, $T_A = 25°C$		0.02	0.2	%
			$R_{SC} = 0\ \Omega$, $T_A = 70°C$		0.03	0.4	
			$R_{SC} = 0\ \Omega$, $T_A = 0°C$		0.03	0.4	
$\Delta V_I - \Delta V_O$	Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.02	%/V
T_S	Temperature Stability[4] of FBSV	$0°C \leq T_A \leq +70°C$			0.3	1.0	%
FBSV	Feedback Sense Voltage			1.55	1.7	1.85	V
N_O	Noise	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
			$C_{REF} > 0.1\ \mu F$		0.002		
V_{CLS}	Current Limit Sense Voltage[3]	$R_{SC} = 10\ \Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV
I_{SCD}	Standby Current Drain	$V_I = 50$ V			0.8	2.0	mA
S	Long Term Stability of FBSV	$T_J = 125°C$	$T_A = 25°C$ For End Point Measurements		0.1	1.0	%/1000 hrs

μA305
Electrical Characteristics $T_A = 25°C$ unless otherwise specified[1]

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IR}	Input Voltage Range		8.5		40	V
V_{OR}	Output Voltage Range		4.5		30	V
$V_I - V_O$	Input/Output Voltage Differential		3.0		30	V
$V_{R\ LINE}$	Line Regulation	$V_I - V_O \leq 5.0$ V		0.025	0.06	%/V
		$V_I - V_O > 5.0$ V		0.015	0.03	

μA305 (Cont.)
Electrical Characteristics $T_A = 25°C$ unless otherwise specified[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$V_{R\ LOAD}$	Load Regulation[2]	$0 \leq I_L \leq 12$ mA	$R_{SC} = 10\ \Omega$, $T_A = 25°C$		0.02	0.05	%
			$R_{SC} = 15\ \Omega$, $T_A = 70°C$		0.03	0.1	
			$R_{SC} = 10\ \Omega$, $T_A = 0°C$		0.03	0.1	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$C_{REF} = 10\ \mu F$, $f = 120$ Hz			0.003	0.02	%/V
T_S	Temperature Stability[4] of FBSV	$0°C \leq T_A \leq +70°C$			0.3	1.0	%
FBSV	Feedback Sense Voltage			1.63	1.7	1.81	V
N_O	Noise	$10\ Hz \leq f \leq 10$ kHz	$C_{REF} = 0$		0.005		%
			$C_{REF} > 0.1\ \mu F$		0.002		
V_{CLS}	Current Limit Sense Voltage[3]	$R_{SC} = 10\ \Omega$, $T_A = 25°C$ $V_O = 0$ V		225	300	375	mV
I_{SCD}	Standby Current Drain	$V_I = 40$ V			0.8	2.0	mA
S	Long Term Stability of FBSV	$T_J = 125°C$	$T_A = 25°C$ For End Point Measurements		0.1	1.0	%/1000 hrs

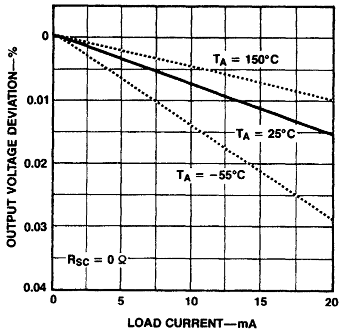
μA376
Electrical Characteristics $0°C \leq T_A \leq 70°C$

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range			9.0		40	V
V_{OR}	Output Voltage Range			5.0		37	V
$V_I - V_O$	Input/Output Voltage Differential			3.0		30	V
$V_{R\ LINE}$	Line Regulation	$T_A = 25°C$				0.03	%/V
		$0°C \leq T_A \leq 70°C$				0.1	
$V_{R\ LOAD}$	Load Regulation	$0 \leq I_L \leq 25$ mA	$R_{SC} = 0\ \Omega$, $T_A = 25°C$			0.2	%
			$R_{SC} = 0\ \Omega$, $T_A = 70°C$			0.5	
			$R_{SC} = 0\ \Omega$, $T_A = 0°C$			0.5	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$f = 120$ Hz, $T_A = 25°C$				0.1	%/V
V_{CLS}	Current Limit Sense Voltage				360		mV
I_{SCD}	Standby Current Drain	$V_{IN} = 30$ V, $T_A = 25°C$				2.5	mA
V_{REF}	Reference Voltage			1.60	1.72	1.80	V

Notes
1. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2.0 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
2. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
3. With no external pass transistor.
4. Temperature stability is defined as the percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

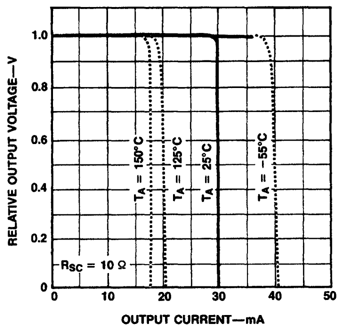
Typical Performance Curves

Load Regulation



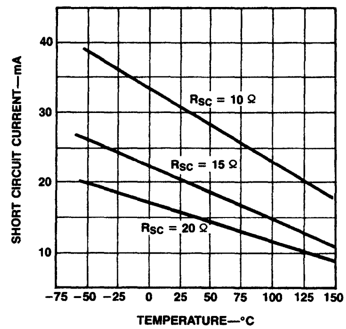
PC09050F

Current-Limiting Characteristics



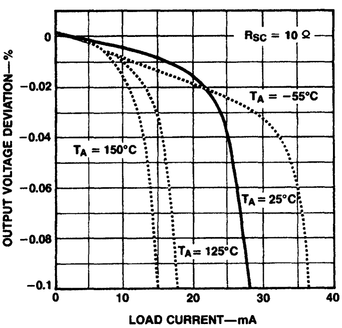
PC09060F

Short Circuit Current vs Temperature



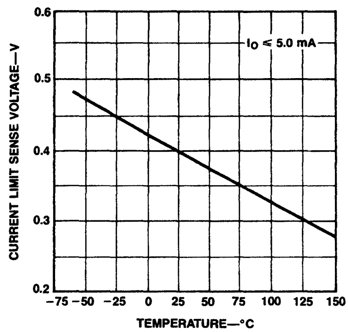
PC09070F

Load Regulation



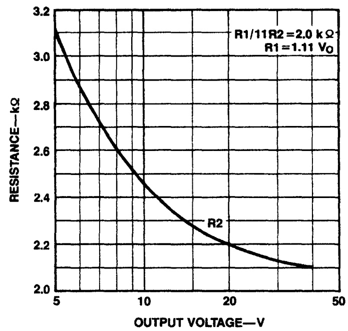
PC09080F

Current Limit Sense Voltage vs Temperature



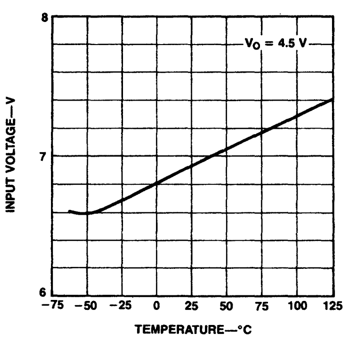
PC09090F

Optimum Divider Resistance Values



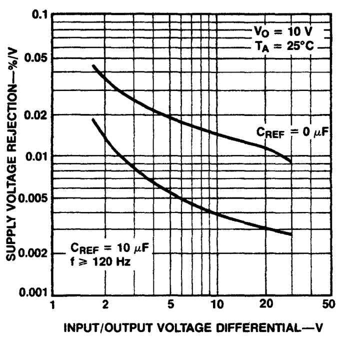
PC09101F

Minimum Input Voltage vs Temperature



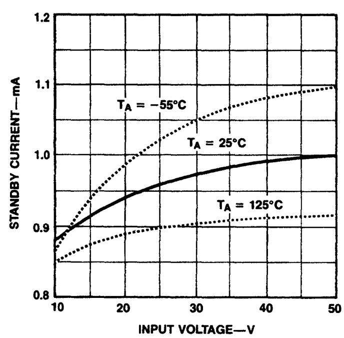
PC09110F

Supply Voltage Rejection vs Input/Output Voltage Differential



PC09120F

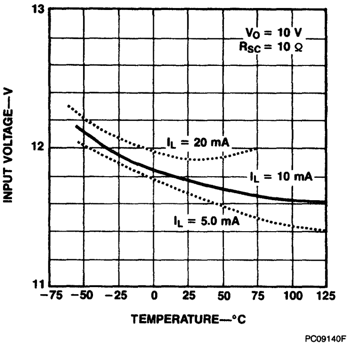
Standby Current Drain vs Input Voltage



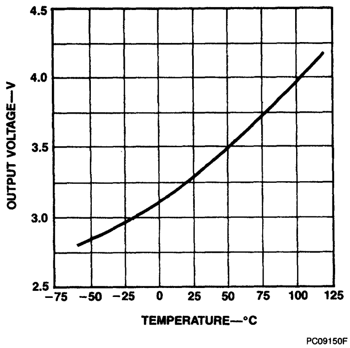
PC09130F

Typical Performance Curves (Cont.)

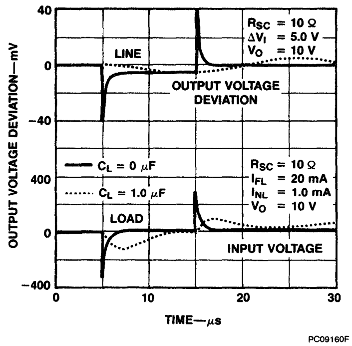
Regulator Dropout Voltage



Minimum Output Voltage vs Temperature

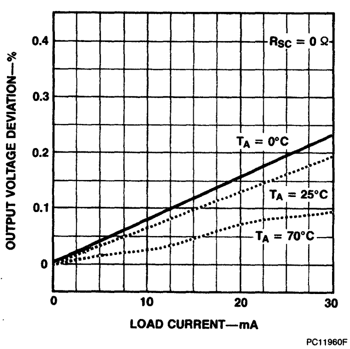


Transient Response

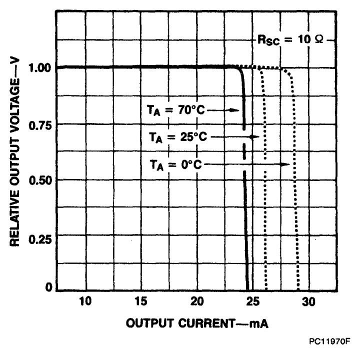


Typical Performance Curves for μA376

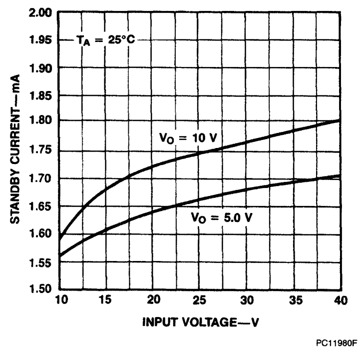
Load Regulation



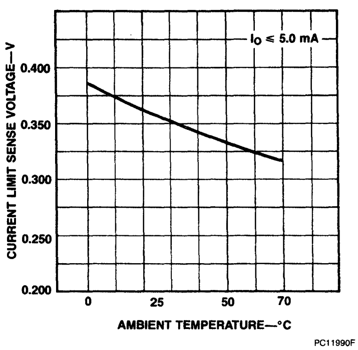
Current Limiting Characteristics



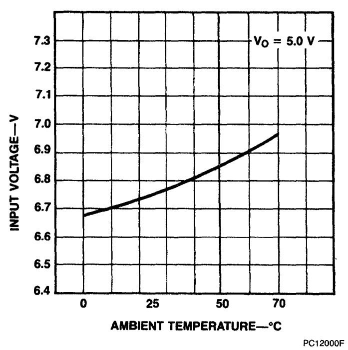
Standby Current Drain vs Input Voltage



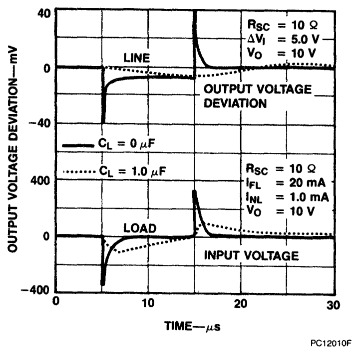
Current Limit Sense Voltage vs Temperature



Minimum Input Voltage vs Temperature

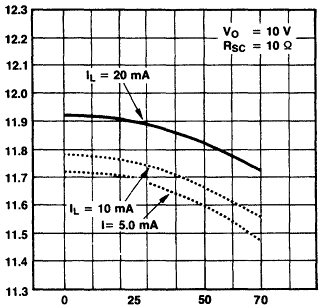


Transient Response

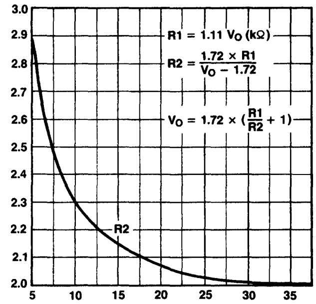


Typical Performance Curves for μA376 (Cont.)

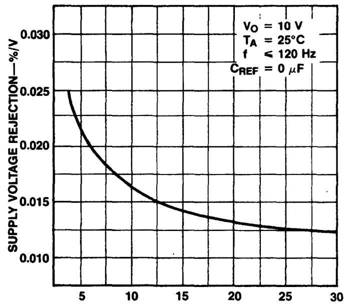
Regulator Dropout Voltage



Optimum Divider Resistance

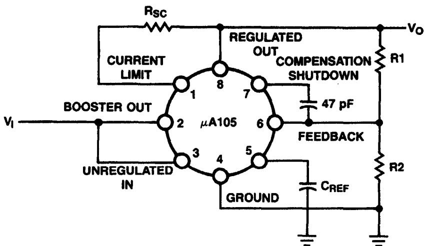


Supply Voltages Rejection vs Input/Output Voltage Differential



Typical Applications

Basic Positive Regulator With Current-Limiting



$V_O \approx 1.72 \frac{R1 + R2}{R2}$ V

$I_{OS} \approx \frac{V_{SENSE}}{R_{SC}}$ mA

CR03621F

FAIRCHILD
A Schlumberger Company

μA117 • μA217 • μA317 3-Terminal Positive Adjustable Regulators

Linear Division Voltage Regulators

Description

The μA117/μA217/μA317 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially blow out proof.

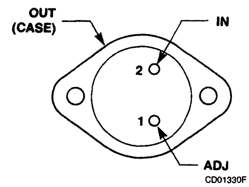
The μA117 series serves a wide variety of applications including local, on-card regulation. They also make an especially simple adjustable switching regulator, and a programmable output regulator; or by connecting a fixed resistor between the adjustment and output, the μA117 series can be used as a precision current regulator.

- **Output Current In Excess Of 1.5 A In TO-3 And TO-220 Packages**
- **Output Adjustable Between 1.2 V And 37 V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting Constant Temperature**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation For High Voltage Applications**
- **Standard 3-Terminal Transistor Packages**
- **Available In Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	-65°C to +175°C
TO-220 Package	-65°C to +150°C
Operating Junction Temperature Range	
Extended (μA117)	-55°C to +150°C
Industrial (μA217)	-40°C to +150°C
Commercial (μA317)	0°C to +150°C
Lead Temperature	
TO-3 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input/Output Voltage Differential	40 V

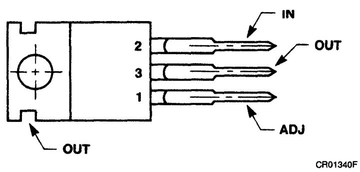
Connection Diagram
TO-3 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA117KM	HJ	Metal
μA217KV	HJ	Metal
μA317KC	HJ	Metal

Connection Diagram
TO-220 Package
(Top View)

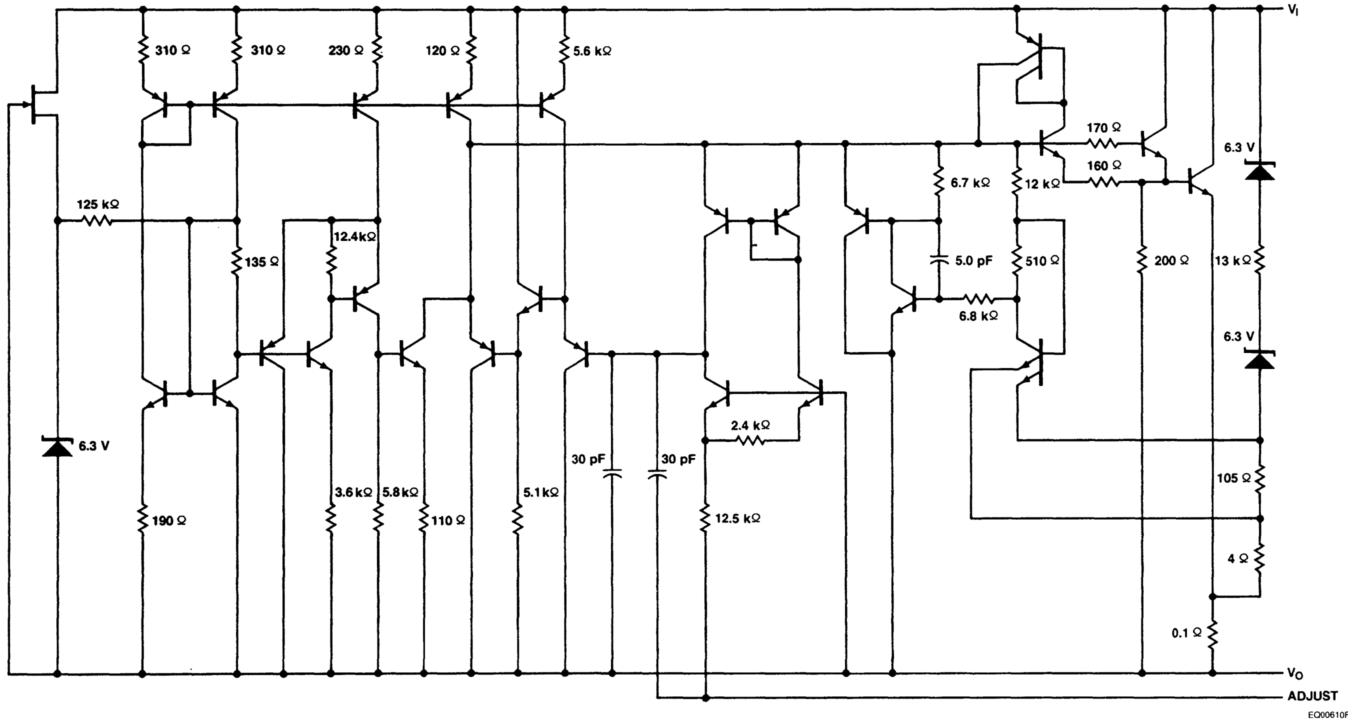


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA217UV	GH	Molded Power Pack
μA317UC	GH	Molded Power Pack

Equivalent Circuit



Electrical Characteristics T_J = −55°C to +150°C for the μA117, −40°C to +125°C for the μA217, and 0°C to +125°C for the μA317; $V_I - V_O$ = 5.0 V; I_O = 0.5 A; I_{Max} = 1.5 A; P_{Max} = 20 W; unless otherwise specified.

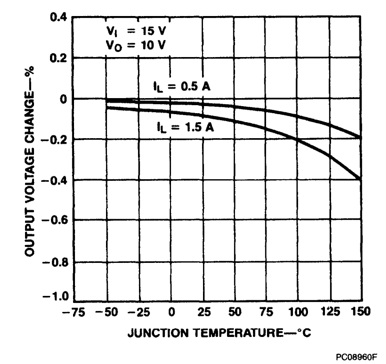
Symbol	Characteristic	Condition[1]		μA117/217 Min	μA117/217 Typ	μA117/217 Max	μA317 Min	μA317 Typ	μA317 Max	Unit
$V_{R\ LINE}$	Line Regulation[1,5]	T_A = 25°C; 3.0 V ≤ $V_I - V_O$ ≤ 40 V			0.01	0.02		0.01	0.04	%/V
		3.0 V ≤ $V_I - V_O$ ≤ 40 V			0.02	0.05		0.02	0.07	
$V_{R\ LOAD}$	Load Regulation[1]	T_A = 25°C, 10 mA ≤ I_O ≤ I_{Max}	V_O ≤ 5.0 V		5.0	15		5.0	25	mV
			V_O ≥ 5.0 V		0.1	0.3		0.1	0.5	%V_O
		10 mA ≤ I_O ≤ I_{Max}	V_O ≤ 5.0 V		20	50		20	70	mV
			V_O ≥ 5.0 V		0.3	1.0		0.3	1.5	%V_O
I_{adj}	Adjustment Lead Current				50	100		50	100	μA
ΔI_{adj}	Adjustment Lead Current Change	2.5 V ≤ $V_I - V_O$ ≤ 40 V; 10 mA ≤ I_O ≤ I_{Max}, P_D ≤ P_{Max}			0.2	5.0		0.2	5.0	μA
V_{REF}	Reference Voltage[2]	3.0 V ≤ $V_I - V_O$ ≤ 40 V; 10 mA ≤ I_O ≤ I_{Max}; P_D ≤ P_{Max}		1.20	1.25	1.30	1.20	1.25	1.30	V
T_S	Temperature Stability				0.7			0.7		%V_O
$I_{O\ Min}$	Minimum Load Current to Maintain Regulation	$V_I - V_O$ = 40 V			3.5	5.0		3.5	10	mA
$I_{O\ Max}$	Maximum Output Current	$V_I - V_O$ ≤ 15 V, P_D ≤ P_{Max}		1.5	2.2		1.5	2.2		A
		T_A = 25°C, $V_I - V_O$ = 40 V, P_D ≤ P_{Max}		0.25	0.4		0.15	0.4		
N_O	Noise	T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz			0.003			0.003		%V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection[3]	V_O = 10 V, f = 120 Hz	Without C_{adj}		65			65		dB
			C_{adj} = 10 μF	66	80		66	80		
S	Long-Term Stability,[4] $T_J = T_{J\ Max}$	T_A = 25°C for Endpoint Measurements			0.3	1.0		0.3	1.0	%/1000 hrs

Notes
1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. Selected devices with tightened tolerance reference voltage available.
3. C_{adj}, when used, is connected between the adjustment lead and ground.
4. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. I_O = 0.5 A for $V_I - V_O$ ≤ 25 V and I_{Max} for $V_I - V_O$ ≥ 25 V.

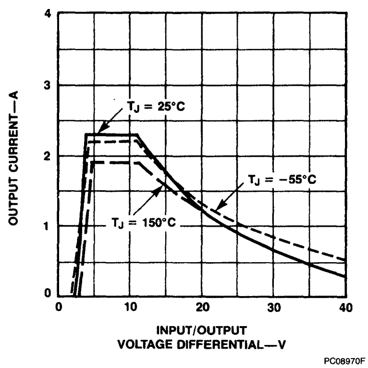
6

Typical Performance Curves

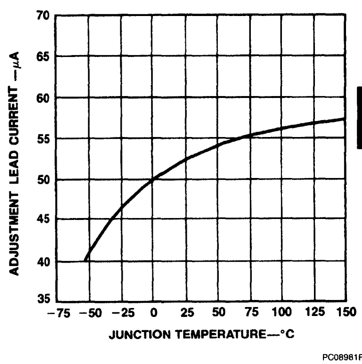
Load Regulation



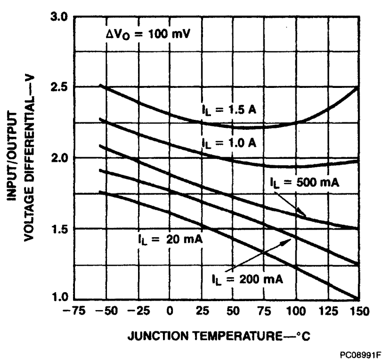
Current Limit



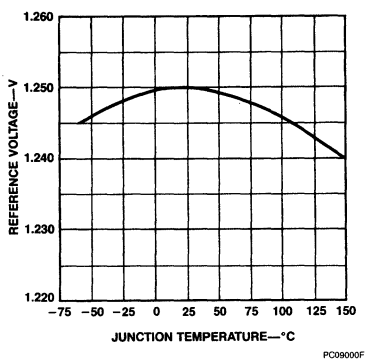
Adjustment Lead Current



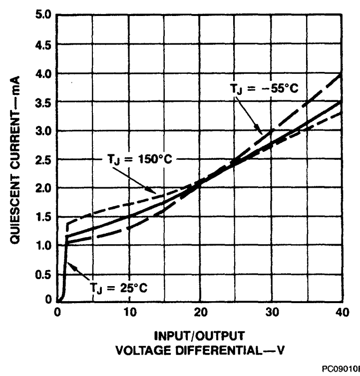
Dropout Voltage



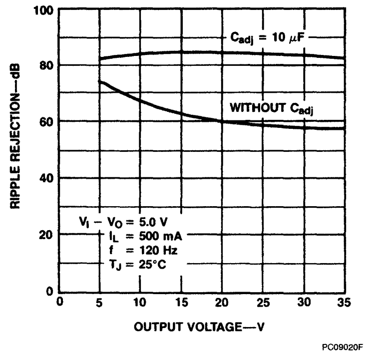
Temperature Stability



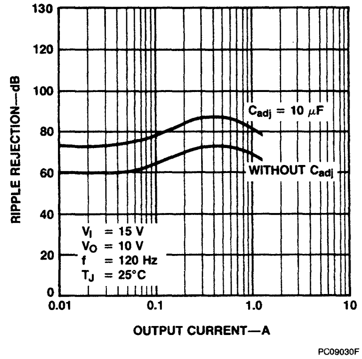
Minimum Operating Current



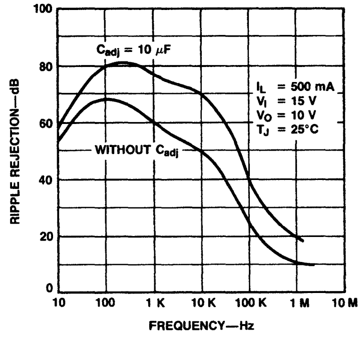
Ripple Rejection vs Output Voltage



Ripple Rejection vs Output Current

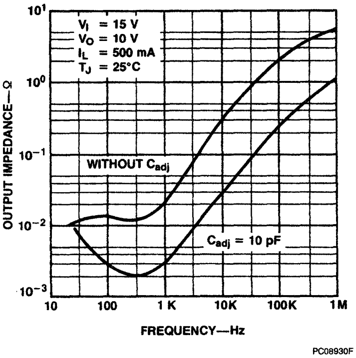


Ripple Rejection vs Frequency

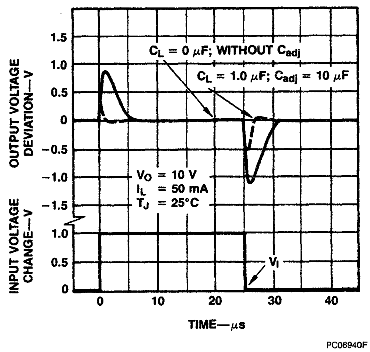


Typical Performance Curves (Cont.)

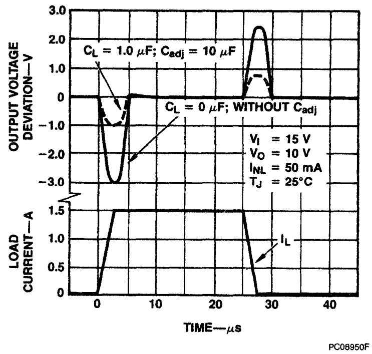
Output Impedance



Line Transient Response



Load Transient Response



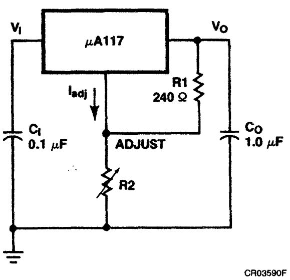
Design Considerations

To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC °C/W	Max θJC °C/W	Typ θJA °C/W	Max θJA °C/W
TO-3	2.3	3.5		35
TO-220 (μA317)		5.0		40

Typical Applications

Standard Application



C_I is required if regulator is located an appreciable distance from power supply filter.

$$V_O = 1.25\text{ V}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2 \qquad (1)$$

Since I_{adj} is controlled to less than 100 μA, the error associated with this term is negligible in most applications.

Basic Circuit Operation

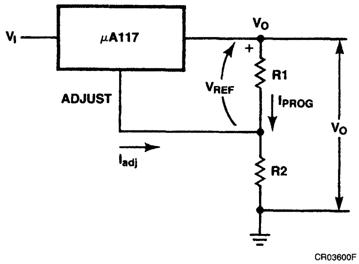
The μA117 is a 3-terminal floating regulator. In operation, the μA117 develops and maintains a nominal 1.25 V reference (V_{REF}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{Prog}) by R1 (*see Figure 1*), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{adj}\,R2 \qquad (2)$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in equation 2, the μA117 was designed to control I_{adj} to less than 0 V and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the μA117 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 1 Basic Circuit Configuration



V_{Ref} = 1.25 V Typical

Load Regulation

The µA117 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 µF disc or 1.0 µF tantalum input bypass capacitor (C_I) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

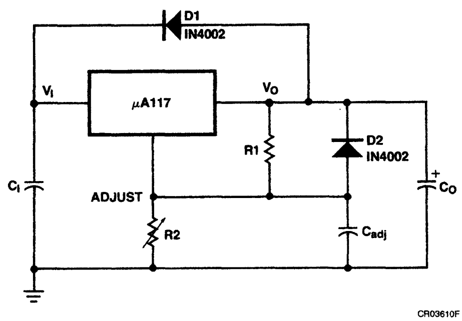
Although the µA117 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 2 shows the µA117 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ µF, $C_{adj} > 10$ µF). Diode D1 prevents C_O from discharging through the IC during an input short circuit. Diode D2 protects against capacitor C_{adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the IC during an input short circuit.

Figure 2 Voltage Regulator with Protection Diodes



FAIRCHILD

A Schlumberger Company

μA138 • μA238 • μA338 5-Amp Positive Adjustable Regulators

Linear Division Voltage Regulators

Description

The μA138/μA238/μA338 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 5.0 A over a 1.2 V to 32 V output range. They are exceptionally easy to use and require only two resistors to set the output voltage.

A unique feature of the μA138 family is time dependent current-limiting. The current limit circuitry allows peak currents of up to 12 A to be drawn from the regulator for short periods of time. This allows the μA138 family to be used with heavy transient loads and speeds start up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe-area protection for the power transistor. Overload protection remains functional even if the adjustment lead is accidentally disconnected.

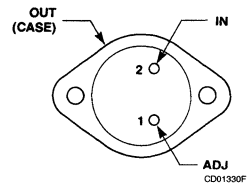
The μA138/μA238/μA338 are packaged in standard TO-3 transistor packages. The μA338 is also available in standard TO-220 transistor packages.

- **Guaranteed 7.0 A Peak Output Current**
- **Guaranteed 5.0 A Output Current**
- **Output Adjustable Between 1.2 V and 32 V**
- **Load Regulation Typically 0.1%**
- **Line Regulation Typically 0.005%/V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation for High Voltage Applications**
- **Standard TO-3 and TO-220 Transistor Packages**
- **Available in Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to 150°C
Operating Junction Temperature Range	
Extended (μA138)	−55°C to +150°C
Industrial (μA238)	−40°C to +150°C
Commercial (μA338)	0°C to +150°C
Lead Temperature	
TO-3 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input/Output Voltage Differential	35 V

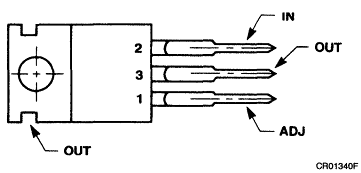
Connection Diagram TO-3 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA138KM	FT	Metal
μA238KV	FT	Metal
μA338KC	FT	Metal

Connection Diagram TO-220 Package (Top View)

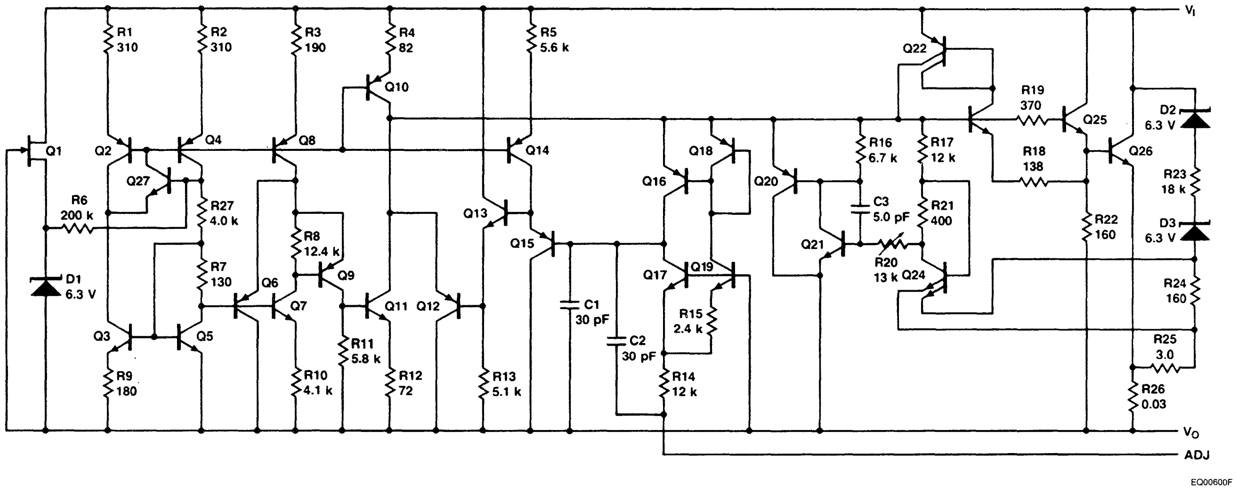


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA338UC	GH	Molded Power Pack

Equivalent Circuit



Electrical Characteristics Unless otherwise specified, these specifications apply: $-55°C \leq T_J \leq +150°C$ for the μA138, $-25°C \leq T_J \leq +150°C$ for μA238 and $0°C \leq T_J \leq +125°C$ for the μA338, $V_I - V_O = 5.0$ V and $I_O = 2.5$ A. Although power dissipation is internally limited, these specifications are applicable for power dissipation up to 50 W, for TO-3; 25 W for TO-220

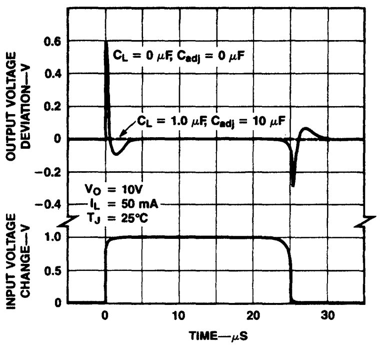
Symbol	Characteristic	Conditions		μA138/μA238 Min	μA138/μA238 Typ	μA138/μA238 Max	μA338 Min	μA338 Typ	μA338 Max	Units
V_{REF}	Reference Voltage[3]	$3.0\ V \leq V_I - V_O \leq 35\ V$, $10\ mA \leq I_O \leq 5.0\ A$, $P \leq 50\ W$, $T_A = 25°C$		1.19	1.24	1.29	1.19	1.24	1.29	V
$V_{R\ LINE}$	Line Regulation[1]	$T_A = 25°C$, $3.0\ V \leq V_I - V_O \leq 35\ V$			0.005	0.01		0.005	0.03	%/V
		$3.0\ V \leq V_I - V_O \leq 35\ V$			0.02	0.04		0.02	0.06	%/V
$V_{R\ LOAD}$	Load Regulation[1]	$T_A = 25°C$, $10\ mA \leq I_O \leq 5.0\ A$	$V_O \leq 5.0\ V$		5.0	15		5.0	25	mV
			$V_O \geq 5.0\ V$		0.1	0.3		0.1	0.5	$\%V_O$
		$10\ mA \leq I_O \leq 5.0\ A$	$V_O \leq 5.0\ V$		20	30		20	50	mV
			$V_O \geq 5.0\ V$		0.3	0.6		0.3	1.0	$\%V_O$
V_{RTH}	Thermal Regulation	Pulse = 20 ms			0.002	0.01		0.002	0.02	%/W
V_{DO}	Dropout Voltage[4]	$I_L \leq 5.0\ A$, $V_I \geq 7.0\ V$, $T_A = 25°C$		3.0			3.0			V
I_{adj}	Adjustment Lead Current				45	100		45	100	μA
ΔI_{adj}	Adjustment Lead Current Change	$10\ mA \leq I_L \leq 5.0\ A$, $3.0\ V \leq V_I - V_O \leq 35\ V$			0.2	5.0		0.2	5.0	μA
T_S	Temperature Stability	$T_{Min} \leq T_J \leq T_{Max}$			1.0			1.0		%
$I_{L\ Min}$	Minimum Load Current	$V_I - V_O = 35\ V$			3.5	5.0		3.5	10	mA
I_L	Current Limit	$V_I - V_O \leq 10\ V$		5.0	8.0		5.0	8.0		A
		0.5 ms Peak		7.0	12		7.0		12	
		$V_I - V_O = 30\ V$			1.0			1.0		
N_O	Noise	$T_A = 25°C$, $10\ Hz \leq f \leq 10\ kHz$			0.003			0.003		$\%V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_O = 10\ V$, $f = 120\ Hz$	Without C_{adj}		60			60		$\%V_O$
			$C_{adj} = 10\ \mu F$	60	75		60	75		dB
S	Long Term Stability[2]	$T_A = 25°C$ for Endpoint Measurements			0.3	1.0		0.3	1.0	%/1000 hrs

Notes

1. Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account sepatately by thermal regulation.
2. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
3. Selected devices with tightened tolerance reference voltage available.
4. Minimum $V_I - V_O$ at $0°C \leq T_J \leq +125°C$ is 3.0 V and at $-55°C \leq T_J \leq +150°C$ is 3.2 V.

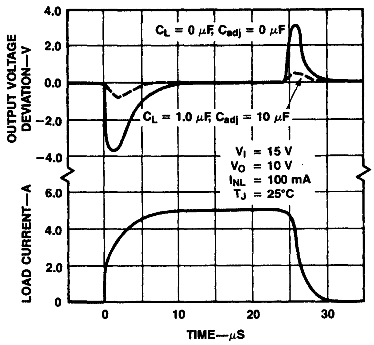
Typical Performance Curves

Line Transient Response



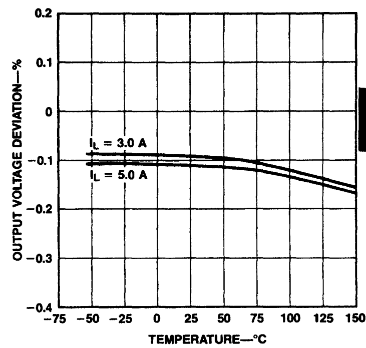
PC08780F

Load Transient Response



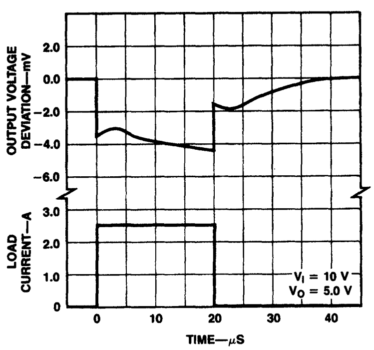
PC08790F

Load Regulation



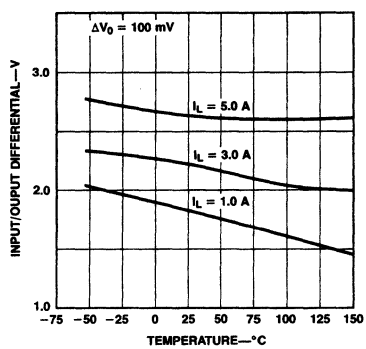
PC08800F

Thermal Regulation



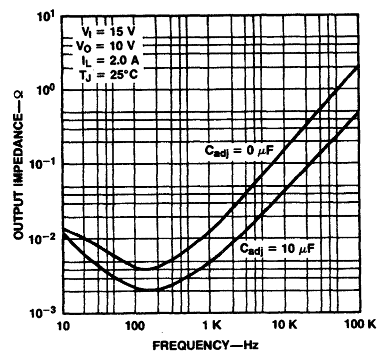
PC08810F

Dropout Voltage



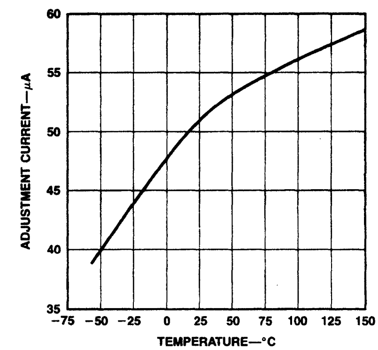
PC08820F

Output Impedance



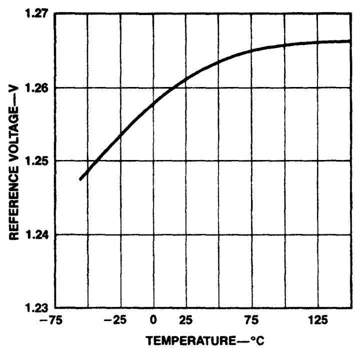
PC08830F

Adjustment Current



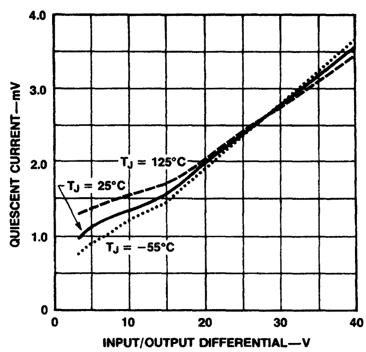
PC08840F

Temperature Stability



PC08850F

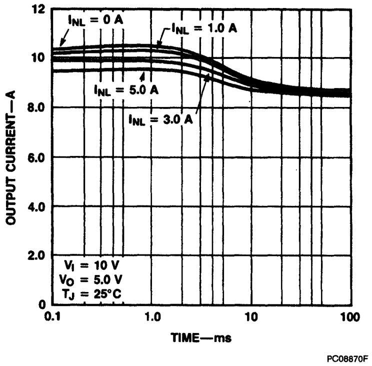
Minimum Operating Current



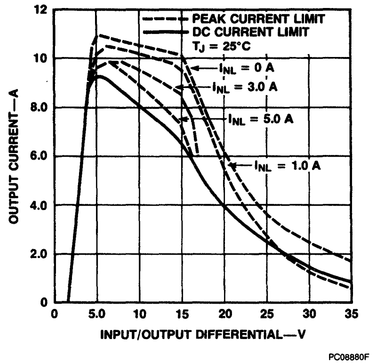
PC08860F

Typical Performance Curves (Cont.)

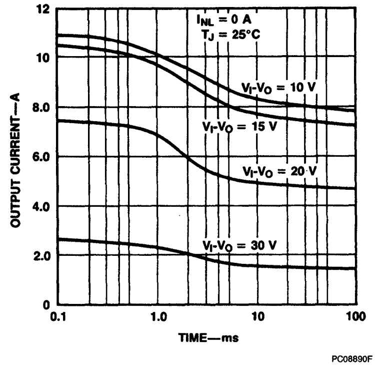
Current Limit



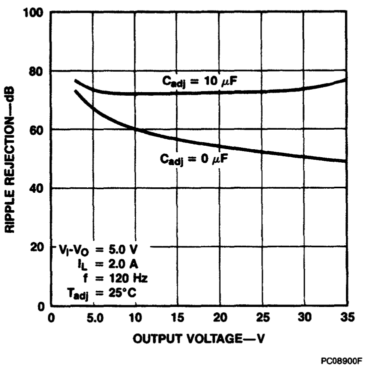
Current Limit



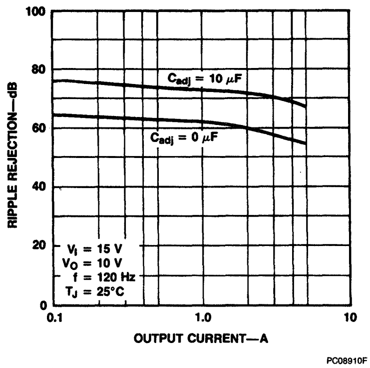
Current Limit



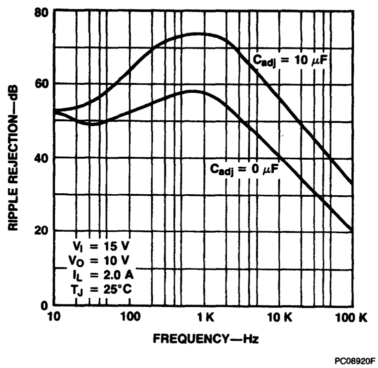
Ripple Rejection



Ripple Rejection



Ripple Rejection



Design Considerations

To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC °C/W	Max θJC °C/W	Typ θJA °C/W	Max θJA °C/W
TO-3		1.0		35
TO-220		3.5		40

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\ Max}\ T_A}{\theta_{JA}}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$ (Without heat sink)

Solving for T_J:

$T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA})$ or

$= T_A + P_D\theta_{JA}$ (Without heat sink)

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction-to-Ambient Thermal Resistance
- θ_{JC} = Junction-to-Case Thermal Resistance
- θ_{CA} = Case-to-Ambient Thermal Resistance
- θ_{CS} = Case-to-Heat Sink Thermal Resistance
- θ_{SA} = Heat Sink-to-Ambient Thermal Resistance

Typical Applications

Basic Circuit Operation

The μA138 is a 3-terminal floating regulator. In operation, the μA138 develops and maintains a nominal 1.25 V reference (V_{REF}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{Prog}) by R1 (*see Figure 1*), and this constant current flows through R2 to ground. The regulated output voltage is given by:

$$V_O = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2 \qquad (1)$$

Since the current from the adjustment terminal (I_{adj}) represents an error term in equation 1, the μA138 was designed to minimize I_{adj} and make it constant with line and load changes. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the μA138 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Load Regulation

The μA138 is capable of providing excellent load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

Figure 1 Basic Circuit Configuration

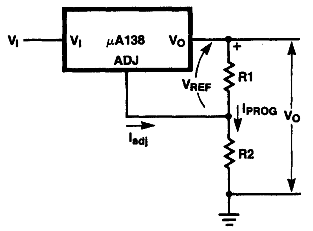
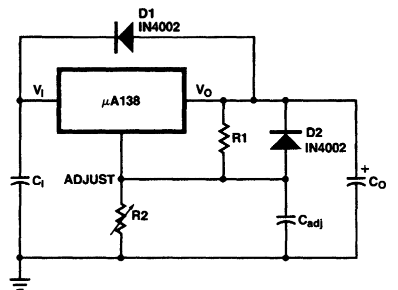


Figure 2 Voltage Regulator with Protection Diodes



External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_I) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection by 15 dB at 120 Hz in a 10 V application.

Although the μA138 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 2 shows the μA138 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values ($C_O > 25$ μF, $C_{adj} > 10$ μF).

Diode D1 prevents C_O from discharging through the IC during an input short circuit Diode D2 protects against capacitor C_{adj} discharging through the IC during an output short circuit. The combination of diodes D1 and D2 prevents C_{adj} from discharging through the IC during an input short circuit.

Figure 3a Adjustable Regulator with Improved Ripple Rejection

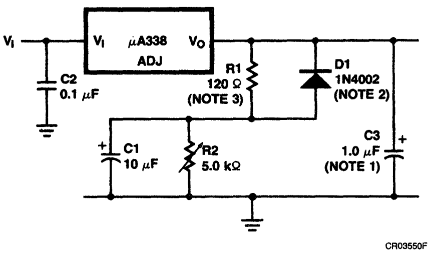


Figure 3b High Stability 10 V Regulator

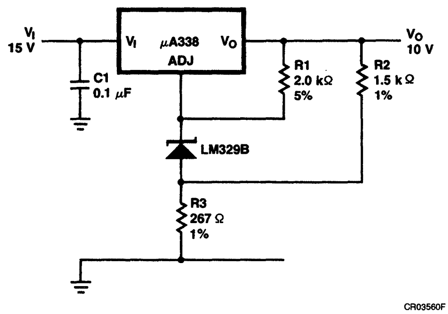


Figure 4 Adjustable Current Regulator

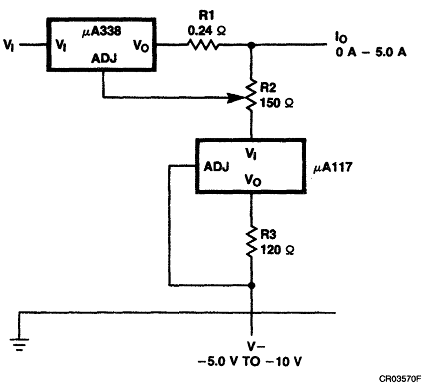
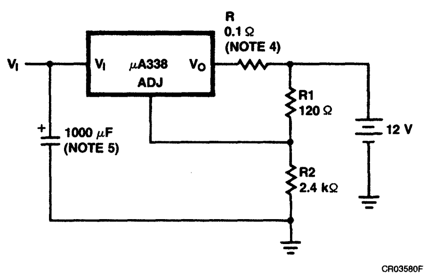


Figure 5 Simple 12 V Battery Charger



Notes

1. Solid tantalum.
2. Discharges C1 if output is shorted to ground.
3. R1 = 240 Ω for LM138 and LM238.
4. R_S — sets output impedance of charger $Z_O = R_S\left(1 + \frac{R2}{R1}\right)$ Use of R_S allows low charging rates with fully charged battery.
5. The 1000 μF is recommended to filter out input transients.

FAIRCHILD

A Schlumberger Company

μA150 • μA250 • μA350 3-Amp Positive Adjustable Regulators

Description

The μA150/μA250/μA350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3.0 A over a 1.2 V to 33 V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage.

A unique feature of the μA150 family is time dependent current-limiting. The current limit circuitry allows peak currents of up to 6.0 A to be drawn from the regulator for short periods of time. This allows the μA150 family to be used with heavy transient loads and speeds start up under full load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe-area protection for the power transistor. Overload protection remains functional even if the adjustment lead is accidentally disconnected.

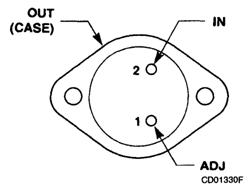
The μA150/μA250/μA350 are packaged in standard TO-3 transistor packages. The μA350 is also available in standard TO-220 transistor packages.

- **Guaranteed 3.0 A Output Current**
- **Output Adjustable Between 1.2 V and 33 V**
- **Load Regulation Typically 0.1%**
- **Line Regulation Typically 0.005%/V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation for High Voltage Applications**
- **Standard TO-3 and TO-220 Transistor Packages**
- **Available in Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to +150°C
Operating Junction Temperature Range	
Extended (μA150)	−55°C to +150°C
Industrial (μA250)	−25°C to +150°C
Commercial (μA350)	0°C to +150°C
Lead Temperature	
TO-3 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input/Output Voltage Differential	35 V

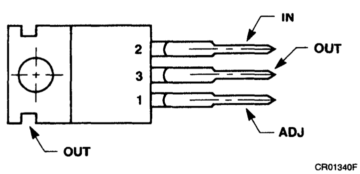
Connection Diagram TO-3 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA150KM	FT	Metal
μA250KV	FT	Metal
μA350KC	FT	Metal

Connection Diagram TO-220 Package (Top View)

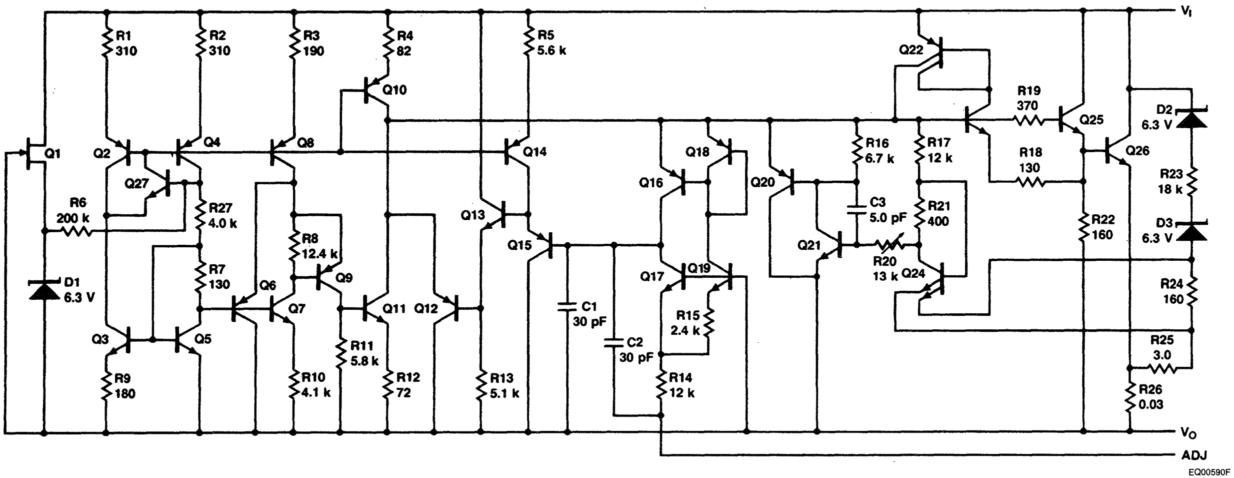


Lead 3 connected to case

Order Information

Device Code	Package Code	Package Description
μA350UC	GH	Molded Power Pack

Equivalent Circuit



µA150/µA250

Electrical Characteristics Unless otherwise specified, these specifications apply $-55°C \leq T_J \leq +150°C$ for the µA150, $-25°C \leq T_J \leq +150°C$ for the µA250, and $0°C \leq T_J \leq +150°C$ for the µA350, $V_I - V_O = 5.0$ V and $I_O = 1.5$ A. Although power dissipation is internally limited, these specifications are applicable for power dissipation up to 30 W, for TO-3; 25 W for TO-220.

Symbol	Characteristic	Conditions		Min	Typ	Max	Units
V_{REF}	Reference Voltage	$3.0 \leq V_I - V_O \leq 35$ V, 10 mA $\leq I_O \leq 3.0$ A, $P \leq 30$ W		1.20	1.25	1.30	V
$V_{R\ LINE}$	Line Regulation[1]	$T_A = 25°C$ 3.0 V $\leq V_I - V_O \leq 35$ V			0.005	0.01	%/V
		3.0 V $\leq V_I - V_O \leq 35$ V			0.02	0.05	%/V
$V_{R\ LOAD}$	Load Regulation[1]	$T_A = 25°C$ 10 mA $\leq I_O \leq 3.0$ A	$V_O \leq 5.0$ V		5.0	15	mV
			$V_O \geq 5.0$ V		0.1	0.3	% V_O
		10 mA $\leq I_O \leq 3.0$ A	$V_O \leq 5.0$ V		20	50	mV
			$V_O \geq 5.0$ V		0.3	1.0	% V_O
V_{RTH}	Thermal Regulation	Pulse = 20 ms			0.002	0.01	%/W
V_{DO}	Dropout Voltage	$T_A = 25°C$, $I_L \leq 3.0$ A, $V_I \leq 7.0$ V		3.0			V
I_{adj}	Adjustment Lead Current				50	100	µA
ΔI_{adj}	Adjustment Lead Current Change	10 mA $\leq I_L \leq 3.0$ A, 3.0 V $\leq V_I - V_O \leq 35$ V			0.2	5.0	µA
T_S	Temperature Stability	$T_{Min} \leq T_J \leq T_{Max}$			1.0		%
$I_{L\ Min}$	Minimum Load Current	$V_I - V_O = 35$ V			3.5	5.0	mA
I_L	Current Limit	$V_I - V_O \leq 10$ V		3.0	4.5		A
		$T_J = 25°C$, $V_I - V_O = 30$ V		0.3	1.0		A
N_O	Noise	$T_A = 25°C$, 10 Hz $\leq f \leq$ 10 kHz			0.001		% V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_O = 10$ V, f = 120 Hz	Without C_{adj}		65		dB
			$C_{adj} = 10$ µF	66	86		dB
S	Long Term Stability[2]	$T_A = 25°C$			0.3	1.0	%/1000 hrs

Notes

1. Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account separately by thermal regulation.
2. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

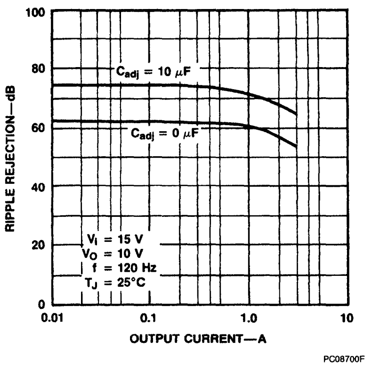
μA350
Electrical Characteristics Unless otherwise specified, these specifications apply $-55°C \leqslant T_J \leqslant +150°C$ for the μA150, $-25°C \leqslant T_J \leqslant +150°C$ for the μA250, and $0°C \leqslant T_J \leqslant +150°C$ for the μA350, $V_I - V_O = 5.0$ V and $t_O = 1.5$ A. Although power dissipation is internally limited, these specifications are applicable for power dissipation up to 30 W, for TO-3; 25 W for TO-220.

Symbol	Characteristic	Conditions		Min	Typ	Max	Units
V_{REF}	Reference Voltage	$3.0 \leqslant V_I - V_O \leqslant 35$ V, 10 mA $\leqslant I_O \leqslant 3.0$ A, $P \leqslant 30$ W		1.20	1.25	1.30	V
$V_{R\ LINE}$	Line Regulation[1]	$T_A = 25°C$ 3.0 V $\leqslant V_I - V_O \leqslant 35$ V			0.005	0.03	%/V
		3.0 V $\leqslant V_I - V_O \leqslant 35$ V			0.02	0.07	%/V
$V_{R\ LOAD}$	Load Regulation[1]	$T_A = 25°C$ 10 mA $\leqslant I_O \leqslant 3.0$ A	$V_O \leqslant 5.0$ V		5.0	25	mV
			$V_O \geqslant 5.0$ V		0.1	0.5	% V_O
		10 mA $\leqslant I_O \leqslant 3.0$ A	$V_O \leqslant 5.0$ V		20	70	mV
			$V_O \geqslant 5.0$ V		0.3	1.5	% V_O
V_{RTH}	Thermal Regulation	Pulse = 20 ms			0.002	0.03	%/W
V_{DO}	Dropout Voltage	$I_L \leqslant 3.0$ A, $V_I \leqslant 7.0$ V, $T_A = 25°C$		3.0			V
I_{adj}	Adjustment Lead Current				50	100	μA
ΔI_{adj}	Adjustment Lead Current Change	10 mA $\leqslant I_L \leqslant 3.0$ A 3.0 V $\leqslant V_I - V_O \leqslant 35$ V			0.2	5.0	μA
T_S	Temperature Stability	$T_{Min} \leqslant T_J \leqslant T_{Max}$			0.5		%
$I_{L\ Min}$	Minimum Load Current	$V_I - V_O = 35$ V			3.5	10	mA
I_L	Current Limit	$V_I - V_O \leqslant 10$ V		3.0	4.5		A
		$V_I - V_O = 30$ V, $T_J = 25°C$		0.25	1.0		A
N_O	Noise	$T_A = 25°C$ 10 Hz $\leqslant f \leqslant 10$ kHz			0.001		% V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_O = 10$ V, f = 120 Hz	Without C_{adj}		65		dB
			$C_{adj} = 10$ μF	66	86		
S	Long Term Stability[2]	$T_A = 25°C$			0.3	1.0	%/1000 hrs

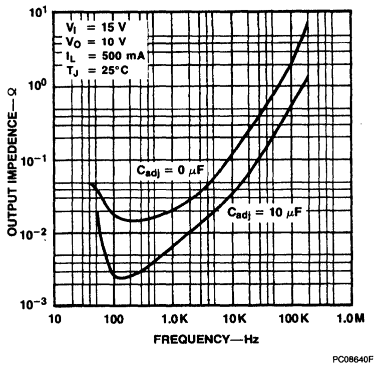
Notes
1. Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects are taken into account separately by thermal regulation.
2. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Typical Performance Curves

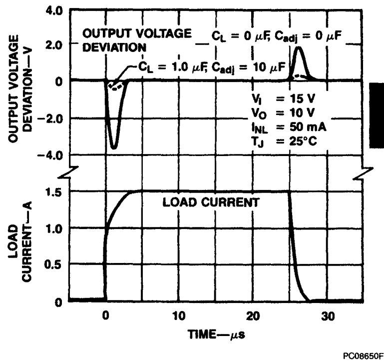
Ripple Rejection



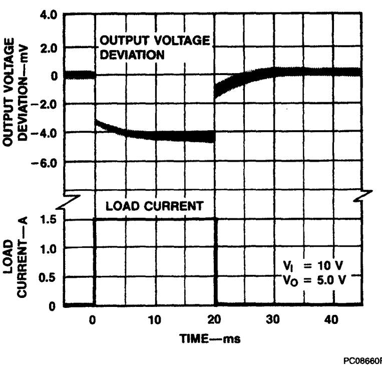
Output Impedance



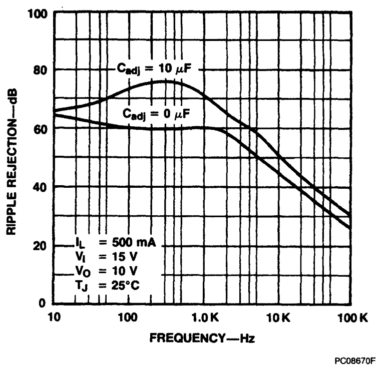
Load Transient Response



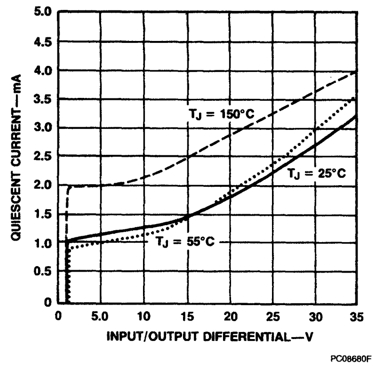
Thermal Regulation



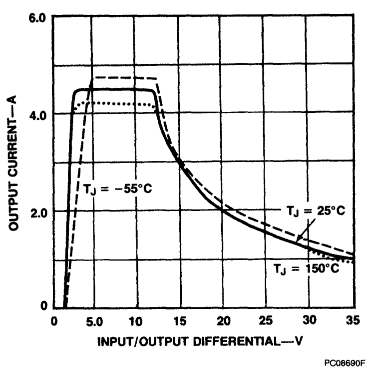
Ripple Rejection



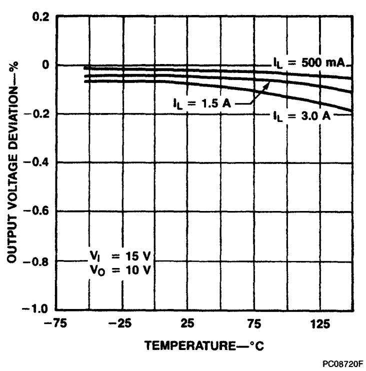
Minimum Operating Current



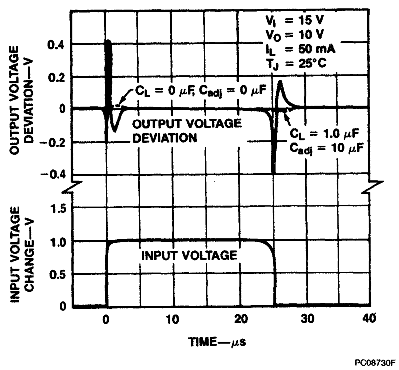
Current Limit



Load Regulation

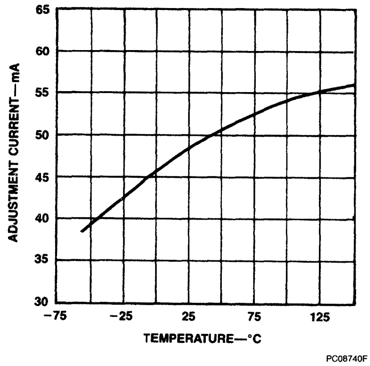


Line Transient Response

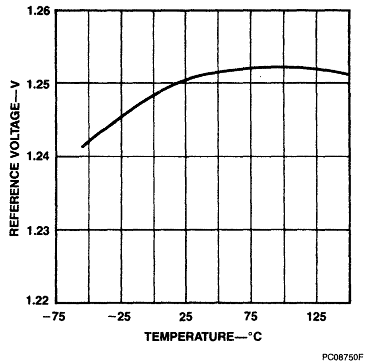


Typical Performance Curves (Cont.)

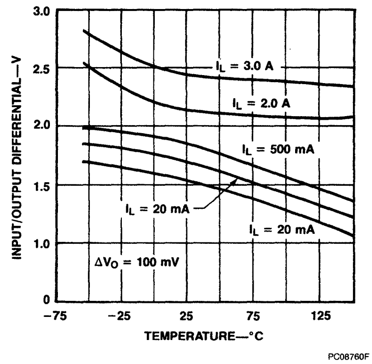
Adjustment Current



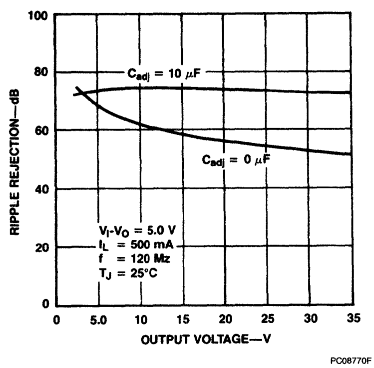
Temperature Stability



Dropout Voltage



Ripple Rejection



Design Considerations

To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC °C/W	Max θJC °C/W	Typ θJA °C/W	Max θJA °C/W
TO-3		1.5		35
TO-220	3.0	4.0		40

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\ Max}\ T_A}{\theta_{JA}}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$ (Without heat sink)

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

$= T_A + P_D\theta_{JA}$ (Without heat sink)

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction-to-Ambient Thermal Resistance
θ_{JC} = Junction-to-Case Thermal Resistance
θ_{CA} = Case-to-Ambient Thermal Resistance
θ_{CS} = Case-to-Heat Sink Thermal Resistance
θ_{SA} = Heat Sink-to-Ambient Thermal Resistance

Typical Applications

In operation, the μA150 develops a nominal 1.25 V reference voltage, V_{REF}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2, giving an output voltage of (*Figure 1*)

$$V_O = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{adj}R2 \quad (1)$$

Since the 50 μA current from the adjustment terminal represents an error term, the μA150 was designed to minimize I_{adj} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

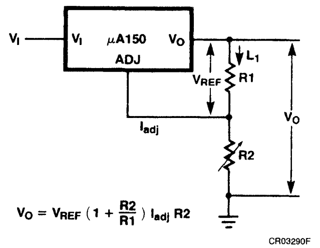
External Capacitors

An input bypass capacitor is recommended. A 0.1 μF disc or 1.0 μF solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used, but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the μA150 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10 μF bypass capacitor 88 dB ripple rejection is obtainable at any output level. Increases over 10 μF do not appreciably improve the ripple rejection at frequencies above 120 Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitor to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about 25 μF in aluminum electrolytic to equal 1.0 μF solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies, but some types have a large decrease in capacitance at frequencies around 0.5 MHz. For this reason, 0.01 μF disc may seem to work better than a 0.1 μF disc as a bypass.

Figure 1 Basic Circuit Configuration



Although the μA150 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values between 500 pF and 5000 pF. A 1.0 μF solid tantalum (or 25 μF aluminum electrolytic) on the output swamps this effect and insures stability.

Load Regulation

The μA150 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240 Ω) should be tied directly to the output of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15 V regulator with 0.05 Ω resistance between the regulator and load will have a load regulation due to line resistance of 0.05 Ω x 1_L. If the set resistor is connected near the load the effective line resistance will be 0.05 Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240 Ω set resistor.

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

6

Protection Diodes

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most 10 μF capacitors have low enough internal series resistance to deliver 20 A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of V_I. In the μA150, this discharge path is through a large junction that is able to sustain 25 A surge with no problem. This is not true of other types of positive regulators. For output capacitors of 25 μF or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the μA150 is a 50 Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25 V or less and 10 μF capacitance. *Figure 3* shows a μA150 with protection diodes included for use with outputs greater than 25 V and high values of output capacitance.

Figure 2 Voltage Regulator with Line Resistance in Output Lead

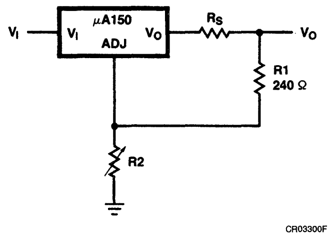
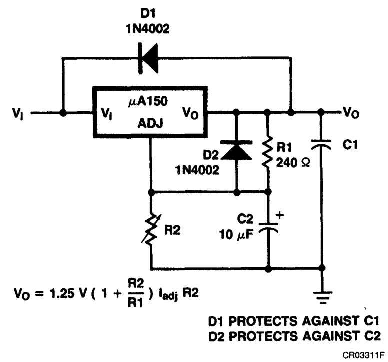
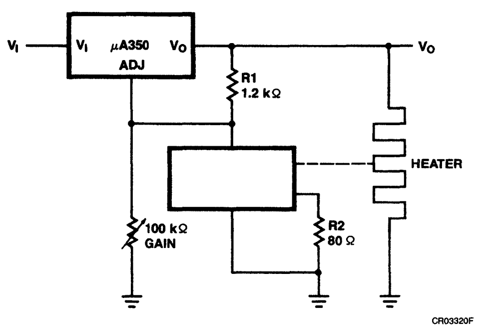


Figure 3 Voltage Regulator with Protection Diodes

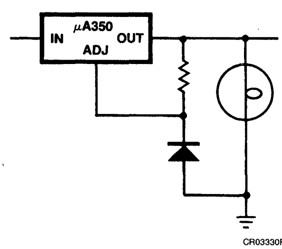


Typical Applications

Temperature Controller

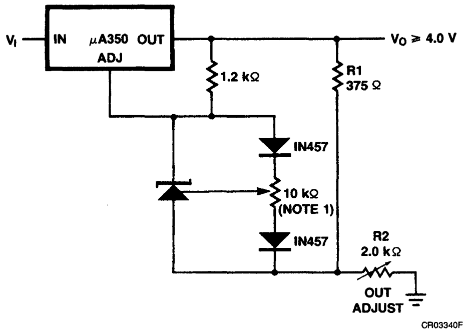


Light Controller

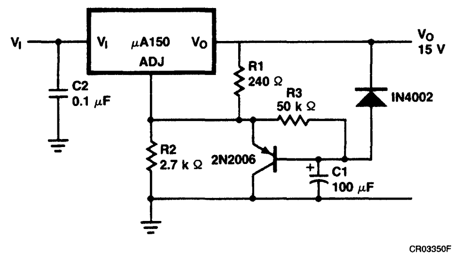


Typical Applications (Cont.)

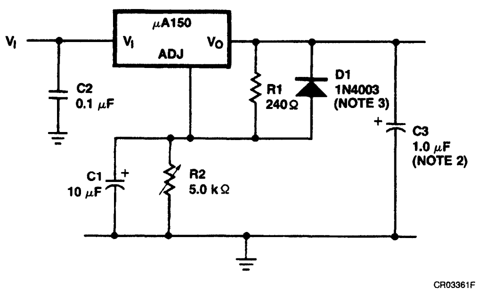
Precision Power Regulator with Low Temperature Coefficient



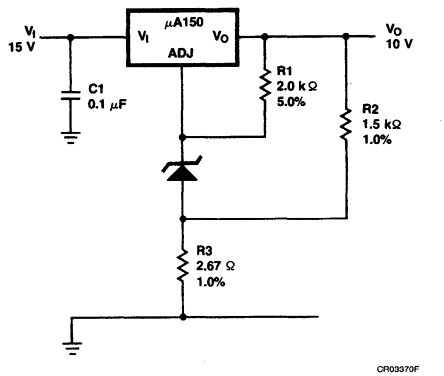
Slow Turn-On 15 V Regulator



Adjustable Regulator with Improved Ripple Rejection



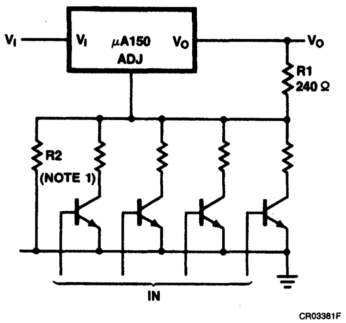
High Stability 10 V Regulator



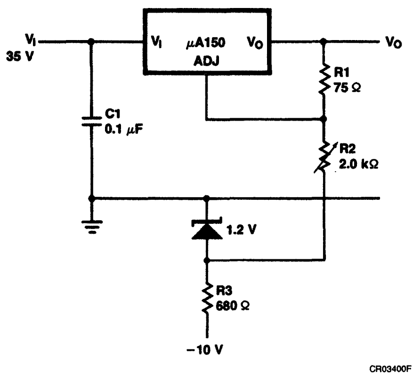
Notes
1. Adjust for 3.75 V across R1
2. Solid Tantalum
3. Discharge C1 if output is shorted to ground

Typical Applications (Cont.)

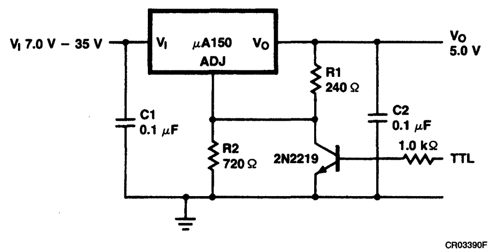
Digitally Selected Outputs



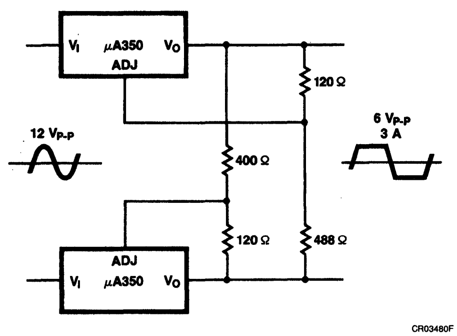
0 to 30 V Regulator



5 V Logic Regulator with Electronic Shutdown (Note 2)



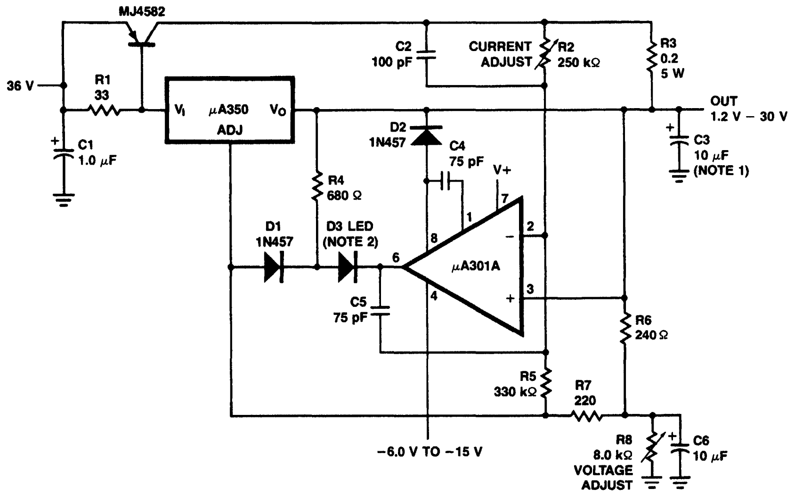
AC Voltage Regulator



Notes
1. Sets maximum V_O
2. Min output ≈ 1.2 V

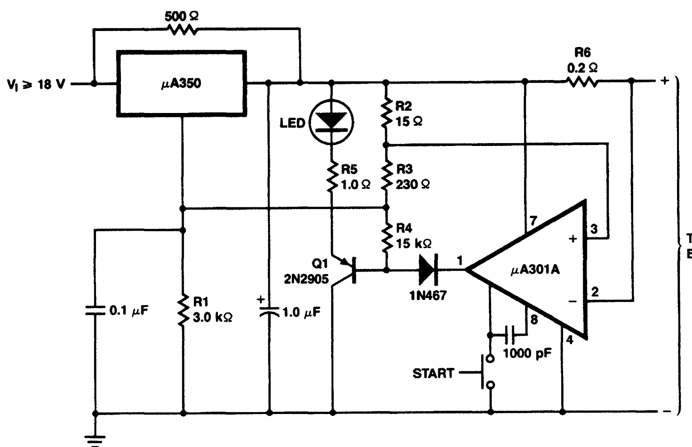
Typical Applications (Cont.)

5.0 A Constant Voltage/Constant Current Regulator



CR03411F

12 V Battery Charger



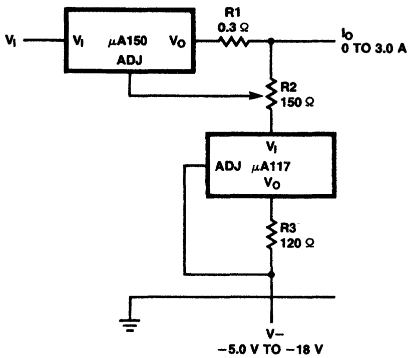
CR03421F

Notes

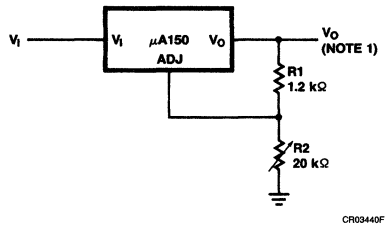
1. Solid tantalum
2. Lights in constant current mode

Typical Applications (Cont.)

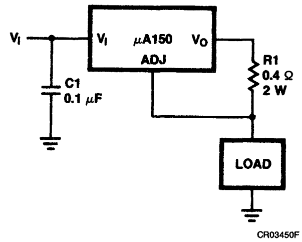
Adjustable Current Regulator



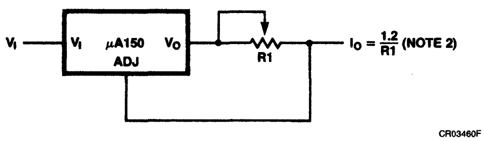
1.2 V — 20 V Regulator with Minimum Program Current



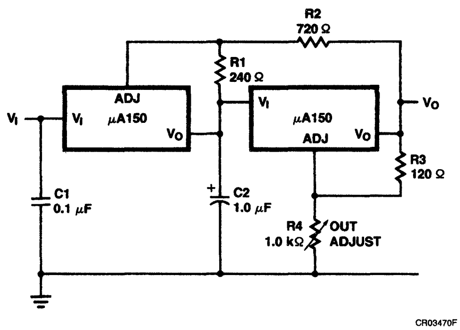
3.0 A Current Regulator



Precision Current Limiter



Tracking Pre-Regulator

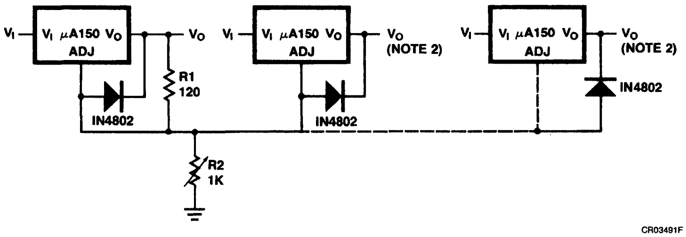


Notes

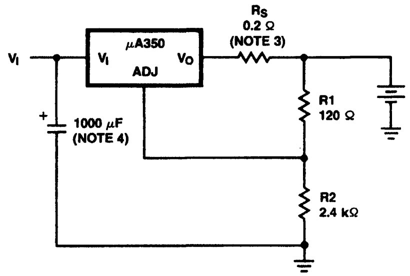
1. Minimum load current 4.0 mA
2. $0.4 \leqslant R1 \leqslant 120\ \Omega$

Typical Applications (Cont.)

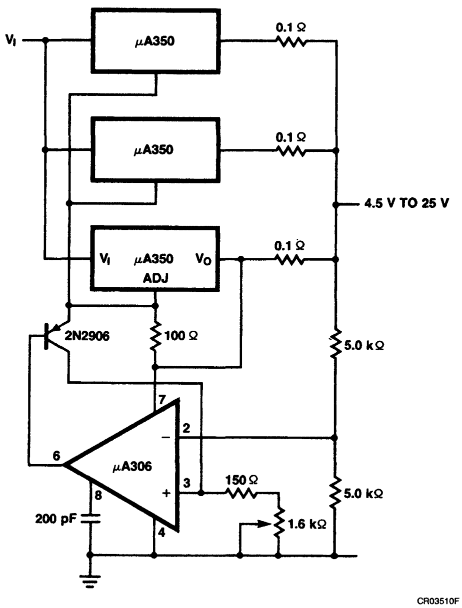
Adjusting Multiple On-Card Regulators with Single Control (Note 1)



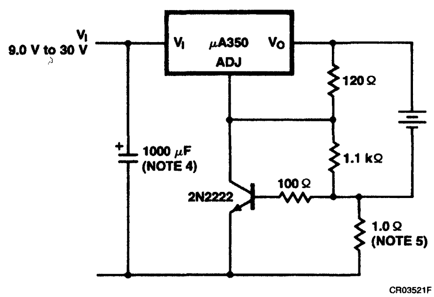
Simple 12 V Battery Charger



Adjustable 10 A Regulator



Current Limited 6.0 V Charger



Notes

1. All outputs within ±100 mV
2. Minimum load — 10 mA
3. R_S — sets output impedance of charger $Z_O = R_S\left(1 + \frac{R2}{R1}\right)$
   Use of R_S allows low charging rates with fully charged battery.
4. 1000 μF is recommended to filter out any input transients.
5. Sets peak current (2 A to 0.3 Ω)

FAIRCHILD

A Schlumberger Company

μA1524A • μA2524A • μA3524A Advanced Pulse Width Modulators

Linear Division Voltage Regulators

Description

The μA1524A family of regulating PWM ICs have been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The μA1524A family is lead compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the μA1524A family, however, frees the designer from many concerns which typically had required additional circuitry to solve.

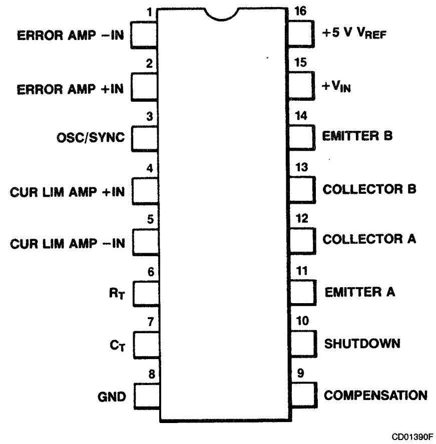
The μA1524A family includes a precise 5.0 V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5.0 V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60 V, 200 mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the μA1524A family is an undervoltage lockout circuit which disables all the internal circuitry except the reference, until the input voltage has risen to the turn-on threshold. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 300 mV of hysteresis for jitter-free activation.

Other product enhancements within the μA1524A family design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments; logic to eliminate double pulsing on a single output; and a 300 ns external shutdown capability. The oscillator circuit of the μA1524A family is usable beyond 500 kHz and is now easier to synchronize with an external clock pulse.

The μA1524A is packaged, in a hermetic 16-lead DIP and rated for operation from −55°C to +125°C. The μA2524A and μA3524A are available in either ceramic or plastic packages and are rated for operation from −25°C to +85°C and 0°C to 70°C respectively.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA1524ADM	7B	Ceramic DIP
μA2524ADV	7B	Ceramic DIP
μA2524APV	9B	Molded DIP
μA3524APC	9B	Molded DIP
μA3524ADC	7B	Ceramic DIP

- **Fully Interchangeable With Standard 1524 Families**
- **Precision Reference Internally Trimmed To ±1%**
- **High Performance Current Limit Function**
- **Under Voltage Lockout With Hysteristic Turn-On**
- **Start-Up Supply Current Less Than 4.0 mA**
- **Output Current To 200 mA**
- **60 V Output Capability**
- **Wide Common Mode Input Range For Both Error And Current Limit Amplifiers**
- **PWM Latch Ensures Single Pulse Per Period**
- **Double Pulse Suppression Logic**
- **300 ns Shutdown Through PWM Latch**
- **Guaranteed Frequency Accuracy**
- **Available In Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA1524A)	-55°C to +125°C
Industrial (μA2524A)	-25°C to +85°C
Commercial (μA3524A)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage	40 V
Collector Supply Voltage	60 V
Output Current (Each Output)	200 mA
Reference Output Current	50 mA
Oscillator Charging Current	5.0 mA

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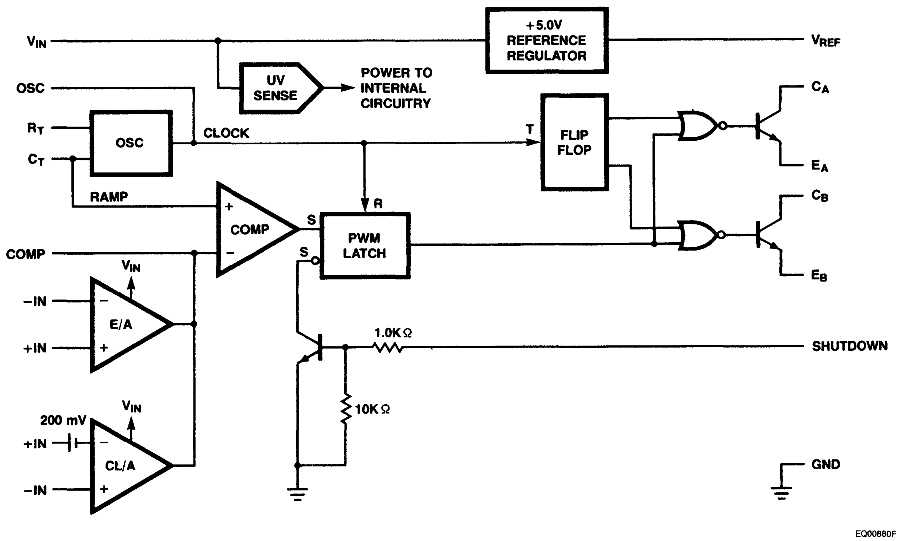
Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Equivalent Circuit



Power Dissipation at T_A = +25°C .... 1000 mW
Derate above +50°C .... 10 mW/°C
Power Dissipation at T_C = +25°C .... 2000 mW
Derate for Case Temperature above +25°C .... 16 mW/°C

μA1524, μA2524A, μA3524A
Electrical Characteristics $T_A = -55°C$ to $+125°C$ for the μA1524A, $-25°C$ to $+85°C$ for the μA2524A, and $0°C$ to $+70°C$ for the μA3524A, $V_I = V_C = 20$ V, unless otherwise specified.

Symbol	Characteristic	Conditions	μA1524A/μA2524A Min	Typ	Max	μA3524A Min	Typ	Max	Unit
Turn-on Characteristics									
V_O	Input Voltage	Operating Range after Turn-on	8.0		40	8.0		40	V
	Turn-on Threshold		5.5	7.5	8.5	5.5	7.5	8.5	V
	Turn-on Current	$V_I = 6.0$ V		2.5	4.0		2.5	4.0	mA
	Operating Current	$V_I = 8.0$ V to 40 V		6.0	10		6.0	10	mA
	Turn-on Hysteresis[1]			0.3			0.3		V
Reference Section									
V_O	Output Voltage	$T_J = 25°C$	4.95	5.0	5.05	4.90	5.0	5.10	V
$V_{R\ LINE}$	Line Regulation	$V_I = 10$ V to 40 V		10	20		10	30	mV
$V_{R\ LOAD}$	Load Regulation	$I_L = 0$ mA to 20 mA		5.0	50		5.0	50	mV
	Temperature Stability[1]	Over Operating Range		20	50		20	50	mV
I_{OS}	Output Short Circuit Current	$V_{REF} = 0$ V, $T_J = 25°C$		80	100		80	100	mA
N_O	Noise[1]	$10\ Hz \leq f \leq 10\ kHz$, $T_J = 25°C$		40			40		μV_{rms}
	Long Term Stability[1]	$T_J = 125°C$, 1000 Hrs		20	50		20	50	mV
Oscillator Section $R_T = 2700\ \Omega$, $C_T = 0.01$ mF, unless otherwise specified									
	Initial Accuracy	$T_J = 25°C$	41	43	45	39	43	47	kHz
	Temperature Stability[1]	Over Operating Temperature Range		2.0			2.0		%
	Minimum Frequency	$T_J = 25°C$, $R_T = 150\ k\Omega$, $C_T = 0.1$ mF			140			120	Hz
	Maximum Frequency	$T_J = 25°C$, $R_T = 2.0\ k\Omega$, $C_T = 470$ pF	500			500			kHz
	Output Amplitude[1]	$T_J = 25°C$		3.5			3.5		V
	Output Pulse Width[1]	$T_J = 25°C$		0.5			0.5		μs
	Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
	Ramp Valley	$T_J = 25°C$	0.6	0.75	0.9	0.6	0.75	0.9	V
Error Amplifier Section $V_{CM} = 2.5$ V, unless otherwise specified.									
$V_{IO}(EA)$	Input Offset Voltage			0.5	5.0		2.0	10	mV
I_{IB}	Input Bias Current			1.0	5.0		1.0	10	μA
I_{IO}	Input Offset Current			.05	1.0		0.5	1.0	μA

μA1524, μA2524A, μA3524A (Cont.)
Electrical Characteristics $T_A = -55°C$ to $+125°C$ for the μA1524A, $-25°C$ to $+85°C$ for the μA2524A, and $0°C$ to $+70°C$ for the μA3524A, $V_I = V_C = 20$ V, unless otherwise specified.

Symbol	Characteristic	Conditions	μA1524A/μA2524A Min	Typ	Max	μA3524A Min	Typ	Max	Unit
CMR	Common Mode Rejection	$V_{CM} = 1.5$ V to 5.5 V	60	75		60	75		dB
PSRR	Power Supply Rejection Ratio	$V_I = 10$ V to 40 V	50	60		50	60		dB
	Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
	Open Loop Voltage Gain	$\Delta V_O = 1.0$ V to 4.0 V, $R_L \geqslant 10$ MΩ	72	80		60	80		dB
	Gain Bandwidth[1]	$T_J = 25°C$, $A_v = 0$ dB	1.0	3.0		1.0	3.0		MHz
	DC Transconductance[1, 2]	$T_J = 25°C$, 30 kΩ $\leqslant R_L \leqslant$ 1.0 MΩ		1.6			1.6		mho
Current Limit Amplifier Lead 5 = 0 V, unless otherwise specified.									
V_{IO}	Input Offset Voltage	$T_J = 25°C$, E/A Set for maximum output	190	200	210	180	200	220	mV
V_{IO}	Input Offset Voltage	Over Operating Temperature Range	180		220	170		230	mV
I_{IB}	Input Bias Current			−1.0	−10		−1.0	−10	μA
CMR	Common Mode Rejection	$V_{Lead\ 5} = -0.2$ V to +5.5 V	50	60		50	60		dB
PSRR	Power Supply Rejection Ratio	$V_I = 10$ V to 40 V	50	60		50	60		dB
	Output Swing	Minimum Total Range	0.5		5.0	0.5		5.0	V
	Open Loop Voltage Gain	$V_O = 1.0$ V to 4.0 V, $R_L \geqslant 10$ MΩ	70	80		70	80		dB
	Delay Time[1]	Lead 4 to Lead 9, $\Delta V_I = 300$ mV		300			300		ns
Output Section (Each Output)									
V_{CE}	Collector Emitter Voltage	$I_C = 100$ μA	60	80		50	80		V
I_{CE}	Collector Leakage Current	$V_{CE} = 50$ V		0.1	20		0.1	20	μA
$V_{CE\ Sat}$	Saturation Voltage	$I_C = 20$ mA		0.2	0.4		0.2	0.4	V
		$I_C = 100$ mA		1.0	1.5		1.0	1.5	
		$I_C = 200$ mA		2.0	2.7		2.0	2.5	
V_E	Emitter Output Voltage	$I_E = 50$ mA	17	18		17	18		V
t_r	Rise Time[1]	$T_J = 25°C$, R = 2.0 kΩ		150			150		ns
t_f	Fall Time[1]	$T_J = 25°C$, R = 2.0 kΩ		50			50		ns

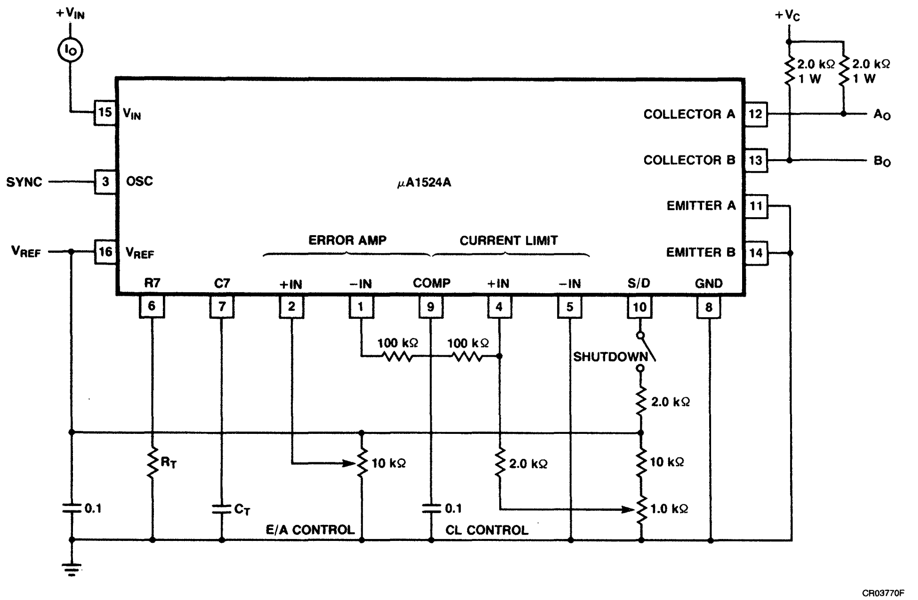
6

μA1524, μA2524A, μA3524A (Cont.)
Electrical Characteristics $T_A = -55°C$ to $+125°C$ for the μA1524A, −25°C to +85°C for the μA2524A, and 0°C to +70°C for the μA3524A, $V_I = V_C = 20$ V, unless otherwise specified.

			μA1524A/μA2524A			μA3524A			
Symbol	**Characteristic**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
	Comparator Delay[1]	$T_J = 25°C$, Lead 9 to Output		350			350		ns
	Shutdown Delay[1]	$T_J = 25°C$, Lead 10 to Output		300			300		ns
	Shutdown Threshold	$T_J = 25°C$, $R_C = 2.0$ kΩ	0.6	0.7	1.0	0.6	0.7	1.0	V

Notes
1. These parameters are guaranteed by design but not 100% tested in production.
2. DC transconductance (g_M) relates to DC open loop voltage gain according to the following equation: $A_v = g_M R_L$ where R_L is the resistance from lead 9 to ground. The minimum g_M specification is used to calculate minimum A_v when the error amplifier output is loaded.

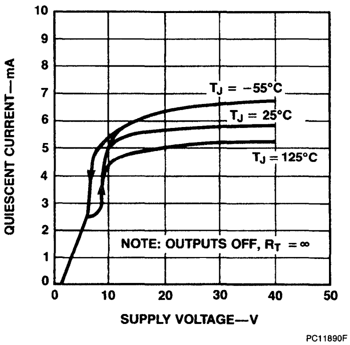
Open Loop Test Circuit (Note 1, 2)



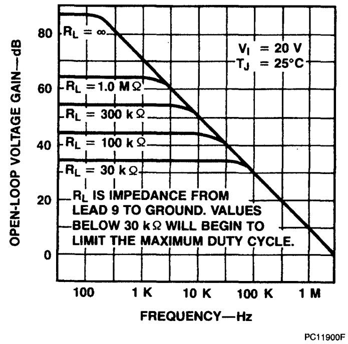
Notes
1. The μA1524A should be able to be tested in any 1524 test circuit with two possible exceptions.
   a. The higher gain bandwidth of the current limit amplifier in the μA1524A may cause oscillations in an uncompensated 1524 test circuit.
   b. The effect of the shutdown, lead 10, cannot be seen at the compensation terminal, lead 9; but must be observed at the outputs.
2. The circuit will allow all μA1524A functions to be evaluated.

Typical Performance Curves

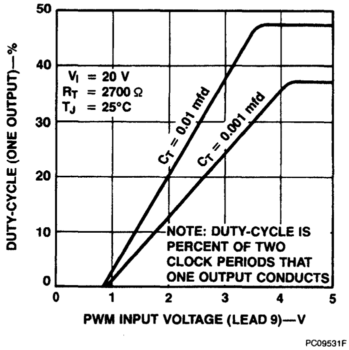
Supply Current vs Voltage



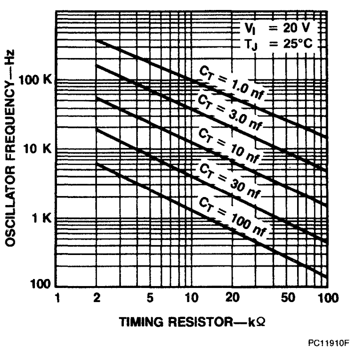
Error Amplifier Voltage Gain vs Frequency



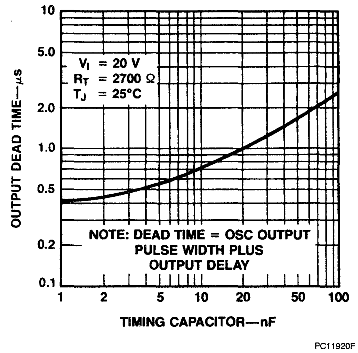
Pulse Width Modulator Transfer Function



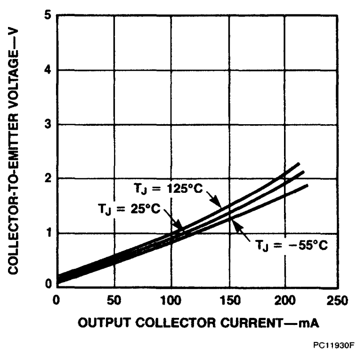
Oscillator Frequency vs Timing Components



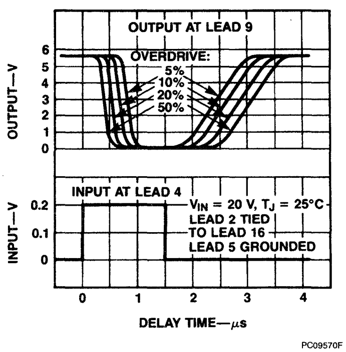
Output Dead Times vs Timing Capacitor Value



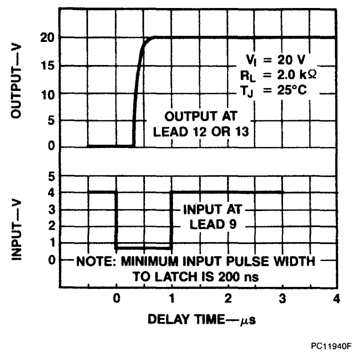
Output Saturation Voltage



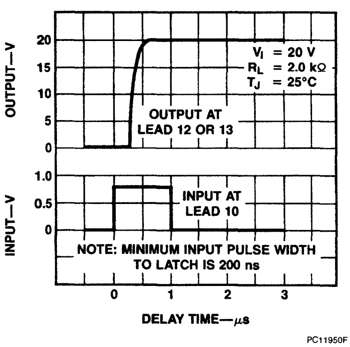
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator — Lead 9



Turn-Off Delay From Shutdown — Lead 10



FAIRCHILD
A Schlumberger Company

μA431A Adjustable Precision Zener Shunt Regulator

Linear Division Voltage Regulators

Description

The μA431A is a 3-terminal adjustable shunt regulator with guaranteed temperature stability over the entire temperature range of operation. The output voltage may be set at any level greater than 2.5 V (V_{REF}) up to 36 V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.

- **Average Temperature Coefficient 50 ppm/°C**
- **Temperature Compensated For Operation Over The Full Temperature Range**
- **Programmable Output Voltage**
- **Fast Turn-On Response**
- **Low Output Noise**

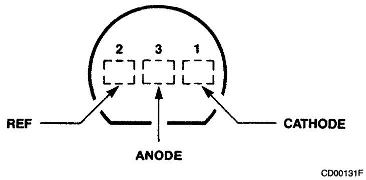
Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial (μA431AV)	−40°C to +85°C
Commercial (μA431AC)	0°C to +70°C
Lead Temperature	
TO-92 Package/SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
TO-92 Package	0.78 W
SO-8 Package	0.81 W
Cathode Voltage	37 V
Continuous Cathode Current	−10 mA to +150 mA
Reference Voltage	−0.5 V
Reference Input Current	10 mA

Operating Conditions	Min	Max
Cathode Voltage	V_{REF}	37 V
Cathode Current	1.0 mA	100 mA

Notes
1. $T_{J\ Max} = 150°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the TO-92 at 6.2 mW/°C, and the S0-8 at 6.5 mW/°C.

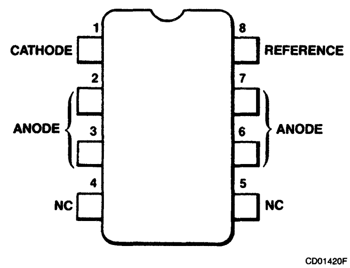
Connection Diagram
TO-92 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA431AWC	EI	Molded
μA431AWV	EI	Molded

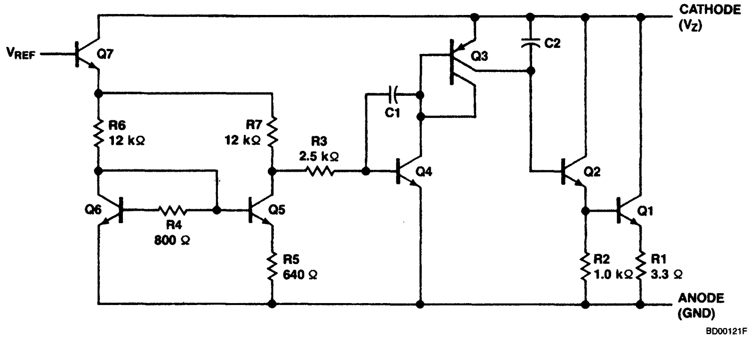
Connection Diagram
SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA431ASC	KC	Molded Surface Mount

Equivalent Circuit



DC Test Circuits

Figure 1 Test Circuit For $V_Z = V_{REF}$

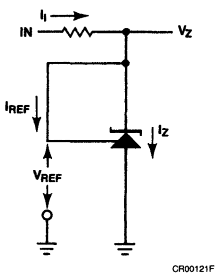


Figure 2 Test Circuit For $V_Z > V_{REF}$

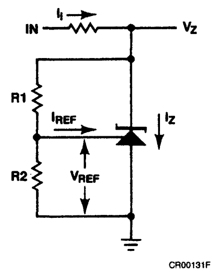
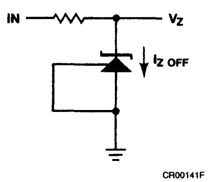


Figure 3 Test Circuit For Off-State Current



Note

$V_Z = V_{REF}\ (1 + R1/R2) + I_{REF} \cdot R1$

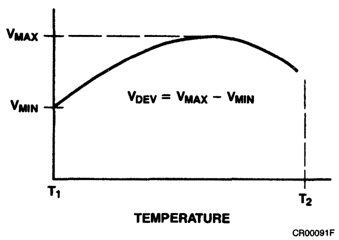
μA431A

Electrical Characteristics $T_A = 25°C$ unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{REF}	Reference Voltage	$V_Z = V_{REF}$, $I_I = 10$ mA, Fig. 1		2.440	2.495	2.550	V
V_{DEV}	Deviation of Reference Input Voltage Over Temperature[1]	$V_Z = V_{REF}$, $I_I = 10$ mA, T_A = full range, Fig. 1			8.0	17	mV
$\frac{\Delta V_{REF}}{\Delta V_Z}$	Ratio of the Change in Reference Voltage to the Change in Cathode Voltage	$I_Z = 10$ mA, Fig. 2	V_Z from V_{REF} to 10 V		−1.4	−2.7	mV/V
			V_Z from 10 V to 36 V		−1.0	−2.0	
I_{REF}	Reference Input Current	$R_1 = 10$ kΩ, $R_2 = \infty$, $I_I = 10$ mA, Fig. 2			2.0	4.0	μA
$\propto I_{REF}$	Deviation of Reference Input Current over Temperature	$R_1 = 10$ kΩ, $R_2 = \infty$, $I_I = 10$ mA, T_A = Full Range, Fig. 2			0.4	1.2	μA
$I_{Z(MIN)}$	Minimum Cathode Current for Regulation	$V_Z = V_{REF}$, Fig. 1			0.4	1.0	mA
$I_{Z(OFF)}$	Off-State Current	$V_Z = 36$ V, $V_{REF} = 0$ V, Fig. 3			0.3	1.0	μA
r_Z	Dynamic Output Impedance[2]	$V_Z = V_{REF}$, Frequency = 0 Hz, Fig. 1				.75	Ω

Notes

1. Deviation of reference input voltage, V_{DEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.



The average temperature coefficient of the reference input voltage, $\propto$VREF, is defined as:

$$\propto V_{REF}\frac{ppm}{°C} = \pm\frac{\left[\frac{V_{Max}-V_{Min}}{V_{REF}\text{ (at 25°C)}}\right]10^6}{T_2-T_1} = \pm\frac{\left[\frac{V_{DEV}}{V_{REF}\text{ (at 25°C)}}\right]10^6}{T_2-T_1}$$

Where:
$T_2 - T_1$ = full temperature change.

$\propto V_{REF}$ can be positive or negative depending on whether the slope is positive or negative.

Example: $V_{DEV} = 8.0$ mV, $V_{REF} = 2495$ mV, $T_2 - T_1 = 70°C$, slope is positive

$$\propto V_{REF} = \frac{\left[\frac{8.0\text{ mV}}{2495\text{ mV}}\right]10^6}{70°C} = +46\text{ ppm/°C}$$

2. The dynamic output impedance, r_Z, is defined as:

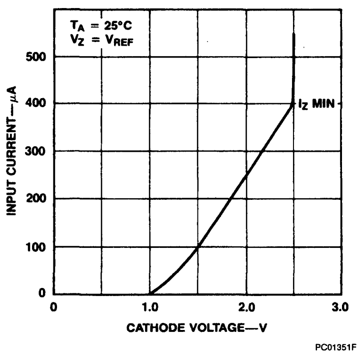
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}$$

When the device is programmed with two external resistors, R1 and R2, (*see Figure 2*), the dynamic output impedance of the overall circuit, r_Z, is defined as:

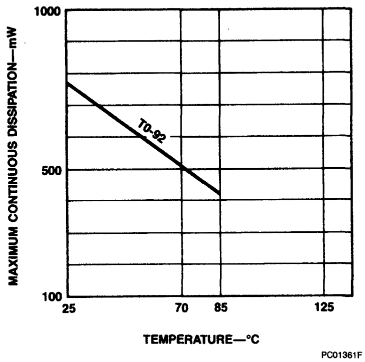
$$r_Z = \frac{\Delta V_Z}{\Delta I_Z} \cong \left[r_Z\ 1 + \frac{R1}{R2}\right]$$

Typical Performance Curves

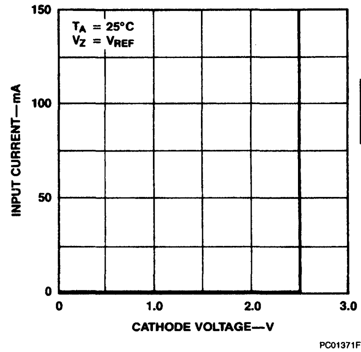
Input Current vs V_Z



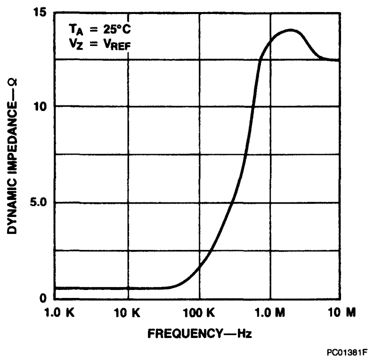
Thermal Information

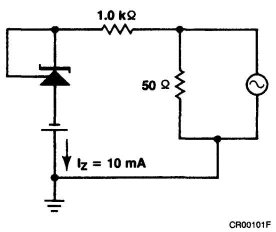


Input Current vs V_Z

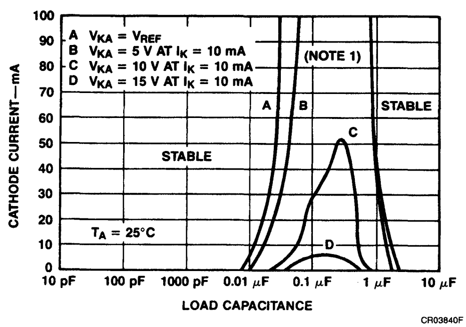


Dynamic Impedance vs Frequency





Stability Boundary Conditions



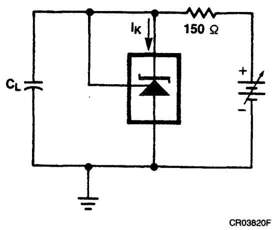
Note

1. The areas under the curves represent conditions that may cause the device to oscillate. For curves B, C, and D, R2 and V+ were adjusted to establish the initial V_{KA} and I_K conditions with $C_L = 0$. V+ and C_L were then adjusted to determine the ranges of stability.

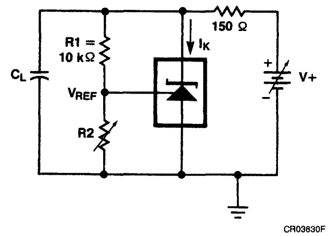
6

Typical Characteristics

Test Circuit For Curve A Below

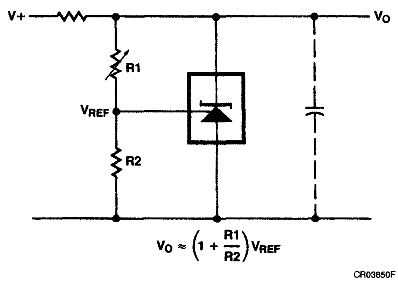


Test Circuit for Curves B, C, And D Below

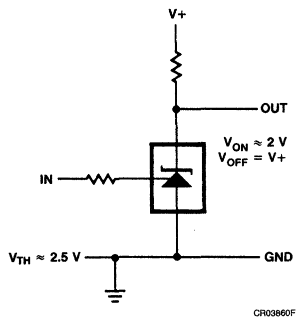


Typical Applications

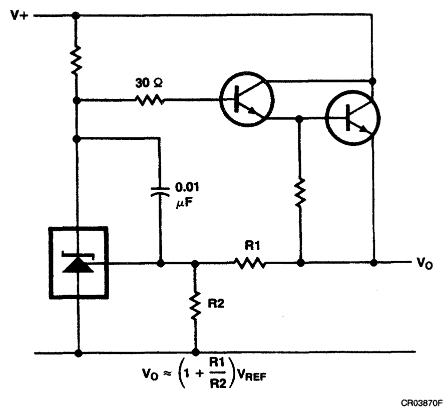
Shunt Regulator



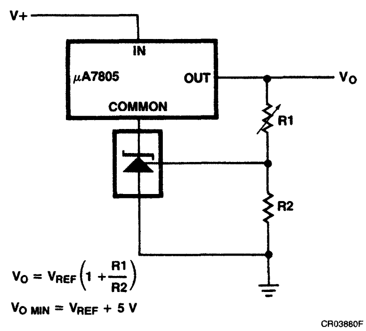
Single Supply Comparator With Temperature Compensated Threshold



Series Regulator

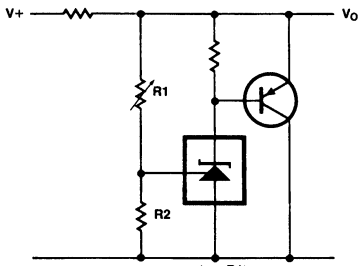


Output Control of a Three Terminal Fixed Regulator



Typical Applications (Cont.)

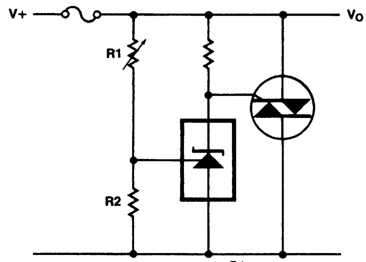
Higher Current Shunt Regulator



$$V_O = \left(1 + \frac{R1}{R2}\right)V_{REF}$$

CR03890F

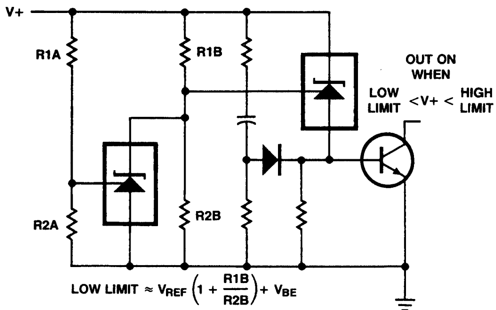
Crow Bar



$$V_{LIMIT} \approx \left(1 + \frac{R1}{R2}\right)V_{REF}$$

CR03900F

Over Voltage/Under Voltage Protection Circuit

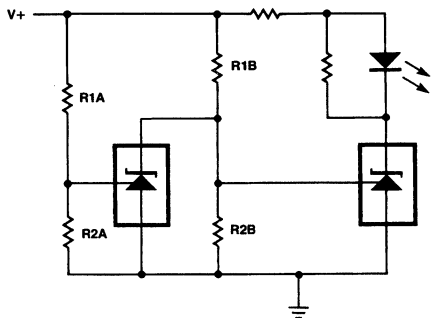


$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right) + V_{BE}$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

CR03910F

Voltage Monitor



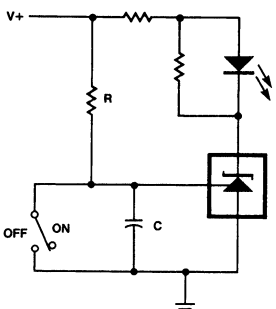
$$\text{LOW LIMIT} \approx V_{REF}\left(1 + \frac{R1B}{R2B}\right)$$

$$\text{HIGH LIMIT} \approx V_{REF}\left(1 + \frac{R1A}{R2A}\right)$$

LED ON WHEN
LOW LIMIT <V+ < HIGH LIMIT

CR03920F

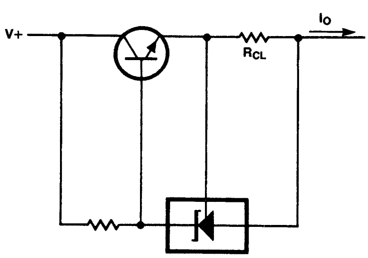
Delay Timer



$$\text{DELAY} = R \cdot C \cdot \text{IN}\ \frac{V+}{(V+) - V_{REF}}$$

CR03930F

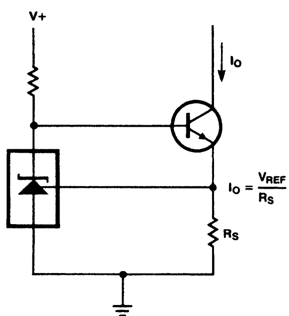
Current Limiter Or Current Source



$$I_O = \frac{V_{REF}}{R_{CL}}$$

CR03940F

Constant Current Sink



CR03950F

6

FAIRCHILD

A Schlumberger Company

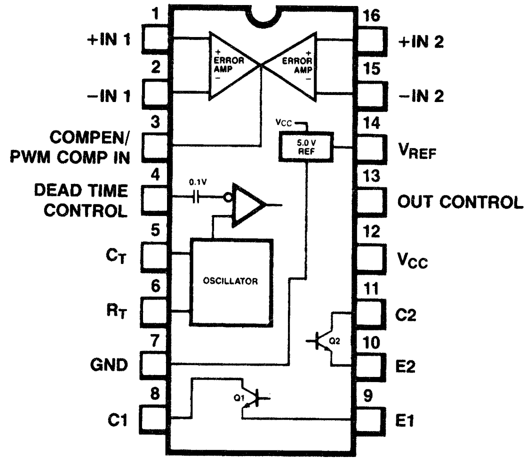
μA494
Pulse Width Modulated Control Circuit

Description

The μA494 is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulated (PWM) switching power supplies, including push-pull, bridge and series configurations. The device can operate at switching frequencies between 1.0 kHz and 300 kHz and output voltages up to 40 V. The operating temperature range specified for the μA494C is 0°C to 70°C and for the μA494V is −40°C to +85°C.

- **Uncommitted Output Transistors Capable Of 200 mA Source Or Sink**
- **On-Chip Error Amplifiers**
- **On-Chip 5.0 V Reference**
- **Internal Protection From Double Pulsing Of Outputs With Narrow Pulse Widths Or With Supply Voltages Below Specified Limits**
- **Dead Time Control Comparator**
- **Output Control Selects Single Ended Or Push-Pull Operation**
- **Easily Synchronized (Slaved) To Other Circuits**

Connection Diagram
16-Lead DIP
(Top View)

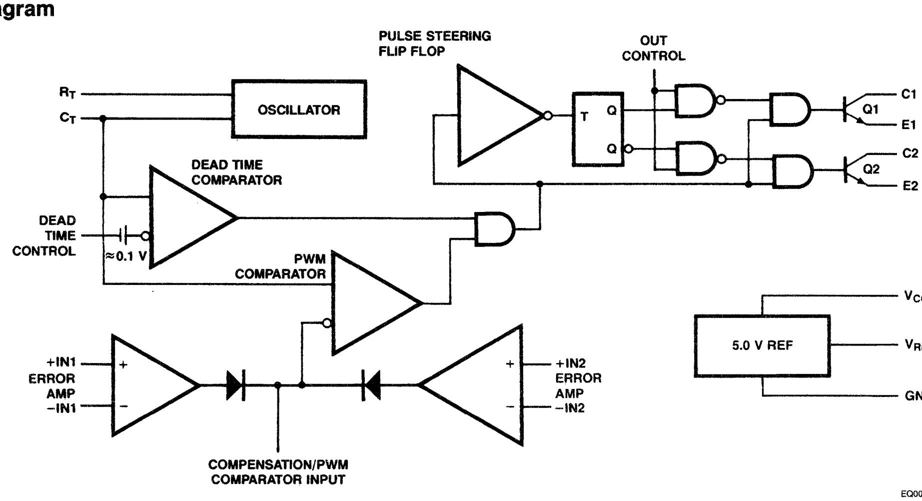


CD01320F

Order Information

Device Code	Package Code	Package Description
μA494PV	9B	Molded DIP
μA494DC	7B	Ceramic DIP
μA494PC	9B	Molded DIP

Block Diagram



EQ00580F

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Industrial (μA494V)	−40°C to +85°C
Commercial (μA494C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage	42 V
Voltage From Any Lead to Ground (except lead 8 and lead 11)	V_{CC} + 0.3 V
Output Collector Voltage	42 V
Peak Collector Current (I_{C1} and I_{C2})	250 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

6

Functional Description

The basic oscillator (switching) frequency is controlled by an external resistor (R_T) and capacitor (C_T). The relationship between the values of R_T, C_T and frequency is shown in *Figure 10.*

The level of the sawtooth wave form is compared with an error voltage by the pulse width modulated comparator. The output of the PWM Comparator directs the pulse steering flip-flop and the output control logic.

The error voltage is generated by the error amplifier. The error amplifier boosts the voltage difference between the output and the 5.0 V internal reference. *See Figure 7* for error amp sensing techniques. The second error amp is typically used to implement current-limiting.

The output control logic selects either push-pull or single ended operation of the output transistors (*see Figure 6*).

The dead time control prevents on-state overlap of the output transistors as can be seen in *Figure 5.* The dead time is approximately 3.0 or 5.0% of the total period if the dead time control is grounded. This dead time can be increased by connecting the dead time control to a voltage up to 5.0 V.

The frequency response of the error amps (*Figure 11*) can be modified by using external resistors and capacitors. These components are typically connected between the compensation terminal and the inverting input of the error amps.

The switching frequency of two or more μA494 circuits can be synchronized. The timing capacitor, C_T is connected as shown in *Figure 8.* Charging current is provided by the master circuit. Discharging is through all the circuits slaved to the master. R_T is required only for the master circuit.

Recommended Operating Conditions

Symbol	Characteristic	μA494 Min	μA494 Max	Unit
V_{CC}	Power Supply Voltage	7.0	40	V
V_I	Voltage on Any Lead Except Leads 8 and 11 (Referenced to Ground)	−0.3	V_{CC} + 0.3	V
V_{C1}, V_{C2}	Output Voltage Collector	−0.3	40	V
I_{C1}, I_{C2}	Output Collector Current		200	mA
C_T	Timing Capacitor	470		pF
			10	μF
R_T	Timing Resistor	1.8	500	kΩ
f_{osc}	Oscillator Frequency	1.0	300	kHz
T_A	Operating Temperature Range	0	+70	°C

μA494

Electrical Characteristics $T_A = 0$ to 70°C for the μA494C, $T_A = -40$°C to +85°C for the μA494V, $V_{CC} = 15$ V, $f_{osc} = 10$ kHz, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
Reference Section							
V_{REF}	Reference Voltage[1]	$I_{REF} = 1.0$ mA		4.75	5.0	5.25	V
Reg_{LINE}	Line Regulation of Reference Voltage	$7.0\ V \leqslant V_{CC} \leqslant 40\ V$			2.0	25	mV
TCV_{REF}	Temperature Coefficient of Reference Voltage	$0°C \leqslant T_A \leqslant 70°C$			0.01	0.03	%/°C
Reg_{LOAD}	Load Regulation of Reference Voltage	$1.0\ mA \leqslant I_{REF} \leqslant 10\ mA$			1.0	15	mV
I_{OS}	Output Short Circuit Current	$V_{REF} = 0$ V	$0°C \leqslant T_A \leqslant +70°C$	10	35	50	mA
			$-40°C \leqslant T_A \leqslant +85°C$		35		
Oscillator Section							
f_{osc}	Oscillator Frequency *(Figure 10)*	$C_T = 0.01$ μF, $R_T = 12$ kΩ			10		kHz
Δf_{osc}	Oscillator Frequency Change	$C_T = 0.01$ μF, $R_T = 12$ kΩ	$0°C \leqslant T_A \leqslant +70°C$			2.0	%
			$-40°C \leqslant T_A \leqslant +85°C$			2.0	
Dead Time Control Section							
$I_{IB(DT)}$	Input Bias Current	$V_{CC} = 15$ V, $0\ V \leqslant V_4 \leqslant 5.25\ V$			−2.0	−10	μA
$DC_{(max)}$	Maximum Duty Cycle, Each Output	$V_{CC} = 15$ V, Lead 4 = 0 V, Output Control = V_{REF}		45			%
$V_{TH(in)}$	Input Threshold Voltage	Zero Duty Cycle			3.0	3.3	V
		Maximum Duty Cycle		0			
Error Amplifier Sections							
V_{IO}	Input Offset Voltage	$V_3 = 2.5$ V			2.0	10	mV
I_{IO}	Input Offset Current	$V_3 = 2.5$ V			25	250	nA
I_{IB}	Input Bias Current	$V_3 = 2.5$ V			0.2	1.0	μA
V_{ICR}	Input Common Mode Voltage Range	$7.0\ V \leqslant V_{CC} \leqslant 40\ V$		−0.3		V_{CC}	V
A_{VS}	Large Signal Voltage Gain	$0.5\ V \leqslant V_3 \leqslant 3.5\ V$		60	74		dB
BW	Bandwidth				650		kHz
PWM Comparator Section (*Figure 9*)							
V_{THI}	Inhibit Threshold Voltage	Zero Duty Cycle			4.0	4.5	V
I_O-	Output Sink Current[2]	$0.5\ V \leqslant V_3 \leqslant 3.5\ V$		−0.2	−0.6		mA
I_O+	Output Source Current[2]	$0.5\ V \leqslant V_3 \leqslant 3.5\ V$		2.0			mA

μA494 (Cont.)
Electrical Characteristics $T_A = 0$ to 70°C for the μA494C, $T_A = -40$°C to +85°C for the μA494V, $V_{CC} = 15$ V, $f_{osc} = 10$ kHz, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
Output Section							
$V_{CE(sat)}$	Output Saturation VoltageCommon Emitter Configuration, (*Figure 3*)	$V_E = 0$ V, $I_C = 200$ mA	0°C ≤ T_A ≤ +70°C −40°C ≤ T_A ≤ +85°C		1.1	1.3	V
	Emitter Follower Configuration, (*Figure 4*)	$V_C = 15$ V, $I_E = 200$ mA			1.5	2.5	
$I_{C(off)}$	Collector Off-State Current	$V_{CC} = 40$ V, $V_{CE} = 40$ V			2.0	100	μA
$I_{E(off)}$	Emitter Off-State Current	$V_{CC} = V_C = 40$ V, $V_E = 0$	0°C ≤ T_A ≤ +70°C, −40°C ≤ T_A ≤ +85°C			−100	μA
Output Control (*Figure 6*)							
V_{OCL}	Output Control Voltage Required for Single Ended or Parallel Output Operation					0.4	V
V_{OCH}	Output Control Voltage Required for Push-Pull Operation			2.4			V
Total Device							
I_{CC}	Standby Power Supply Current				6.0	10	mA
Output AC Characteristics Use Recommended Operating Conditions with $T_A = 25$°C							
t_r	Rise Time of Output Voltage Common Emitter Configuration, (*Figure 3*)				100	200	ns
	Emitter Follower Configuration, (*Figure 4*)				100	200	
t_f	Fall Time of Output Voltage Common Emitter Configuration, (*Figure 3*)				25	100	ns
	Emitter Follower Configuration, (*Figure 4*)				40	100	

Notes
1. Selected devices with tightened tolerance reference voltage available.
2. These limits apply when the voltage measured at Lead 3 is within the range specified.

Test Circuits

Figure 1 Error Amplifier Test Circuit

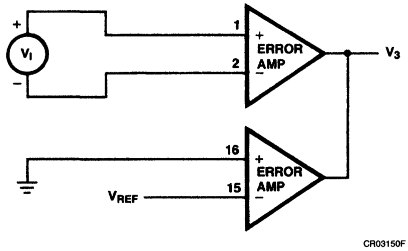


Figure 2 Current Limit Sense Amplifier Test Circuit

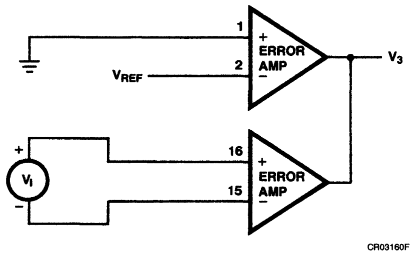


Figure 3 Common Emitter Configuration Test Circuit and Waveform

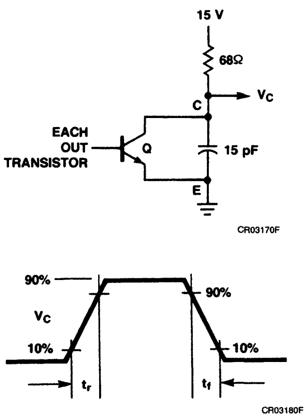


Figure 4 Emitter Follower Configuration Test Circuit and Waveform

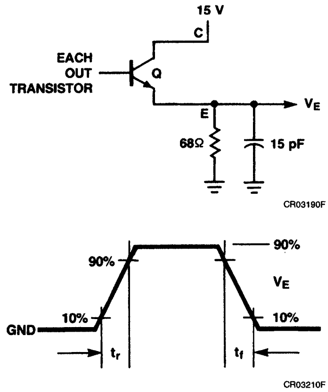
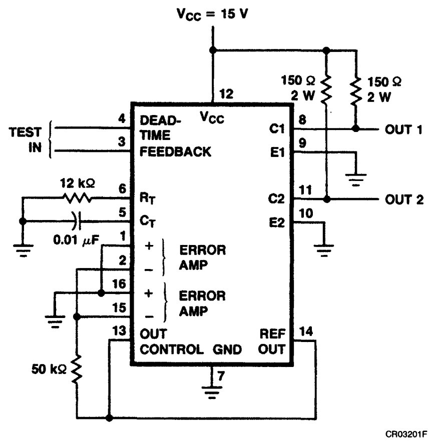


Figure 5 Dead Time and Feedback Control Test Circuit



6

Typical Applications

Figure 6 Output Connections for Single Ended and Push-Pull Configurations

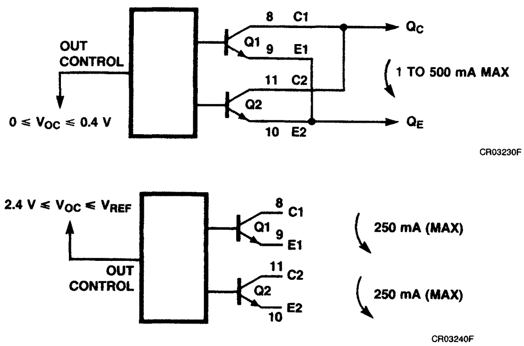


Figure 7 Error Amplifier Sensing Techniques

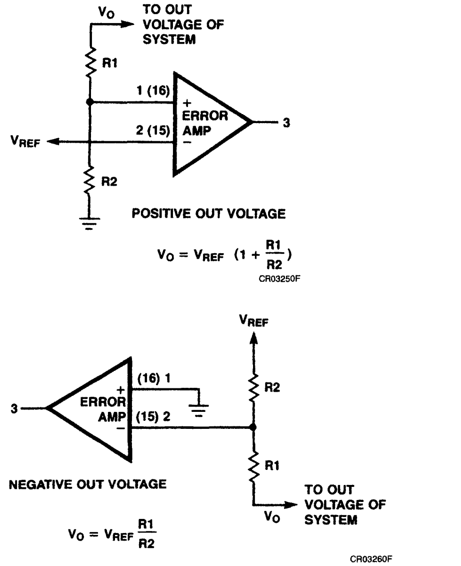


Figure 8 Slaving Two or More Control Circuits

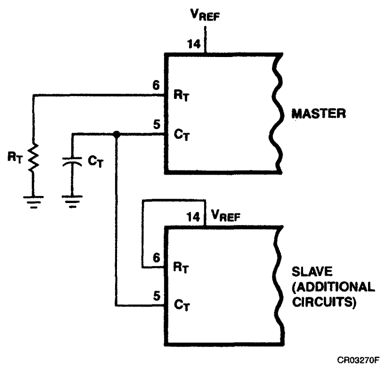
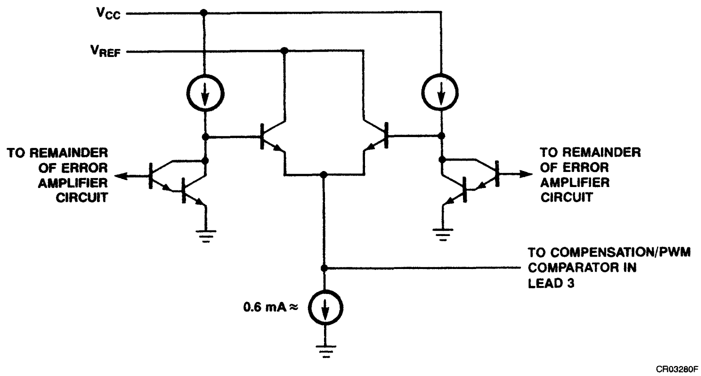
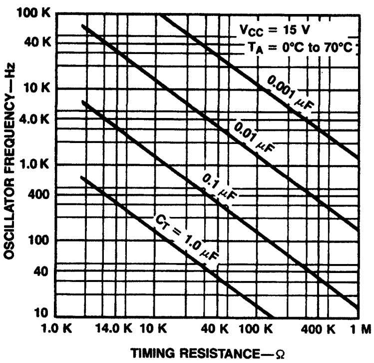


Figure 9 Error Amplifier and Current Limit Sense Amplifier Output Circuits



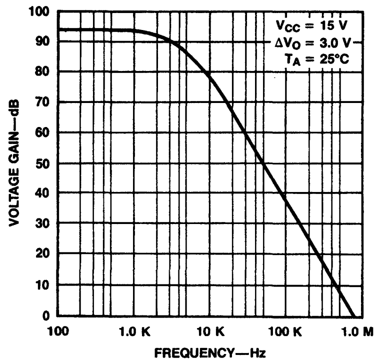
Typical Performance Curves

Figure 10 Oscillator Frequency vs Timing Resistance



PC08620F

Figure 11 Amplifier Voltage Gain vs Frequency



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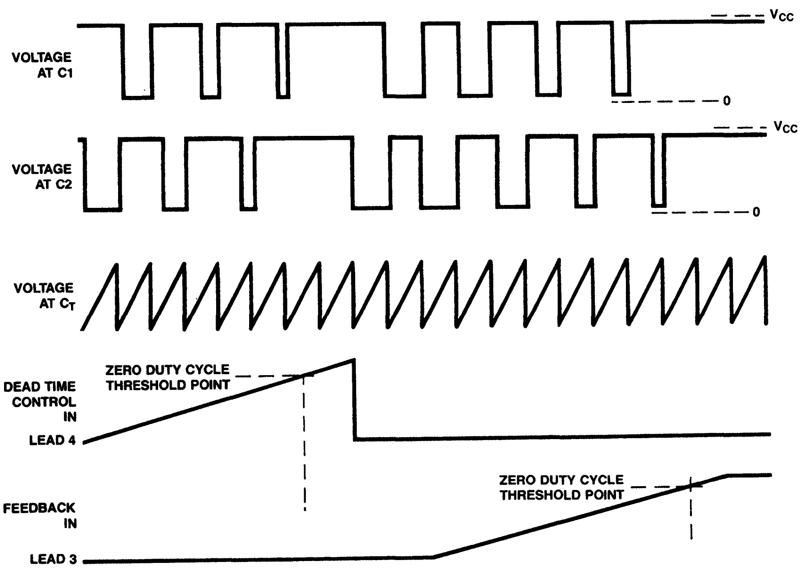
Voltage Waveforms



CR03220F

μA723
Precision Voltage Regulator

Description

The μA723 is a monolithic voltage regulator constructed using the Fairchild Planar Epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current-limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current-limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

- **Positive Or Negative Supply Operation**
- **Series, Shunt, Switching Or Floating Operation**
- **0.01% Line And Load Regulation**
- **Output Voltage Adjustable From 2 V To 37 V**
- **Output Current To 150 mA Without External Pass Transistor**

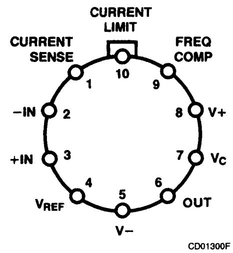
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP/Metal Can	−65°C to +175°C
Molded DIP/SO Package	−55°C to +150°C
Operating Temperature Range	
Extended (μA723M)	−55°C to +125°C
Commercial (μA723C)	0°C to +70°C
Lead Temperature	
Ceramic DIP/Metal Can (soldering, 60 s)	300°C
Molded DIP/SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
10L-Metal Can	1.07 W
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Pulse Voltage from V+ to V−, (50 ms) (μA723M)	50 V
Continuous Voltage from V+ to V−	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5.0 V
Voltage Between Non-Inverting Input and V−	8.0 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings supply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Connection Diagram
10-Lead Metal Package
(Top View)

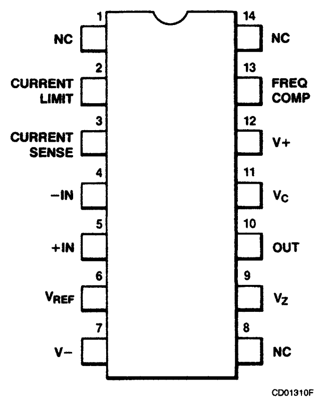


Lead 5 connected to case.

Order Information

Device Code	Package Code	Package Description
μA723HM	5X	Metal
μA723HC	5X	Metal

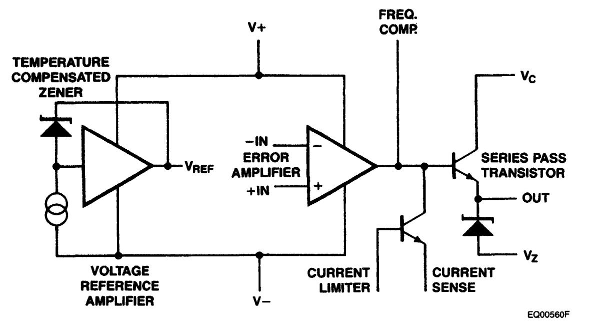
Connection Diagram
14-Lead DIP and SO-14 Package
(Top View)



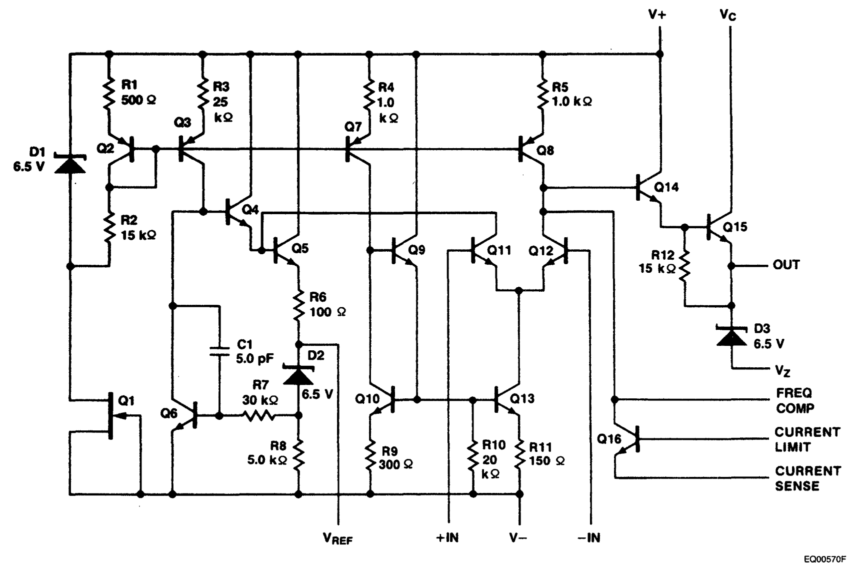
Order Information

Device Code	Package Code	Package Description
μA723DM	6A	Ceramic DIP
μA723DC	6A	Ceramic DIP
μA723PC	9A	Molded DIP
μA723SC	KD	Molded Surface Mount

Block Diagram



Equivalent Circuit



6

μA723M

Electrical Characteristics $T_A = 25°C$, $V_I = V+ = V_C = 12$ V, $V- = 0$, $V_O = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{REF} = 0$, unless otherwise specified.

Symbol	Characteristic[1]	Condition		Min	Typ	Max	Unit
$V_{R\ LINE}$	Line Regulation	$V_I = 12$ V to $V_I = 15$ V			0.01	0.1	$\%V_O$
		$V_I = 12$ V to $V_I = 40$ V			0.02	0.2	
		$-55°C \leqslant T_A \leqslant +125°C$, $V_I = 12$ V to $V_I = 15$ V				0.3	
$V_{R\ LOAD}$	Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA			0.03	0.15	$\%V_O$
		$-55°C \leqslant T_A \leqslant +125°C$, $I_L = 1$ mA to $I_L = 50$ mA				0.6	
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 50 Hz to 10 kHz			74		dB
		f = 50 Hz to 10 kHz, $C_{REF} = 0.5$ μF			86		
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$-55°C \leqslant T_A \leqslant +125°C$			0.002	0.015	%/°C
I_{OS}	Output Short Circuit Current	$R_{SC} = 10\ \Omega$, $V_O = 0$			65		mA
V_{REF}	Reference Voltage	$I_{REF} = 0.1$ mA		6.95	7.15	7.35	V
V_{REF}(Load)	Reference Voltage Change With Load	$I_{REF} = 0.1$ mA to 5 mA				20	mV
N_O	Noise	BW = 100 Hz to 10 kHz, $C_{REF} = 0$			20		μV_{rms}
		BW = 100 Hz to 10 kHz, $C_{REF} = 5.0$μF			2.0		
S	Long Term Stability	$T_J = T_{J\ Max}$	$T_A = 25°C$ For End Point Measurement		0.1		%/1000 hrs
I_{SCD}	Standby Current Drain	$I_L = 0$, $V_I = 30$ V			2.3	3.5	mA
V_{IR}	Input Voltage Range			9.5		40	V
V_{OR}	Output Voltage Range			2.0		37	V
$V_I - V_O$	Input/Output Voltage Differential			3.0		38	V

μA723C

Electrical Characteristics $T_A = 25°C$, $V_I = V+ = V_C = 12$ V, $V- = 0$, $V_O = 5$ V, $I_L = 1$ mA, $R_{SC} = 0$, C1 = 100 pF, $C_{REF} = 0$, unless otherwise specified.

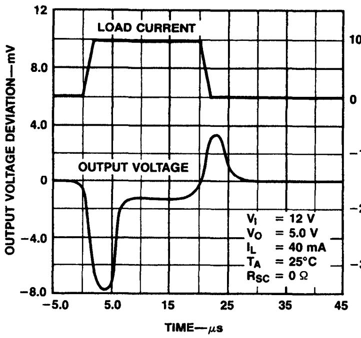
Symbol	Characteristic[1]	Condition		Min	Typ	Max	Unit
$V_{R\ LINE}$	Line Regulation	$V_I = 12$ V to $V_I = 15$ V			0.01	0.1	$\%V_O$
		$V_I = 12$ V to $V_I = 40$ V			0.1	0.5	
		$0°C \leqslant T_A \leqslant 70°C$, $V_I = 12$ V to $V_I = 15$ V				0.3	
$V_{R\ LOAD}$	Load Regulation	$I_L = 1.0$ mA to $I_L = 50$ mA			0.03	0.2	$\%V_O$
		$0°C \leqslant T_A \leqslant 70°C$, $I_L = 1.0$ mA to $I_L = 50$ mA				0.6	
$\Delta V_I / \Delta V_O$	Ripple Rejection	f = 50 Hz to 10 kHz			74		dB
		f = 50 Hz to 10 kHz, $C_{REF} = 5\ \mu F$			86		
$\Delta V_O / \Delta T$	Average Temperature Coefficient of Output Voltage	$0°C \leqslant T_A \leqslant 70°C$			0.003	0.015	%/°C
I_{OS}	Output Short Circuit Current	$R_{SC} = 10\ \Omega$, $V_O = 0$			65		mA
V_{REF}	Reference Voltage	$I_{REF} = 0.1$ mA		6.80	7.15	7.50	V
V_{REF}(Load)	Reference Voltage Change With Load	$I_{REF} = 0.1$ mA to 5 mA				20	mV
N_O	Noise	BW = 100 Hz to 10 kHz, $C_{REF} = 0$			20		μV_{rms}
		BW = 100 Hz to 10 kHz, $C_{REF} = 5\ \mu F$			2.0		
S	Long Term Stability	$T_J = T_{J\ Max}$	$T_A = 25°C$ For End Point Measurement		0.1		%/1000 hrs
I_{SCD}	Standby Current Drain	$I_L = 0$, $V_I = 30$ V			2.3	4.0	mA
V_{IR}	Input Voltage Range			9.5		40	V
V_{OR}	Output Voltage Range			2.0		37	V
$V_I - V_O$	Input/Output Voltage Differential			3.0		38	V

Note

1. Divider impedance as seen by error amplifier $\leqslant 10\ k\Omega$ connected as shown in *Figure 1*. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

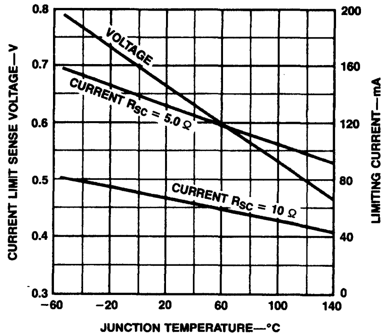
Typical Performance Curves for μA723 and μA723C

Load Transient Response



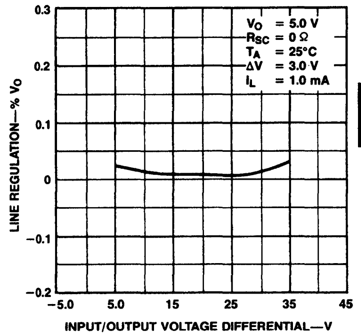
PC08460F

Current-Limiting Characteristics vs Junction Temperature



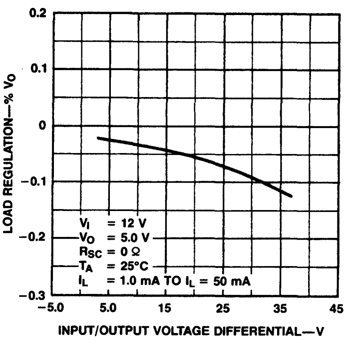
PC08450F

Line Regulation vs Input/Output Voltage Differential



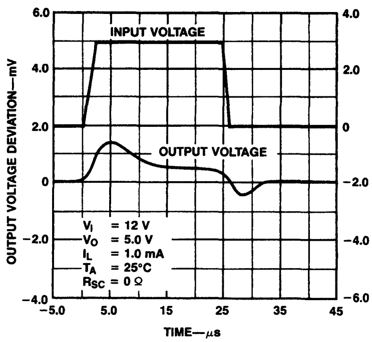
PC08440F

Load Regulation vs Input/Output Voltage Differential



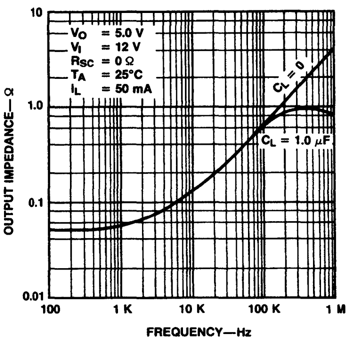
PC08470F

Line Transient Response



PC08480F

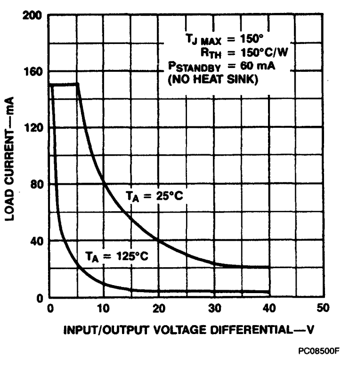
Output Impedance vs Frequency



PC08490F

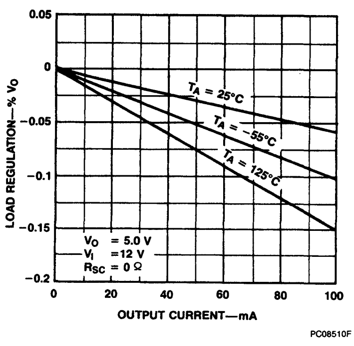
Typical Performance Curves for μA723

Maximum Load Current vs Input/Output Voltage Differential



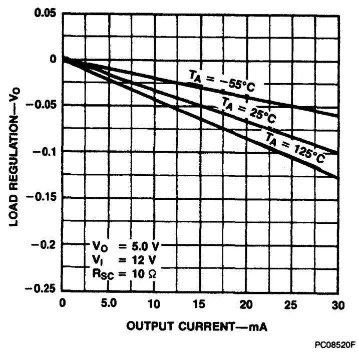
PC08500F

Load Regulation Characteristics Without Current-Limiting



PC08510F

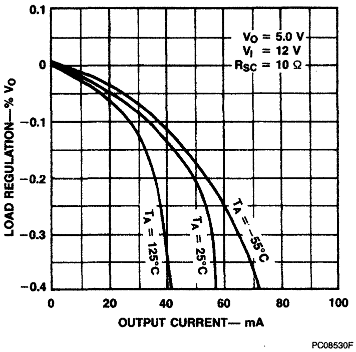
Load Regulation Characteristics With Current-Limiting



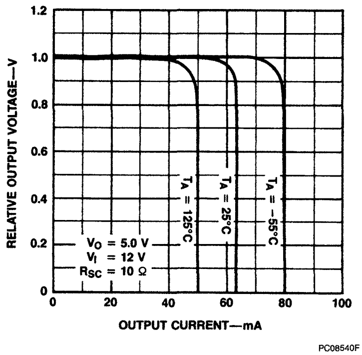
PC08520F

Typical Performance Curves for μA723

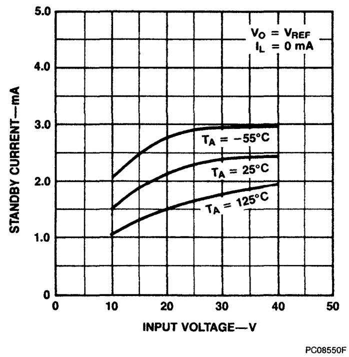
Load Regulation Characteristics With Current-Limiting



Current-Limiting Characteristics

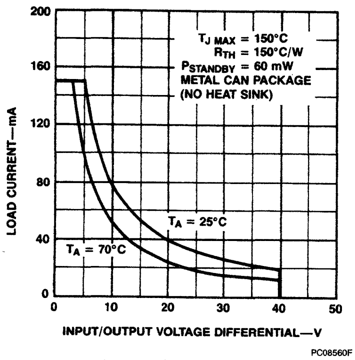


Standby Current Drain vs Input Voltage

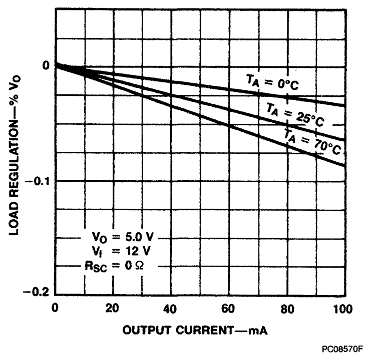


Typical Performance Curves for μA723C

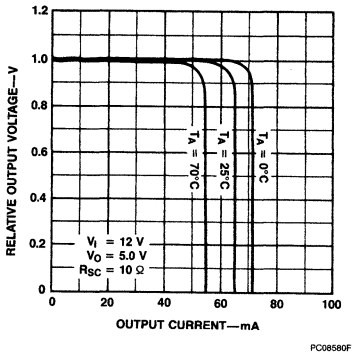
Maximum Load Current vs Input/Output Voltage Differential



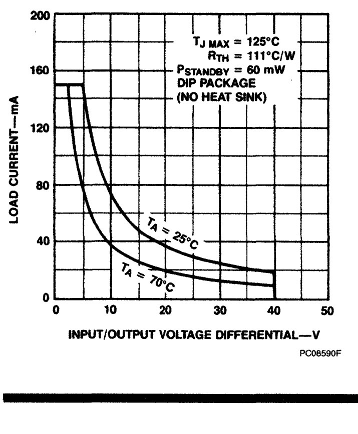
Load Regulation Characteristics Without Current-Limiting



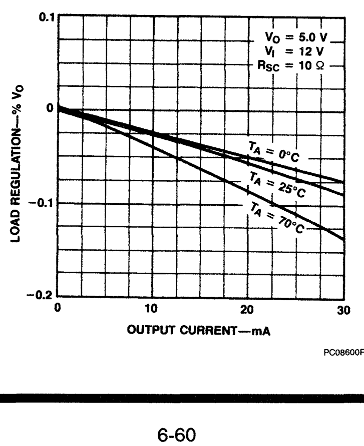
Current-Limiting Characteristics



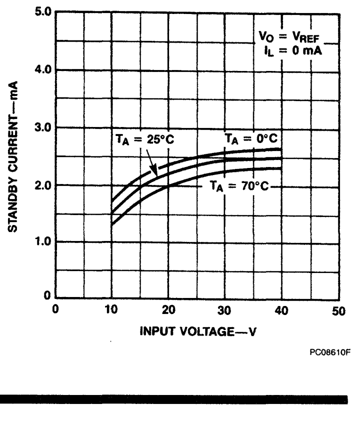
Maximum Load Current vs Input/Output Voltage Differential



Load Regulation Characteristics With Current-Limiting

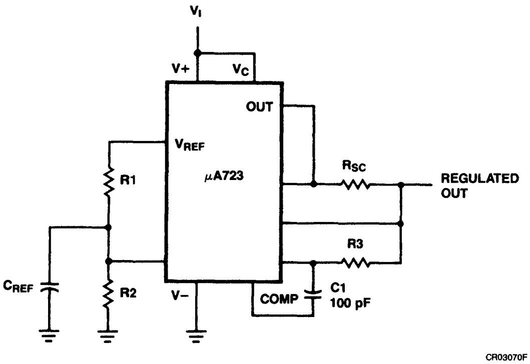


Standby Current Drain vs Input Voltage



Typical Applications

Figure 1 Basic Low Voltage Regulator
(V_O = 2.0 V to 7.0 V)

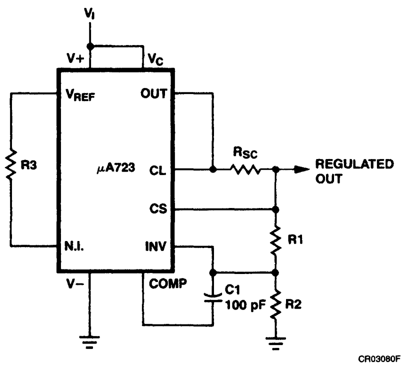


Typical Performance

Regulated Output Voltage	+ 5.0 V
Line Regulation (ΔV_I = 3.0 V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2 Basic High Voltage Regulator
(V_O = 7.0 V to 37 V)



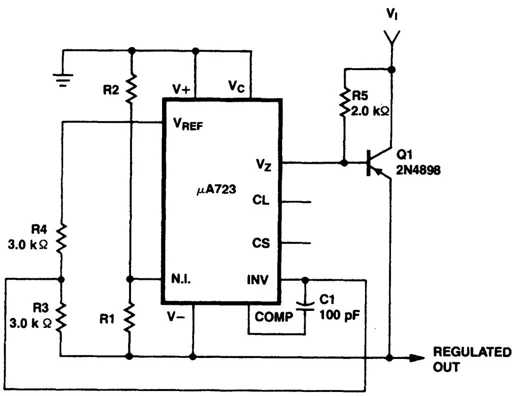
Typical Performance

Regulated Output Voltage	+15 V
Line Regulation (ΔV_I = 3.0 V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 3 Negative Voltage Regulator (Note 1)



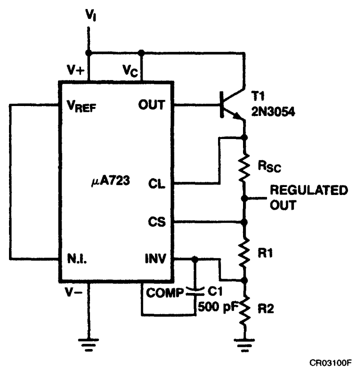
Typical Performance

Regulated Output Voltage	−15 V
Line Regulation (ΔV_I = 3.0 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Note

1. For metal can applications where V_Z is required, an external 6.2 V Zener diode should be connected in series with V_O.

Figure 4 Positive Voltage Regulator (External NPN Pass Transistor)



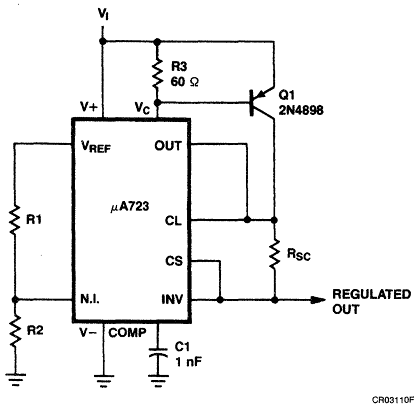
Typical Performance

Regulated Output voltage	+15 V
Line Regulation (ΔV_I = 3.0 V)	1.5 mV
Load Regulation (ΔI_L = 1.0 A)	15 mV

6

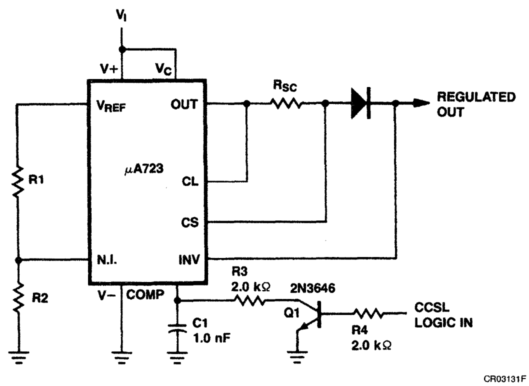
Typical Applications (Cont.)

Figure 5 Positive Voltage Regulator (External PNP Pass Transistor)



Typical Performance	
Regulated Output Voltage	+5.0 V
Line Regulation ($\Delta V_I = 3.0$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1.0$ A)	5.0 mV

Figure 7 Remote Shutdown Regulator with Current-Limiting (Note 1)

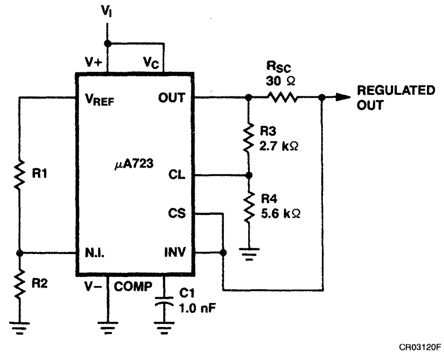


Typical Performance	
Regulated Output Voltage	+5.0 V
Line Regulation ($\Delta V_I = 3.0$ V)	0.5 mV
Load Regulation ($\Delta I_L = 50$ mA)	1.5 mV

Note

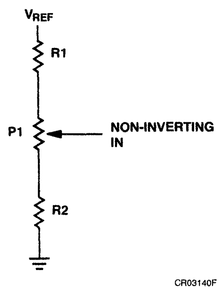
1. Current limit transistor may be used for shutdown if current limiting is not required. Add diode if $V_O > 10$ V.

Figure 6 Foldback Current-Limiting



Typical Performance	
Regulated Output Voltage	+5.0 V
Line Regulation ($\Delta V_I = 3.0$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1.0 mV
Short Circuit Current	20 mA

Figure 8 Output Voltage Adjust



FAIRCHILD

A Schlumberger Company

μA78G • μA79G 4-Terminal Adjustable Voltage Regulators

Linear Division Voltage Regulators

Description

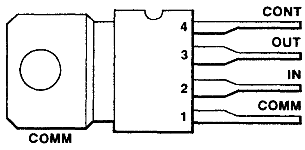
The μA78G and μA79G are 4-terminal adjustable voltage regulators. They are designed to deliver continuous load currents of up to 1.0 A with a maximum input voltage of +40 V for the positive regulator μA78G and -40 V for the negative regulator μA79G. Output current capability can be increased to greater than 1.0 A through use of one or more external transistors. The output voltage range of the μA78G positive voltage regulator is +5 V to +30 V and the output voltage range of the negative μA79G is -30 V to -2.2 V. For systems requiring both a positive and negative, the μA78G and μA79G are excellent for use as a dual tracking regulator with appropriate external circuitry. These 4-terminal voltage regulators are constructed using the Fairchild Planar process.

- **Output Current In Excess Of 1 A**
- **μA78G Positive Output +5 To +30 V**
- **μA79G Negative Output -30 To -2.2 V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Protection**
- **Output Transistor Safe-Area Protection**

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	0°C to 150°C
Lead Temperature (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
μA78G	+40 V
μA79G	-40 V
Control Lead Voltage	
μA78G	$0\ V \leq V+ \leq V_O$
μA79G	$V_O- \leq V- \leq 0\ V$

Connection Diagram 4-Lead TO-202 Package (Top View)

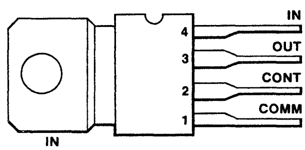


Heat sink tabs connected to common through device substrate.

Order Information

Device Code	Package Code	Package Description
μA78GU1C	8Z	Power Watt

Connection Diagram 4-Lead TO-202 Package (Top View)



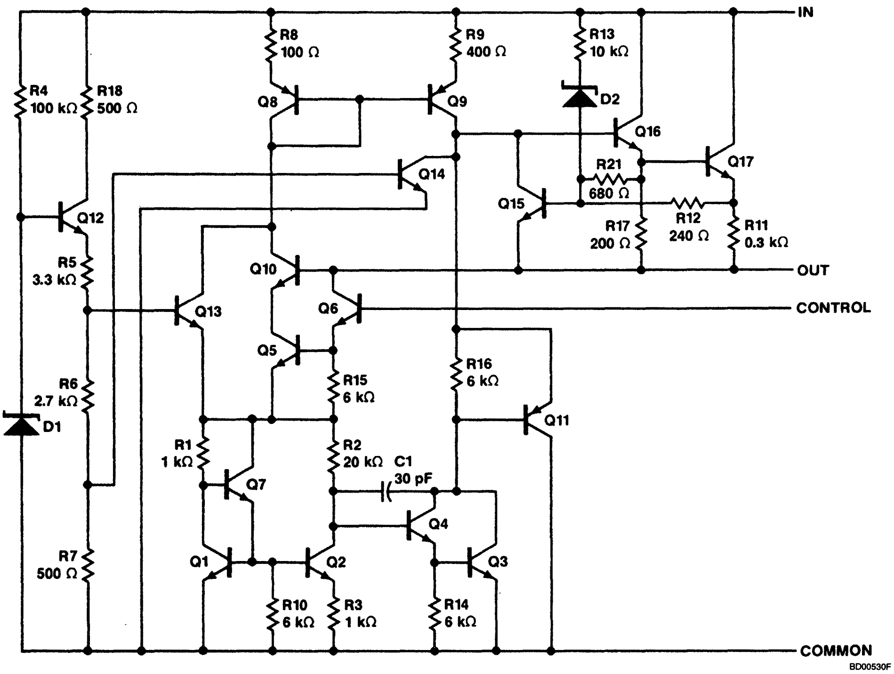
Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

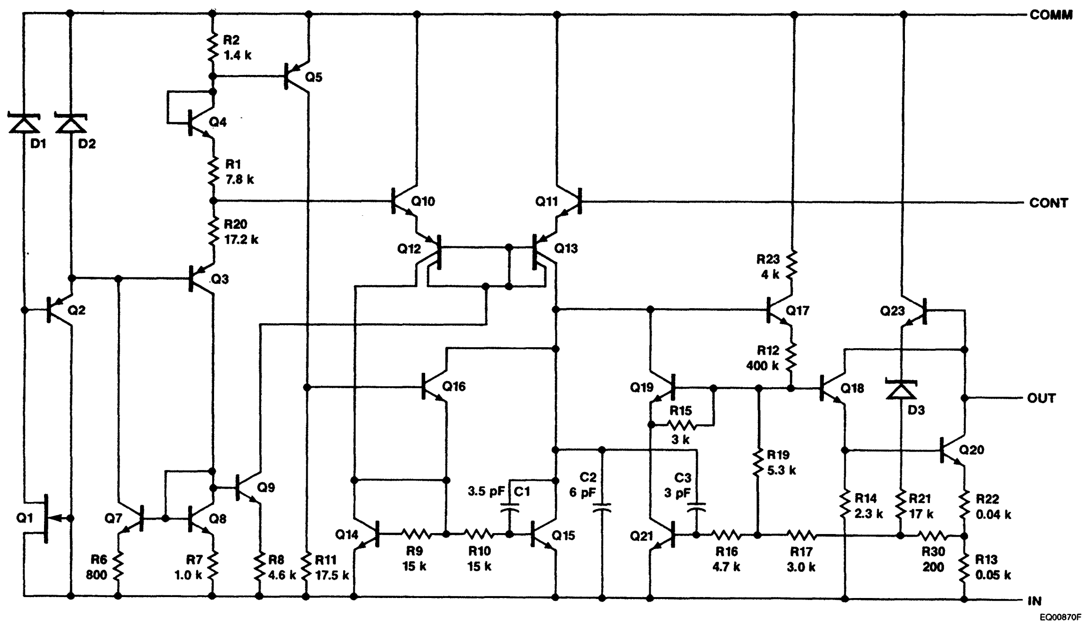
Device Code	Package Code	Package Description
μA79GU1C	8Z	Power Watt

6

μA78G Equivalent Circuit



μA79G Equivalent Circuit (Note 1)



Note

1. All Resistor values in ohms

μA78G

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $C_I = 0.33\ \mu F$, $C_O = 0.1\ \mu F$, $V_I = 10\ V$, $I_O = 500\ mA$, Test Circuit 1, unless otherwise specified.

Symbol	Characteristic	Condition[1,3]		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range	$T_J = 25°C$		7.5		40	V
V_{OR}	Output Voltage Range	$V_I = V_O + 5.0\ V$		5.0		30	V
V_O	Output Voltage Tolerance	$V_O + 3.0\ V \leq V_I \leq V_O + 15\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $P_D \leq 15\ W$, $V_{I\ max} = 38\ V$	$T_J = 25°C$			4.0	% V_O
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $V_O \leq 10\ V$ $(V_O + 2.5\ V) \leq V_I \leq (V_O + 20\ V)$				1.0	% V_O
$V_{O\ LOAD}$	Load Regulation	$T_J = 25°C$, $V_I = V_O + 5.0\ V$	$250\ mA \leq I_O \leq 750\ mA$			1.0	% V_O
			$5.0\ mA \leq I_O \leq 1.5\ A$			2.0	
I_C	Control Lead Current	$T_J = 25°C$			1.0	5.0	μA
						8.0	
I_Q	Quiescent Current	$T_J = 25°C$			3.2	6.0	mA
						7.0	
$\Delta V_I / \Delta V_O$	Ripple Rejection	$8.0\ V \leq V_I \leq 18\ V$, $f = 2400\ Hz$ $V_O = 5.0\ V$, $I_C = 350\ mA$		68	78		dB
N_O	Noise	$T_J = 25°C$, $10\ Hz < f < 100\ kHz$, $V_O = 5.0\ V$, $I_O = 5.0\ mA$			8.0	40	$\mu V/V_O$
V_{DO}	Dropout Voltage[2]				2.0	2.5	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 30\ V$			.750	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O / \Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = 5.0\ V$, $I_O = 5.0\ mA$	$T_A = -55°C$ to $+25°C$			0.4	mV/°C/ V_O
			$T_A = 25°C$ to $125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
				4.75		5.25	

Notes

1. V_O is defined for the μA78G as $V_O = \frac{R1 + R2}{R2}(5.0)$; the μA79G as $V_O = \frac{R1 + R2}{R2}(-2.23)$.
2. Dropout Voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_w \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA79G

Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$ for μA79G, $V_I = -10$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, Test Circuit 2 and Note 3, unless otherwise specified.

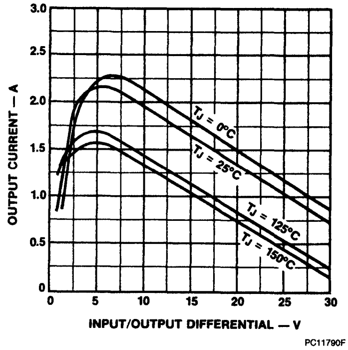
Symbol	Charateristic	Condition[1]		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range	$T_J = 25°C$		-40		-7.0	V
V_{OR}	Nominal Output Voltage Range	$V_I = V_O - 5.0$ V		-30		-2.23	V
V_O	Output Voltage Tolerance	$V_O - 15\text{ V} \leqslant V_I \leqslant V_O - 3.0$ V $5.0\text{ mA} \leqslant I_O \leqslant 1.0$ A $P_D \leqslant 15$ W, $V_{I\ Max} = -3.8$ V	$T_J = 25°C$			4.0	$\%V_O$
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $V_O \geqslant -10$ V $(V_O - 20\text{ V}) \leqslant V_I \leqslant (V_O - 2.5\text{ V})$				1.0	$\%V_O$
$V_{O\ LOAD}$	Load Regulation	$T_J = 25°C$, $V_I = V_O - 5.0$ V	$250\text{ mA} \leqslant I_O \leqslant 750$ mA			1.0	$\%V_O$
			$5.0\text{ mA} \leqslant I_O \leqslant 1.5$ A			2.0	
I_C	Control Lead Current	$T_J = 25°C$			0.4	2.0	μA
						3.0	
I_Q	Quiescent Current	$T_J = 25°C$			0.5	2.5	mA
						3.0	
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_O = -8.0$ V, $V_I = -13$ V, f = 2400 Hz, $I_C = 350$ mA		50	60		dB
N_O	Noise	$T_J = 25°C$, $10\text{ Hz} \leqslant f \leqslant 100$ kHz, $V_O = -8.0$ V, $I_O = 5.0$ mA			25	80	$\mu V/V_O$
V_{DO}	Dropout Voltage[2]				1.1	2.3	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = -30$ V			0.25	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = -5.0$ V, $I_O = 5.0$ mA	$T_A = -55°C$ to $+25°C$			0.3	$mV/°C/V_O$
			$T_A = 25°C$ to $125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		-2.32	-2.23	-2.14	V
				-2.35		-2.11	

Notes

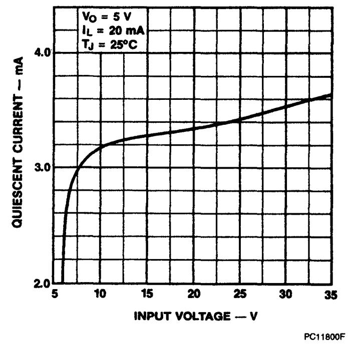
1. V_O is defined for the μA78G as $V_O = \frac{R1 + R2}{R2}(5.0)$; the μA79G as $V_O = \frac{R1 + R2}{R2}(-2.23)$.
2. Dropout voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. The convention for negative regulators is the algebraic value, thus −15 V is less than −10 V.
4. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves for μA78G

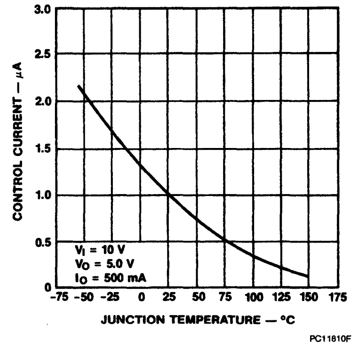
Peak Output Current vs Input/Output Differential Voltage



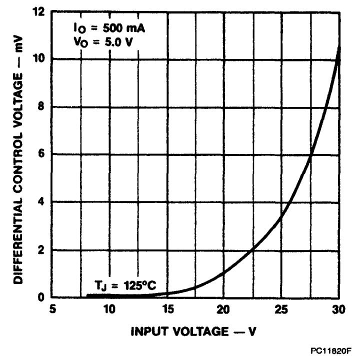
Quiescent Current vs Input Voltage



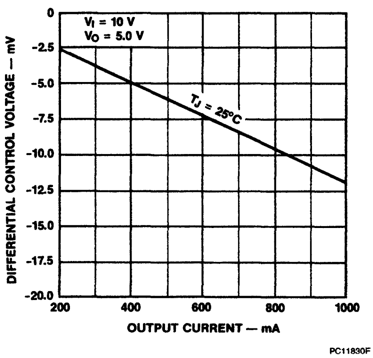
Control Current vs Junction Temperature



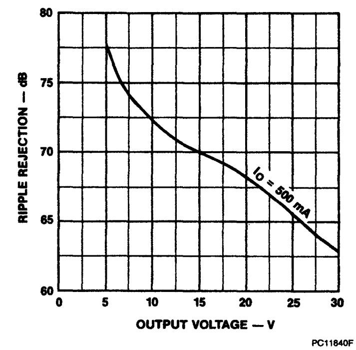
Differential Control Voltage vs Input Voltage



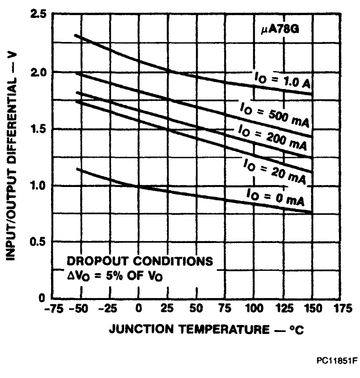
Differential Control Voltage vs Output Current



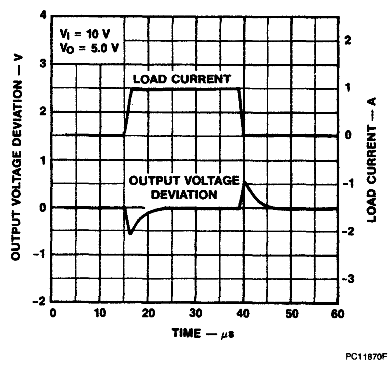
Ripple Rejection vs Output Voltage



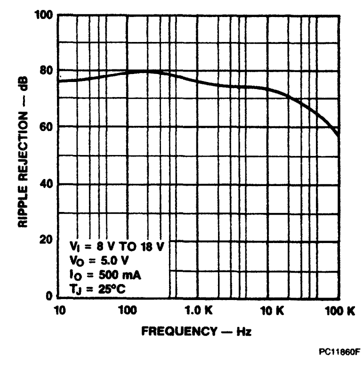
Dropout Voltage vs Junction Temperature vs Frequency



Load Transient Response

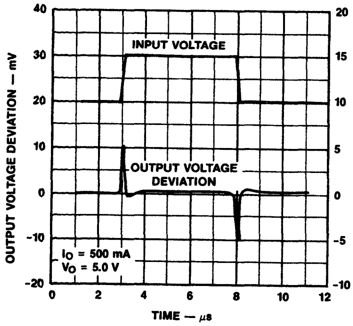


Ripple Rejection vs Frequency



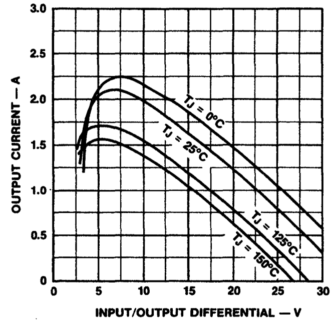
Typical Performance Curves for μA79G

Line Transient Response for μA78G



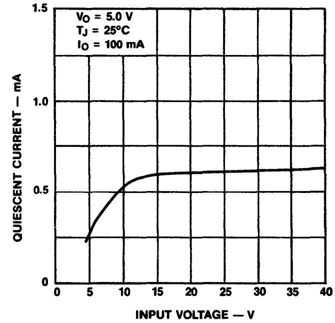
PC11680F

Peak Output Current vs Input/Output Differential Voltage



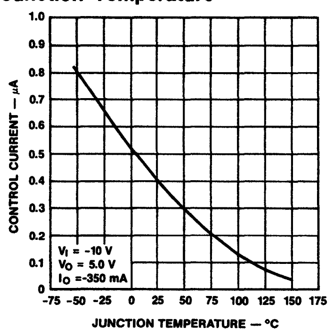
PC11690F

Quiescent Current vs Input Voltage



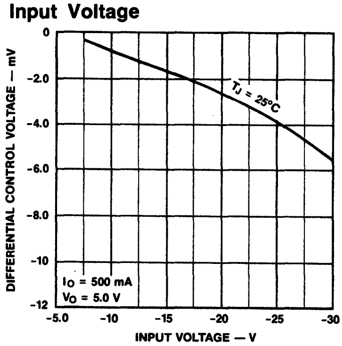
PC11700F

Control Current vs Junction Temperature



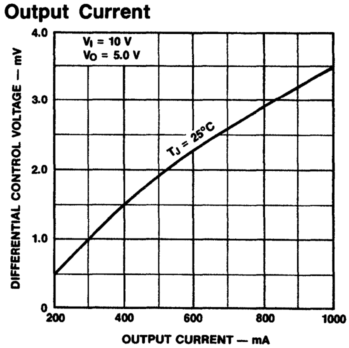
PC11710F

Differential Control Voltage vs Input Voltage



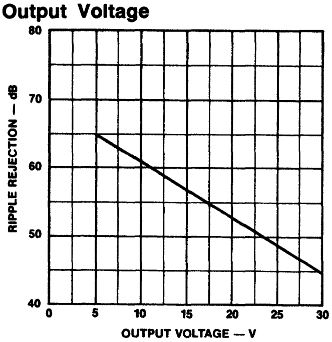
PC11720F

Differential Control Voltage vs Output Current



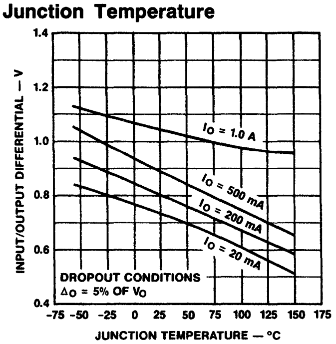
PC11730F

Ripple Rejection vs Output Voltage



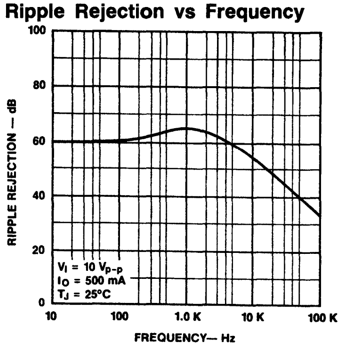
PC11740F

Dropout Voltage vs Junction Temperature



PC11750F

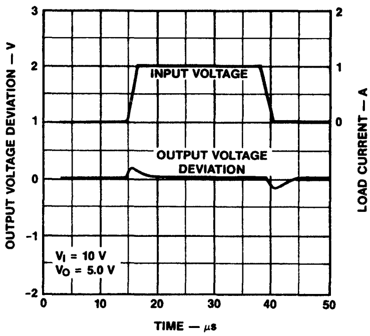
Ripple Rejection vs Frequency



PC11760F

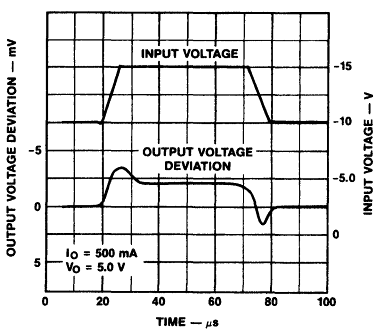
Typical Performance Curves for μA79G (Cont.)

Load Transient Response



PC11770F

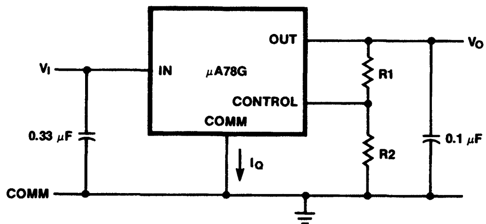
Line Transient Response



PC11780F

Test Circuits

μA78G Test Circuit 1

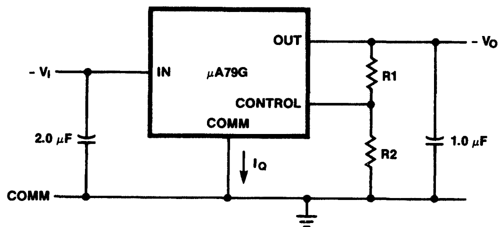


CR05650F

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{CONT}$$

V_{CONT} Nominal = 5.0 V

μA79G Test Circuit 2



CR05660F

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{CONT}$$

V_{CONT} Nominal = −2.23 V
Recommended R2 current ≈ 1.0 mA
∴ R2 = 5.0 kΩ (μA78G)
R2 = 2.2 kΩ (μA79G)

Design Considerations

The μA78G and μA79G Adjustable Voltage Regulators have an output voltage which varies from V_{CONT} to typically

$$V_I - 2.0 \text{ V by } V_O = V_{CONT} \frac{R1 + R2}{R2}$$

The nominal reference in the μA78G is 5.0 V and μA79G is −2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5.0 kΩ in the μA78G. Then, the output voltage is; V_O = (R1 + R2) V, where R1 and R2 are in kΩs.

Example: If R2 = 5.0 kΩ and R1 = 10 kΩ then
V_O = 15 V nominal, for the μA78G
R2 = 2.2 kΩ and R1 = 12.8 kΩ then
V_O = −15.2 nominal, for the μA79G

By proper wiring of the feedback resistors, load regulation of the device can be improved significantly.

Both μA78G and μA79G regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

6

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

	Typ °C/W	Max °C/W	Typ °C/W	Max °C/W
Package	θ_{JC}	θ_{JC}	θ_{JA}	θ_{JA}
Power Watt	7.5	11	75	80

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\ Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

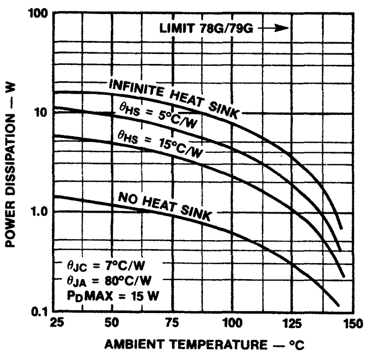
Solving for T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$
$$= T_A + P_D\theta_{JA} \text{ (without heat sink)}$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink resistance
θ_{SA} = Heat sink to ambient thermal resistance

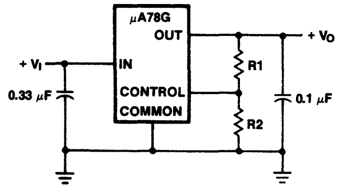
μA78G and μA79G
Power Tab (U1) Package
Worst Case Power Dissipation vs Ambient Temperature



Typical Applications For μA78G (Note 1)

Bypassing of the input and output (0.33 μF and 0.1 μF, respectively) is necessary.

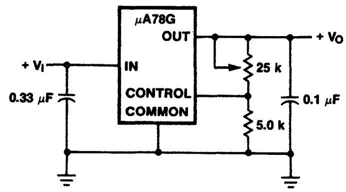
Basic Positive Regulator



$$V_O = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

CR05670F

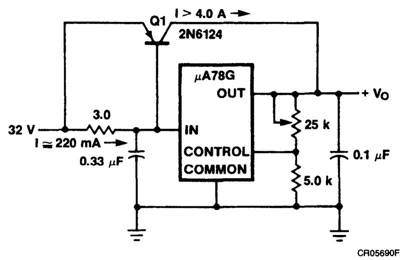
Positive 5.0 V to 30 V Adjustable Regulator



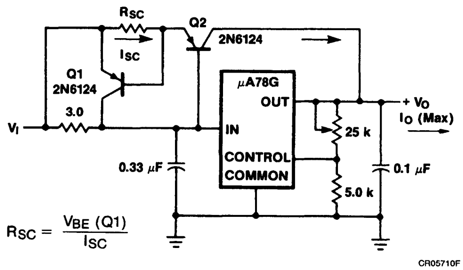
Note
1. All resistor values in ohms.

Typical Applications For μA78G (Note 1) (Cont.)

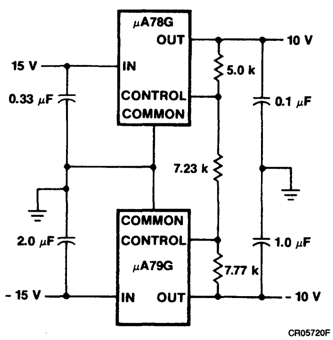
Positive 5.0 V to 30 V Adjustable Regulator
(I_O > 5.0 A) (Note 2)



Positive High Current Short Circuit, Protected Regulator

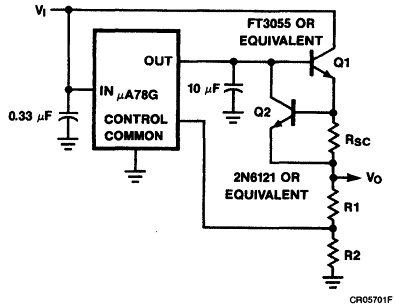


± 10 V, 1.0 A
Dual Tracking Regulator (Note 3)



Notes
1. All resistor values in ohms.
2. External series pass device is not short circuit protected.
3. If load is not ground referenced, connect reverse biased diodes from outputs to ground.

Positive High Current, Short Circuit Protected Regulator



FAIRCHILD

A Schlumberger Company

μA78L00 Series 3-terminal positive voltage regulators

Linear Division Voltage Regulators

Description

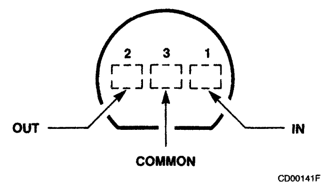
The μA78L00 series of 3-terminal positive voltage regulators is constructed using the Fairchild Planar Epitaxial process. These regulators employ internal current-limiting and thermal shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high current voltage regulators. The μA78L00 used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

- **Output Current Up To 100 mA**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Available In JEDEC TO-92**
- **Output Voltages Of 5.0 V, 6.2 V, 8.2 V, 9.0 V, 12 V, 15 V**
- **Output Voltage Tolerances Of ±5% Over The Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	
Industrial (μA78L00V)	-40°C to +125°C
Commercial (μA78L00C)	0°C to +125°C
Lead Temperature	
TO-92 Package/SO-8	
(soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0 V to 15 V	35 V

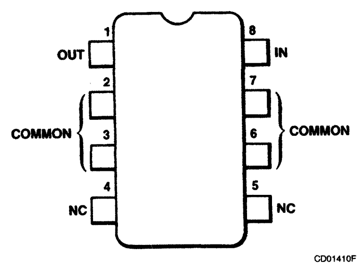
Connection Diagram TO-92 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA78L05AWV	EI	Molded
μA78L09AWV	EI	Molded
μA78L12AWV	EI	Molded
μA78L15AWV	EI	Molded
μA78L62AWV	EI	Molded
μA78L82AWV	EI	Molded
μA78L05AWC	EI	Molded
μA78L09AWC	EI	Molded
μA78L12AWC	EI	Molded
μA78L15AWC	EI	Molded
μA78L62AWC	EI	Molded
μA78L82AWC	EI	Molded

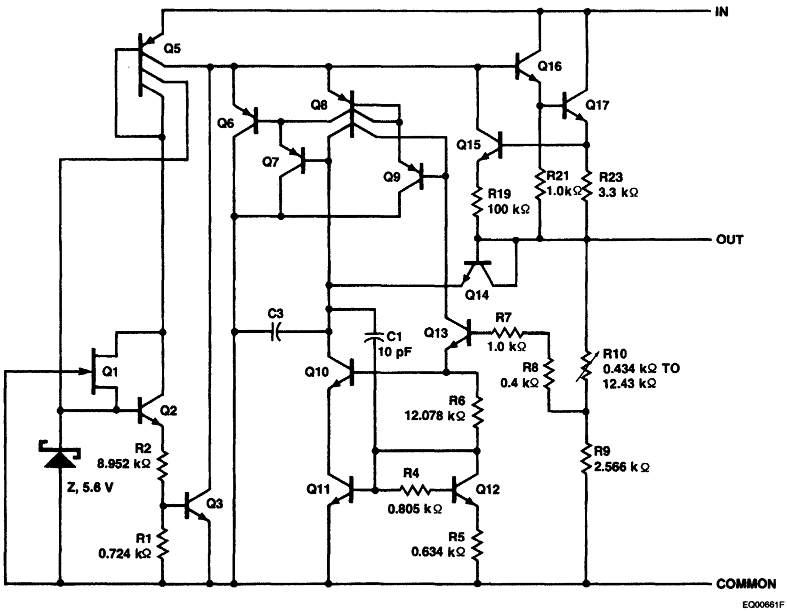
Connection Diagram SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA78L05ASC	KC	Molded Surface Mount

Equivalent Circuit



μA78L05AC[3]

Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_O	Output Voltage	T_J = 25°C		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation	T_J = 25°C	7.0 V ≤ V_I ≤ 20 V		55	150	mV
			8.0 V ≤ V_I ≤ 20 V		45	100	
$V_{R\ LOAD}$	Load Regulation	T_J = 25°C	1.0 mA ≤ I_O ≤ 100 V		11	60	mV
			1.0 mA ≤ I_O ≤ 40 mA		5.0	30	
V_O	Output Voltage[2]	7.0 V ≤ V_I ≤ 20 V	1.0 mA ≤ I_O ≤ 40 mA	4.75		5.25	V
		7.0 V ≤ V_I ≤ V_{Max}	1.0 mA ≤ I_O ≤ 70 mA	4.75		5.25	
I_Q	Quiescent Current				2.0	5.5	mA
ΔI_Q	Quiescent Current Change, with line	8.0 V ≤ V_I ≤ 20 V				1.5	mA
	Quiescent Current Change, with load	1.0 mA ≤ I_O ≤ 40 mA				0.1	
N_O	Noise	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 120 Hz, 8.0 V ≤ V_I ≤ 18 V, T_J = 25°C		41	49		dB
V_{DO}	Dropout Voltage	T_J = 25°C			1.7		V

μA78L05AC[3] (Cont.)
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 10$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[1]

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current	$T_J = 25°C$		140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA		−0.65		mV/°C

μA78L62AC[3]
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 12$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[1]

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		5.95	6.2	6.45	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.5\ V \leq V_I \leq 20$ V		65	175	mV
				$9.0\ V \leq V_I \leq 20$ V		55	125	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \leq I_O \leq 100$ mA		13	80	mV
				$1.0\ mA \leq I_O \leq 40$ mA		6.0	40	
V_O	Output Voltage[2]		$8.5\ V \leq V_I \leq 20$ V	$1.0\ mA \leq I_O \leq 40$ mA	5.90		6.5	V
			$8.5\ V \leq V_I \leq V_{Max}$	$1.0\ mA \leq I_O \leq 70$ mA	5.90		6.5	
I_Q	Quiescent Current					2.0	5.5	mA
ΔI_Q	Quiescent Current Change	with line	$8.0\ V \leq V_I \leq 20$ V				1.5	mA
		with load	$1.0\ mA \leq I_O \leq 40$ mA				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			50		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120$ Hz, $10\ V \leq V_I \leq 20$ V, $T_J = 25°C$		40	46		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−0.75		mV/°C

μA78L82AC[3]
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 14$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[1]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$		7.87	8.2	8.53	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	$11\ V \leq V_I \leq 23$ V		80	175	mV
			$12\ V \leq V_I \leq 23$ V		70	125	
$V_{R\ LOAD}$	Load Regulation	$T_J = 25°C$	$1.0\ mA \leq I_O \leq 100$ mA		15	80	mV
			$1.0\ mA \leq I_O \leq 40$ mA		8.0	40	

6

μA78L82AC[3] (Cont.)

Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.[1]

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
V_O	Output Voltage[2]		11 V ≤ V_I ≤ 23 V	1.0 mA ≤ I_O ≤ 40 mA	7.8		8.5	V
			11 V ≤ V_I ≤ V_{Max}	1.0 mA ≤ I_O ≤ 70 mA	7.8		8.6	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	with line	12 V ≤ V_I ≤ 23 V				1.5	mA
		with load	1.0 mA ≤ I_O ≤ 40 mA				0.1	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			60		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 120 Hz, 12 V ≤ V_I ≤ 22 V, T_J = 25°C		39	45		dB
V_{DO}	Dropout Voltage		T_J = 25°C			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		T_J = 25°C			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			−0.8		mV/°C

μA78L09AC[3]

Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 15 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.[1]

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
V_O	Output Voltage		T_J = 25°C		8.64	9.0	9.36	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	11.5 V ≤ V_I ≤ 24 V		90	200	mV
				13 V ≤ V_I ≤ 24 V		100	150	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	1.0 mA ≤ I_O ≤ 100 mA		20	90	mV
				1.0 mA ≤ I_O ≤ 40 mA		10	45	
V_O	Output Voltage[2]		11.5 V ≤ V_I ≤ 24 V	1.0 mA ≤ I_O ≤ 40 mA	8.55		9.45	V
			11.5 V ≤ V_I ≤ V_{Max}	1.0 mA ≤ I_O ≤ 70 mA	8.55		9.45	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	with line	11.5 V ≤ V_I ≤ 24 V				1.5	mA
		with load	1.0 mA ≤ I_O ≤ 40 mA				0.1	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			70		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = 25°C		38	44		dB
V_{DO}	Dropout Voltage		T_J = 25°C			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		T_J = 25°C			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			−0.9		mV/°C

μA78L12AC[3]

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[1]

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		11.5	12	12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$14.5\ V \leq V_I \leq 27\ V$		120	250	mV
				$16\ V \leq V_I \leq 27\ V$		100	200	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \leq I_O \leq 100\ mA$		20	100	mV
				$1.0\ mA \leq I_O \leq 40\ mA$		10	50	
V_O	Output Voltage[2]		$14.5\ V \leq V_I \leq 27\ V$	$1.0\ mA \leq I_O \leq 40\ mA$	11.4		12.6	V
			$14.5\ V \leq V_I \leq V_{Max}$	$1.0\ mA \leq I_O \leq 70\ mA$	11.4		12.6	
I_Q	Quiescent Current					2.1	5.5	mA
ΔI_Q	Quiescent Current Change	with line	$16\ V \leq V_I \leq 27\ V$				1.5	mA
		with load	$1.0\ mA \leq I_O \leq 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			80		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 120$ Hz, $15\ V \leq V_I \leq 25\ V$, $T_J = 25°C$		37	42		dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current		$T_J = 25°C$			140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			−1.0		mV/°C

μA78L15AC[3]

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 40$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[1]

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		14.4	15	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$17.5\ V \leq V_I \leq 30\ V$		130	300	mV
				$20\ V \leq V_I \leq 30\ V$		110	250	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$1.0\ mA \leq I_O \leq 100\ mA$		25	150	mV
				$1.0\ mA \leq I_O \leq 40\ mA$		12	75	
V_O	Output Voltage[2]		$17.5\ V \leq V_I \leq 30\ V$	$1.0\ mA \leq I_O \leq 40\ mA$	14.25		15.75	V
			$17.5\ V \leq V_I \leq V_{Max}$	$1.0\ mA \leq I_O \leq 70\ mA$	14.25		15.75	
I_Q	Quiescent Current					2.2	5.5	mA
ΔI_Q	Quiescent Current Change	with line	$20\ V \leq V_I \leq 30\ V$				1.5	mA
		with load	$1.0\ mA \leq I_O \leq 40\ mA$				0.1	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			90		μV

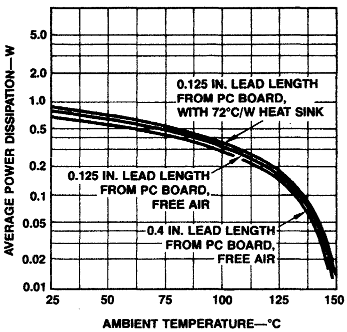
µA78L15AC[3] (Cont.)
Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, unless otherwise specified.[1]

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C	34	39		dB
V_{DO}	Dropout Voltage	T_J = 25°C		1.7		V
I_{pk}/I_{OS}	Peak Output/Output Short Circuit Current	T_J = 25°C		140		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	I_O = 5.0 mA		−1.3		mV/°C

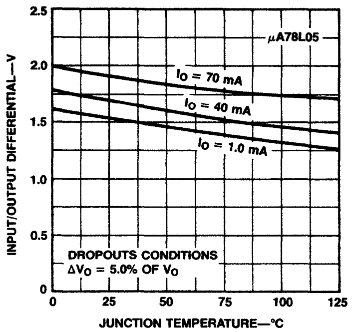
Notes
1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
2. Power Dissipation ≤ .75 W.
3. Industrial Grade product is guaranteed to have output voltage tolerances less than ±8% at −40°C.

Typical Performance Curves

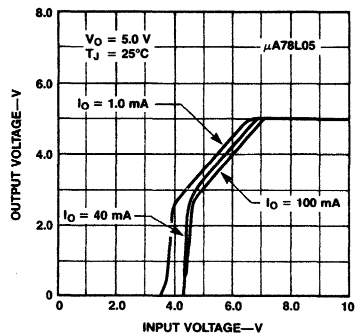
Worst Case Power Dissipation vs Ambient Temperature (TO-92)



Dropout Voltage vs Junction Temperature



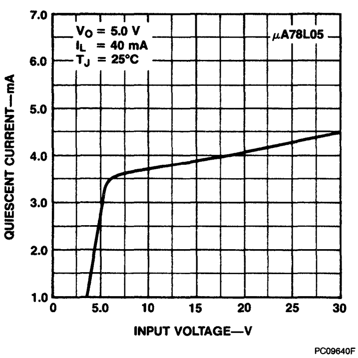
Dropout Characteristics



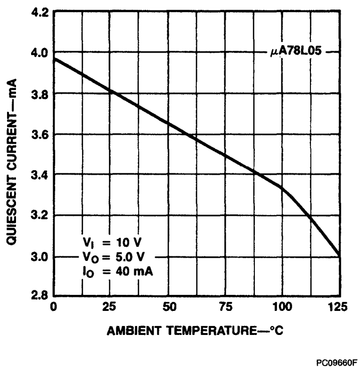
Note
Other µA78L00 Series devices have similar curves.

Typical Performance Curves (Cont.)

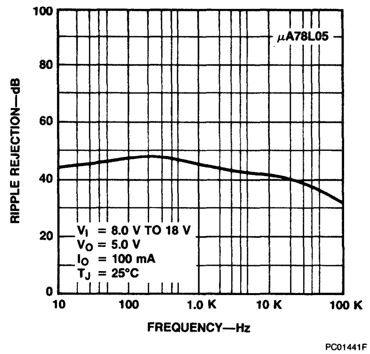
Quiescent Current vs Input Voltage



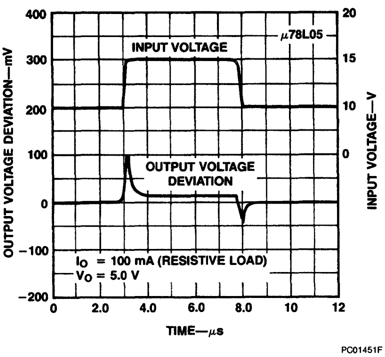
Quiescent Current vs Temperature



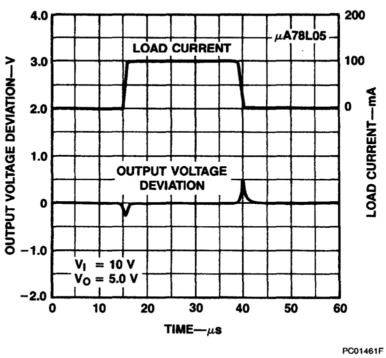
Ripple Rejection vs Frequency



Line Transient Response



Load Transient Response



Design Considerations

The μA78L series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-92			160	160

Thermal Considerations

The TO-92 molded package manufactured by Fairchild is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1 cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the leads, in parallel with the case path, to ambient temperature, as shown in *Figure 1.*

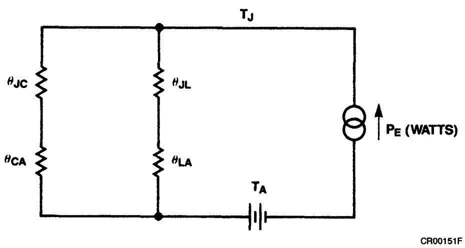
The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})\ (\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}} \quad (1)$$

Where:

- θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.
- θ_{CA} = thermal resistance between the case and air at ambient temperature.
- θ_{JL} = thermal resistance from regulator die through the input lead to a point 1/16 inch below the regulator case.
- θ_{LA} = total thermal resistance of the input/output ground leads to ambient temperature.
- θ_{JA} = junction to ambient thermal resistance.

Figure 1 TO-92 Thermal Equivalent Circuit



Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the μA78LXX molded case. The heat sink effectively replaces the θ_{CA} (*Figure 2*) and the new thermal resistance, θ'_{JA}, equals 145°C/W (assuming 0.125 inch lead length).

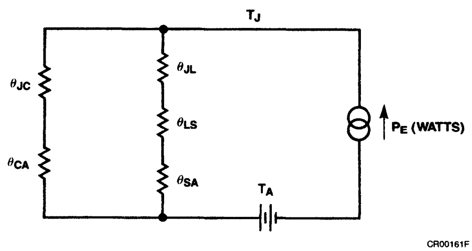
The net change of 15°C/W increases the allowable power dissipation to 0.86 W with a minimal inserted cost. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the leads at the mounting point to ambient, that is, the mounting medium. θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in *Figure 2.*

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but lead sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the leads. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

Figure 2 TO-92 Thermal Equivalent Circuit
(Lead at Other Than Ambient Temperature)



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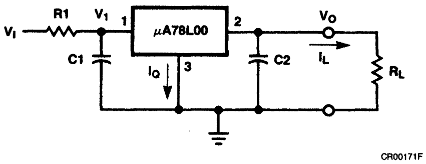
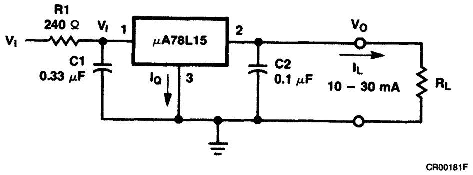
High Dissipation Applications





When it is necessary to operate a μA78L00 regulator with a large input/output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 = \frac{V_{I\ Min} - V_O - 2.0\ V}{I_{L\ Max} + I_Q} \qquad (3)$$

where:

I_Q is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D\ Max} = (V_1 - V_O)\ I_{L\ Max} + V_1\ I_Q \qquad (4)$$

where:

$$V_1 = V_{I\ Max} - (I_{L\ Max} + I_Q)\ R1$$

The presence of R1 will affect load regulation according to the equation:

Load regulation (at constant V_I) (5)
= load regulation (at constant V_1)
+ line regulation (mV per V)
x (RI) x (ΔI_L).

As an example, consider a 15 V regulator with a supply voltage of 30 ±5.0 V, required to supply a maximum load current of 30 mA. I_Q is 4.3 mA, and minimum load current is to be 10 mA.

$$R1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{8}{34.3} \cong 240\ \Omega \qquad (6)$$

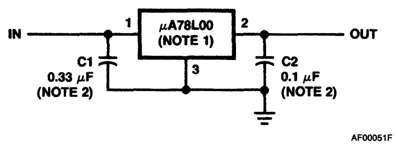
$$V_1 = 35 - (30 + 4.3)\ 0.24 = 35 - 8.2 = 26.8\ V$$

$P_{D\ Max} = (26.8 - 15)\ 30 + 26.8\ (4.3)$
$= 354 + 115$
$= 470$ mW, which permit operation up to 70°C in most applications.

Line regulation of this circuit is typically 110 mV for an input range of 25 – 35 V at a constant load current; i.e. 11 mV/V.

Load regulation = constant V_1 load regulation (7)
(typically 10 mV, 10 – 30 mA I_L)
+ (11 mV/V) x 0.24 x 20 mA
(typically 53 mV)
= 63 mV for a load current change of 20 mA at a constant V_I of 30 V.

Typical Applications



Notes

1. To specify an output voltage, substitute voltage value for "00".
2. Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

FAIRCHILD

A Schlumberger Company

μA78MG • μA79MG 4-Terminal Adjustable Voltage Regulators

Linear Division Voltage Regulators

Description

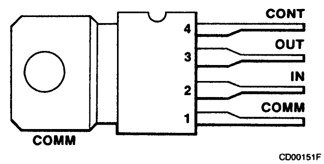
The μA78MG and μA79MG are 4-terminal adjustable voltage regulators. They are designed to deliver continuous load currents of up to 500 mA with a maximum input voltage of +40 V for the positive regulator μA78MG and -40 V for the negative regulator μA79MG. Output current capability can be increased to greater than 10 A through use of one or more external transistors. The output voltage range of the μA78MG positive voltage regulator is 5.0 V to 30 V and the output voltage range of the negative μA79MG is -30 to -2.2 V. For systems requiring both a positive and negative, the μA78MG and μA79MG are excellent for use as a dual tracking regulator. These 4-terminal voltage regulators are constructed using the Fairchild Planar process.

- **Output Current In Excess Of 0.5 A**
- **μA78MG Positive Output Voltage +5.0 To +30 V**
- **μA79MG Negative Output Voltage -30 V To -2.2 V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current Protection**
- **Output Transistor Safe-Area Protection**

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	0°C to 150°C
Lead Temperature (soldering, 10 s)	265°C
Internal Power Dissipation	Internally Limited
Input Voltage	
μA78MGC	+40 V
μA79MGC	-40 V
Control Lead Voltage	
μA78MGC	$0\ V \leqslant V+ \leqslant V_O$
μA79MGC	$V_O- \leqslant -V \leqslant 0\ V$

Connection Diagram μA78MG Power Watt (Top View)

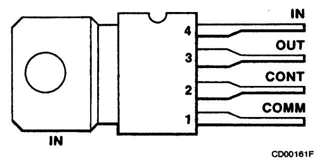


Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

Device Code	Package Code	Package Description
μA78MGU1C	8Z	Molded Power Pack

Connection Diagram μA79MG Power Watt (Top View)



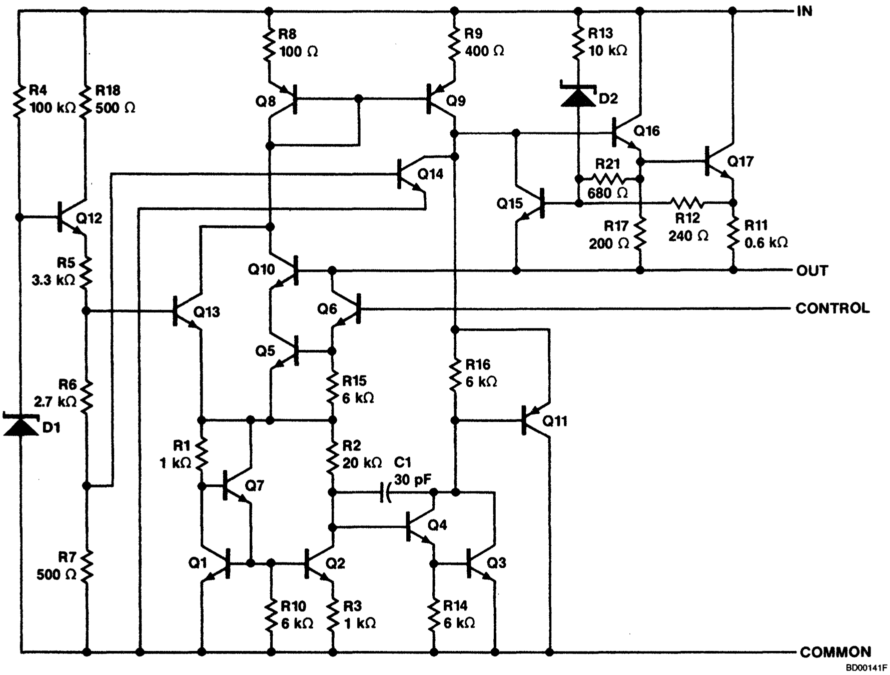
Heat sink tabs connected to input through device substrate. Not recommended for direct electrical connection.

Order Information

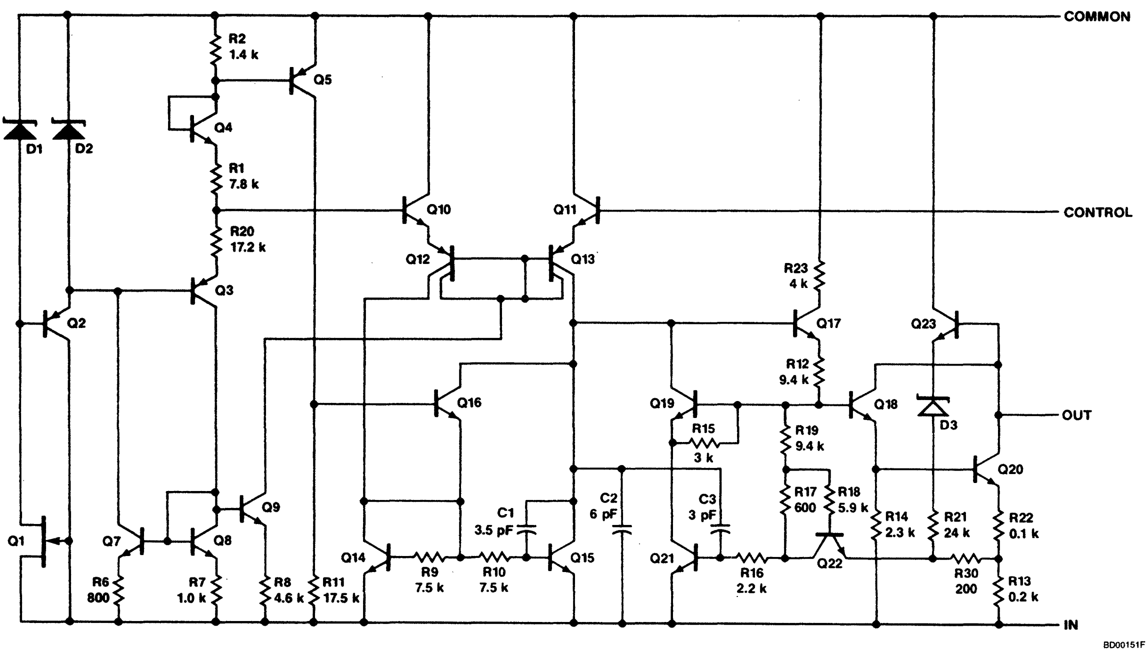
Device Code	Package Code	Package Description
μA79MGU1C	8Z	Molded Power Pack

6

μA78MG Equivalent Circuit



μA79MG Equivalent Circuit (Note 1)



Note

1. Resistor values in Ω unless otherwise noted.

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μA78MGC

Electrical Characteristics $0°C \leq T_A \leq 125°C$ for μA78MGC, $V_I = 10$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, Test Circuit 1, unless otherwise specified.

Symbol	Characteristic	Condition[1,3]		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range	$T_J = 25°C$		7.5		40	V
V_{OR}	Output Voltage Range	$V_I = V_O + 5.0$ V		5.0		30	V
V_O	Output Voltage Tolerance	$V_O + 3.0 \text{ V} \leq V_I \leq V_O + 15$ V, 5.0 mA $\leq I_O \leq$ 350 mA, $P_D \leq 5.0$ W, $V_{I\,Max} = 38$ V	$T_J = 25°C$			4.0	%(V_O)
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $I_O = 200$ mA, $V_O \leq 10$ V, $(V_O + 2.5 \text{ V}) \leq V_I \leq (V_O + 20 \text{ V})$, $T_J = 25°C$, $I_O = 200$ mA, $V_O \geq 10$ V				1.0	%(V_O)
$V_{O\ LOAD}$	Load Regulation	$T_J = 25°C$, 5.0 mA $\leq I_O \leq$ 500 mA, $V_I = V_O + 7.0$ V				1.0	%(V_O)
I_C	Control Lead Current	$T_J = 25°C$			1.0	6.0	μA
						7.0	
I_Q	Quiescent Current	$T_J = 25°C$			2.8	5.0	mA
						6.0	
RR	Ripple Rejection	$I_O = 125$ mA, 8.0 V $\leq V_I \leq$ 18 V, $V_O = 5.0$ V, f = 2400 Hz		62	80		dB
N_O	Output Noise Voltage	10 Hz $\leq$ f $\leq$ 100 kHz, $V_O = 5.0$ V			8	40	μV/V_O
V_{DO}	Dropout Voltage[2]				2	2.5	V
I_{OS}	Short Circuit Current	$V_I = 35$ V, $T_J = 25°C$				600	mA
I_{pk}	Peak Output Current	$T_J = 25°C$		0.4	0.8	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = 5.0$ V, $I_O = 5.0$ mA	$T_A = -55°C$ to $+25°C$			0.4	mV/°C/V_O
			$T_A = 25°C$ to 125°C			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		4.8	5.0	5.2	V
				4.75		5.25	

μA79MGC

Electrical Characteristics $0°C \leq T_J \leq 125°C$ for μA79MGC, $V_I = -14$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, Test Circuit 2, unless otherwise specified.

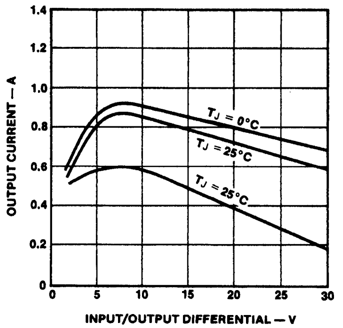
Symbol	Characteristic	Condition[1,4,5]		Min	Typ	Max	Unit
V_{IR}	Input Voltage Range	$T_J = 25°C$		-40		-7.0	V
V_{OR}	Output Voltage Range	$V_I = V_O - 5.0$ V		-30		-2.23	V
V_O	Output Voltage Tolerance	$V_O - 15\text{ V} \leq V_I \leq V_O - 3.0$ V, 5.0 mA $\leq I_O \leq$ 350 mA, $P_D \leq 5.0$ W, $V_{I\ Max} = -38$ V	$T_J = 25°C$			4.0	%(V_O)
						5.0	
$V_{O\ LINE}$	Line Regulation	$T_J = 25°C$, $I_O = 200$ mA, $V_O \leq -10$ V, $(V_O - 20\text{ V}) \leq V_I \leq (V_O - 2.5\text{ V})$, $T_J = 25°C$, $I_O = 200$ mA, $V_O \leq -10$ V				1.0	%(V_O)
$V_{O\ LOAD}$	Load Regulation	$V_I = V_O - 7.0$ V, 5.0 mA $\leq I_O \leq$ 500 mA, $T_J = 25°C$				1.0	%(V_O)
I_C	Control Lead Current	$T_J = 25°C$				2.0	μA
						3.0	
I_Q	Quiescent Current	$T_J = 25°C$			0.5	2.5	mA
						3.5	
RR	Ripple Rejection	$T_J = 25°C$, $I_O = 125$ mA, $V_I = -13$ V $V_O = -5.0$ V, f = 2400 Hz		50			dB
N_O	Noise	10 Hz $\leq f \leq$ 100 kHz, $V_O = -8.0$ V, $I_L = 50$ mA			25	80	μV/ V_O
V_{DO}	Dropout Voltage				1.1	2.3	V
I_{OS}	Short Circuit Current	$V_I = 35$ V, $T_J = 25°C$				600	mA
I_{pk}	Peak Output Current			0.4	0.65	1.4	mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_O = -5.0$ V, $I_O = -5.0$ mA	$T_A = -55°C$ to $+25°C$			0.3	mV/ °C/ V_O
			$T_A = 25°C$ to $125°C$			0.3	
V_C	Control Lead Voltage (Reference)	$T_J = 25°C$		-2.32	-2.23	-2.14	V
				-2.35		-2.11	

Notes

1. V_O is defined for the μA78MGC as $V_O = \frac{R1 + R2}{R2}(5.0)$. The μA79MGC as $V_O = \frac{R1 + R2}{R2}(-2.23)$.
2. Dropout voltage is defined as that input/output voltage differential which causes the output voltage to decrease by 5% of its initial value.
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.
4. The convention for negative regulators is the Algebraic value, thus −15 V is less than −10 V.
5. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

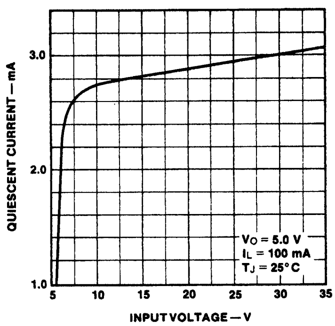
Typical Performance Curves For μA78MG

Peak Output Current vs Input/Output Differential Voltage



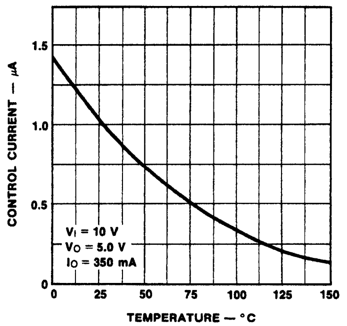
PC01481F

Quiescent Current vs Input Voltage



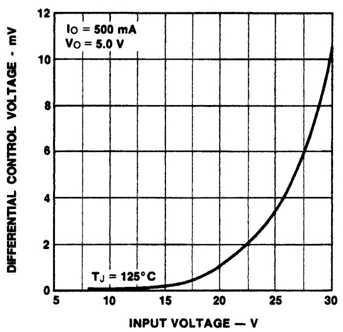
PC01491F

Control Current vs Temperature



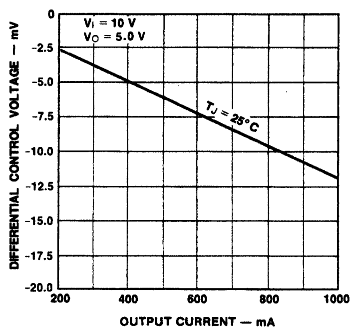
PC01501F

Differential Control Voltage vs Input Voltage



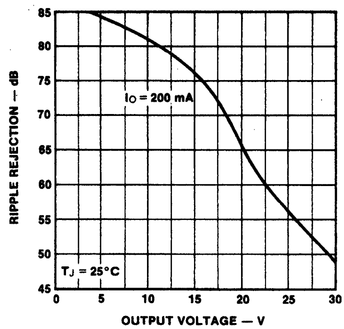
PC01511F

Differential Control Voltage vs Output Current



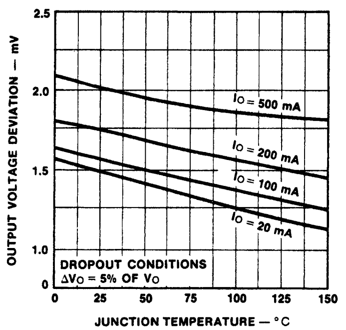
PC01521F

Ripple Rejection vs Output Voltage



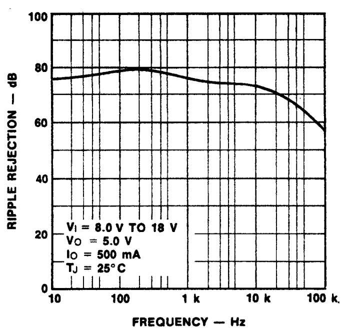
PC01531F

Dropout Voltage vs Junction Temperature



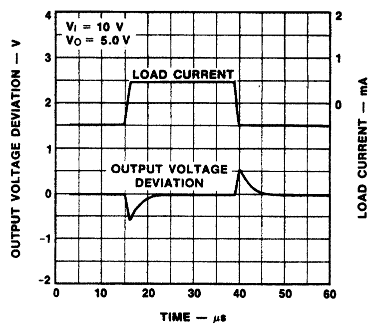
PC01541F

Ripple Rejection vs Frequency



PC01551F

Load Transient Response

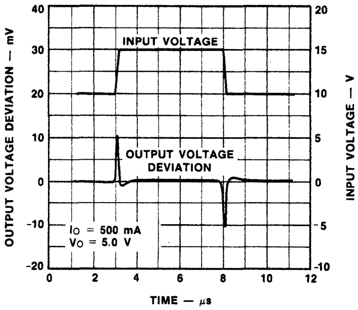


PC01561F

6

Typical Performance Curves For μA78MG (Cont.)

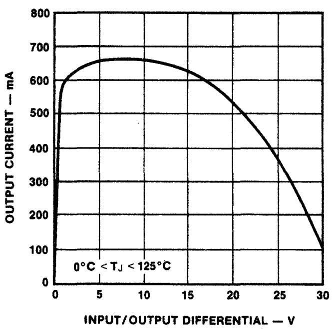
Line Transient Response



PC01571F

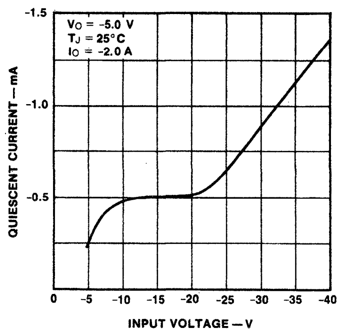
Typical Performance Curves For μA79MG

Peak Output Current vs Input/Output Differential Voltage



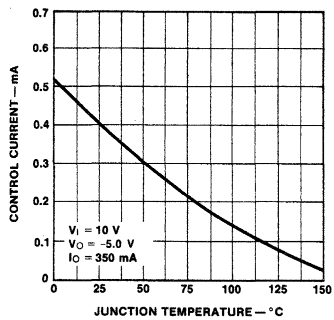
PC01581F

Quiescent Current vs Input Voltage



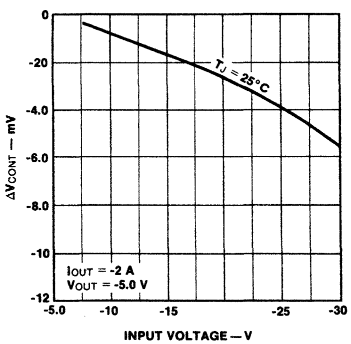
PC01591F

Control Current vs Temperature



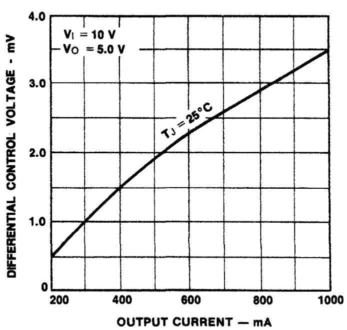
PC01601F

Differential Control Voltage vs Input Voltage



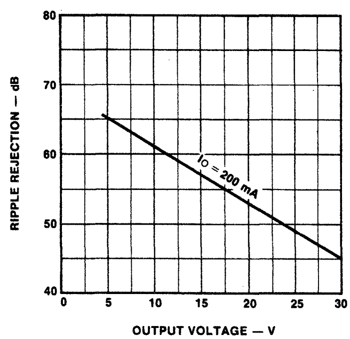
PC11670F

Differential Control Voltage vs Output Current



PC01621F

Ripple Rejection vs Output Voltage



PC01631F

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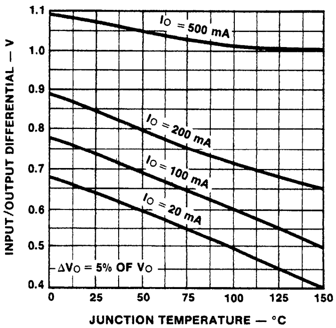
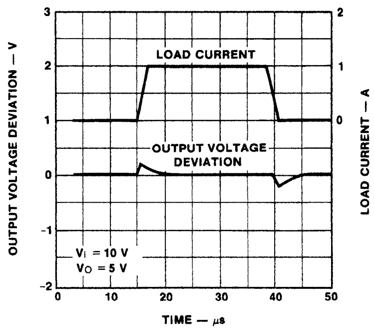
Typical Performance Curves For μA79MG (Cont.)

Dropout Voltage vs Junction Temperature



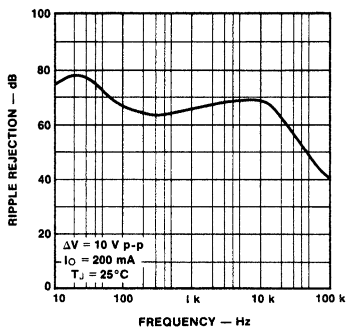
PC01641F

Load Transient Response



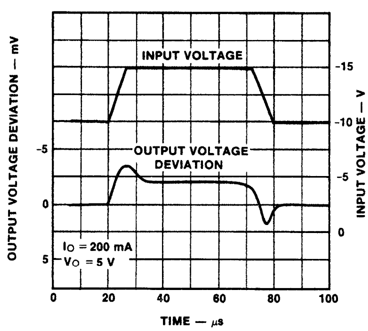
PC01661F

Ripple Rejection vs Frequency



PC01651F

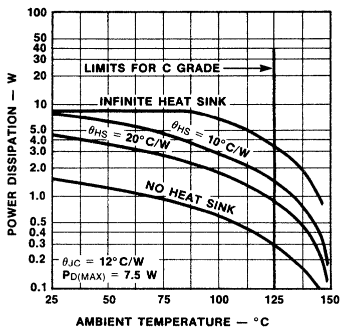
Line Transient Response



PC01671F

Typical Performance Curve For μA78MG and μA79MG

Worst Case Power Dissipation vs Ambient Temperature



PC01680F

Design Considerations

The μA78MG and μA79MG variable voltage regulators have an output voltage which varies from V_{CONT} to typically

$$V_I - 2.0\ V \text{ by } V_O = V_{CONT}\ \frac{(R1 + R2)}{R2}$$

The nominal reference in the μA78MG is 5.0 V and μA79MG is −2.23 V. If we allow 1.0 mA to flow in the control string to eliminate bias current effects, we can make R2 = 5 kΩ in the μA78MG. The output voltage is then: V_O = (R1 + R2) Volts, where R1 and R2 are in kΩs.

Example: If R2 = 5.0 kΩ and R1 = 10 kΩ then V_O = 15 V nominal, for the μA78MG; R2 = 2.2 kΩ and R1 = 12.8 kΩ then V_O = −15.2 V nominal, for the μA79MG.

By proper wiring of the feedback resistors, load regulation of the devices can be improved significantly.

Both μA78MG and μA79MG regulators have thermal overload protection from excessive power, internal short circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typical θ_{JC}	Max θ_{JC}	Typical θ_{JA}	Max θ_{JA}
Power Watt	8.0	12.0	70	75

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$\frac{T_{J\ Max} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

$T_A + P_D\theta_{JA}$ (Without heat sink)

Where

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JC} = Junction-to-case thermal resistance
- θ_{CA} = Case-to-ambient thermal resistance
- θ_{CS} = Case-to-heat sink thermal resistance
- θ_{SA} = Heat sink-to-ambient thermal resistance
- θ_{JA} = Junction-to-ambient thermal resistance

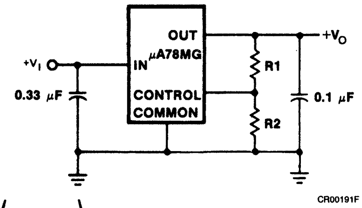
Typical Applications for μA78MG (Note 1)

Bypass capacitors are recommended for stable operation of the μA78MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (0.33 μF on the input, 0.1 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

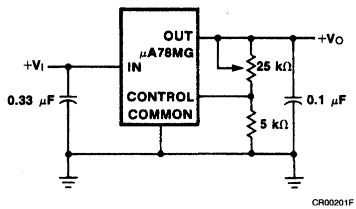
Note
1. All resistor values in ohms.

Basic Positive Regulator

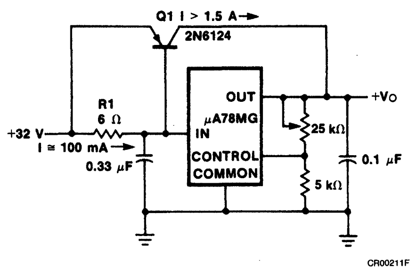


$$V_O = V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

Positive 5.0 V to 30 V Adjustable Regulator



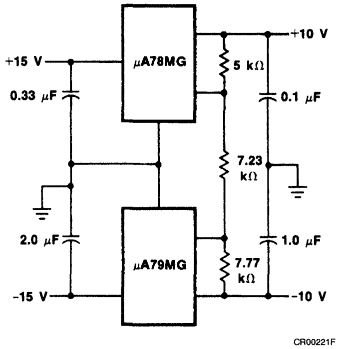
Positive 5.0 V to 30 V Adjustable Regulator $I_O > 1.5$ A



$$R1 = \frac{\beta V_{BE(Q1)}}{I_{R\ Max(\beta)} - I_O}$$

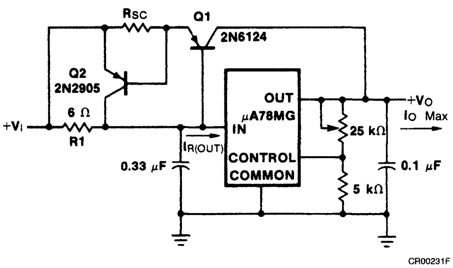
Typical Applications for μA78MG (Note 1) (Cont.)

± 10 V, 500 mA Dual Tracking Regulator



Note
External series pass device is not short circuit protected.

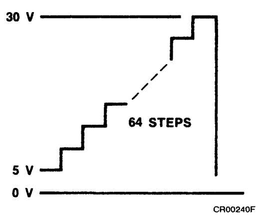
Positive High Current Short Circuit Protected Regulator



$$R1 = \frac{\beta V_{BE(Q1)}}{V_{R\ Max}(\beta + 1) - I_{O\ Max}}$$

If load is not ground referenced, connect reverse biased diodes from outputs to ground.

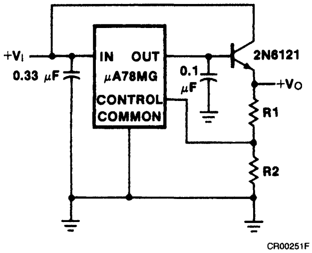
Output Waveform

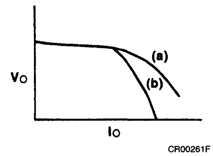


Note
1. All resistor values in ohms.

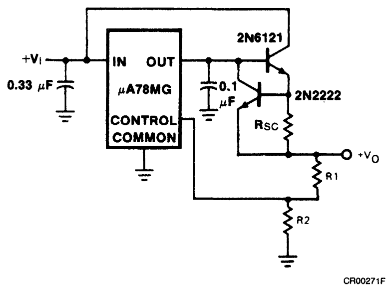
Positive High-Current Voltage Regulator

External Series Pass (a)





Short-Circuit Limit (b)



Typical Applications for μA79MG (Note 1)

Bypass capacitors are recommended for stable operation of the μA79MG over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.0 μF on the input, 1.0 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

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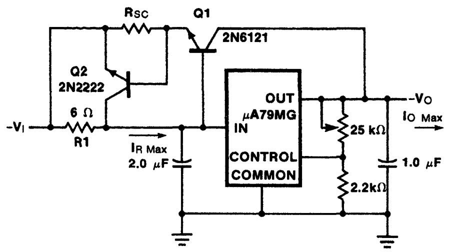
Typical Applications for μA79MG (Note 1) (Cont.)

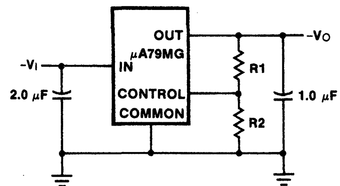
Negative High Current Short Circuit Protected Regulator



CR00281F

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{R\ Max(\beta)} - I_{O\ Max}}$$

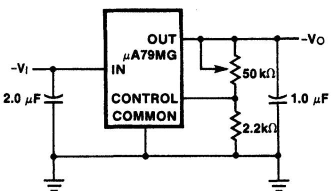
Basic Negative Regulator



CR00291F

$$V_O = -V_{CONT}\left(\frac{R1 + R2}{R2}\right)$$

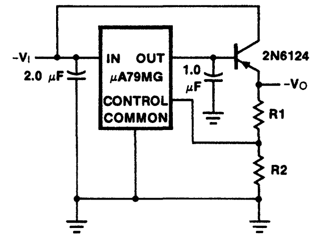
−30 V to −2.2 V Adjustable Regulator



CR00301F

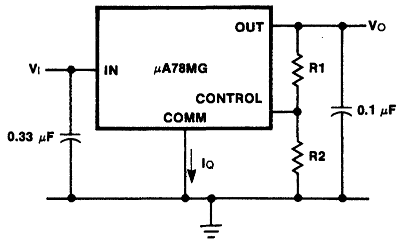
Note
1. All resistor values in ohms.

Negative High Current Voltage Regulator External Series Pass



CR00311F

μA78MG Test Circuit 1

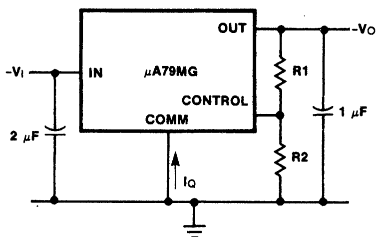


CR00321F

$$V_O = \left(\frac{R1 + R2}{R2}\right)V_{CONT}$$

V_{CONT} Nominally = 5 V

μA79MG Test Circuit 2



CR00331F

$$V_O = \left(\frac{R1 + R2}{R2}\right)V_{CONT}$$

V_{CONT} Nominally = −2.23 V

Recommended R2 current ≈ 1 mA
∴R2 = 5 kΩ (μA78MG)
R2 = 2.2 kΩ (μA79MG)

FAIRCHILD

A Schlumberger Company

μA78M00 Series 3-Terminal Positive Voltage Regulators

Linear Division Voltage Regulators

Description

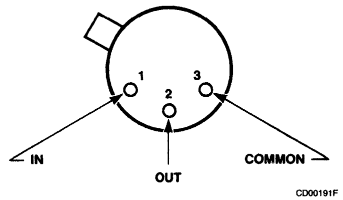
The μA78M00 series of 3-terminal medium current positive voltage regulators is constructed using the Fairchild Planar Epitaxial process. These regulators employ internal current-limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver in excess of 0.5 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Available In JEDEC TO-220 And TO-39 Packages**
- **Output Voltages Of 5 V, 6 V, 8 V, 12 V, 15 V, And 24 V**
- **Available In Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
TO-39 Metal Can	-65°C to +175°C
TO-220 Package	-65°C to +150°C
Operating Junction Temperature Range	
Extended (μA78M00M)	-55°C to +150°C
Commercial (μA78M00C)	0°C to +150°C
Lead Temperature	
TO-39 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 60 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0 V to 15 V	35 V
24 V	40 V

Connection Diagram TO-39 Package (Top View)

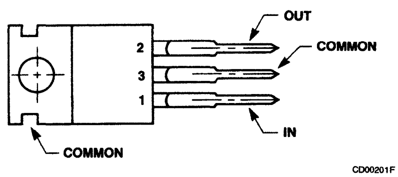


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA78M05HM	FC	Metal
μA78M06HM	FC	Metal
μA78M08HM	FC	Metal
μA78M12HM	FC	Metal
μA78M15HM	FC	Metal
μA78M24HM	FC	Metal
μA78M05HC	FC	Metal
μA78M06HC	FC	Metal
μA78M08HC	FC	Metal
μA78M12HC	FC	Metal
μA78M15HC	FC	Metal
μA78M24HC	FC	Metal

Connection Diagram TO-220 Package (Top View)



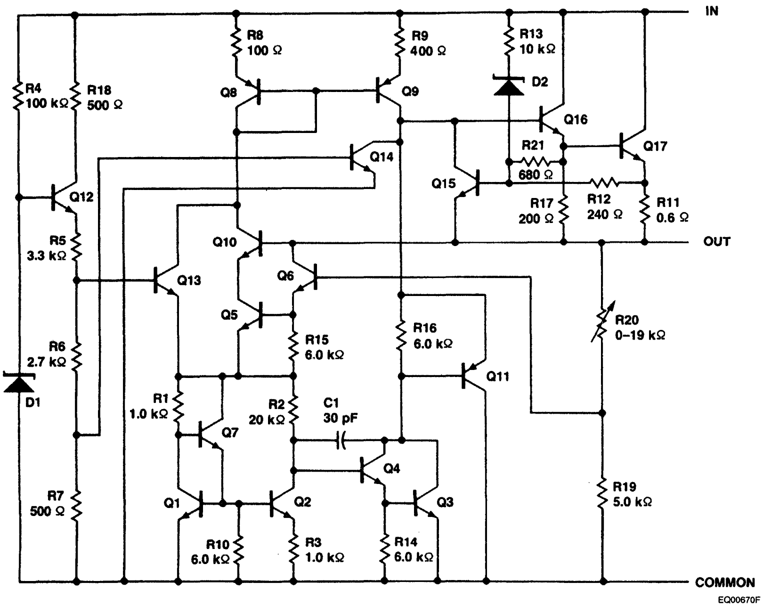
Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA78M05UC	GH	Molded Power Pack
μA78M06UC	GH	Molded Power Pack
μA78M08UC	GH	Molded Power Pack
μA78M12UC	GH	Molded Power Pack
μA78M15UC	GH	Molded Power Pack
μA78M24UC	GH	Molded Power Pack

6

Equivalent Circuit



μA78M05

Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = 10$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$7.0\ V \leqslant V_I \leqslant 25\ V$, $I_O = 200$ mA		3.0	50	mV
				$8.0\ V \leqslant V_I \leqslant 20\ V$, $I_O = 200$ mA		1.0	25	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leqslant I_O \leqslant 500\ mA$		20	50	mV
				$5.0\ mA \leqslant I_O \leqslant 200\ mA$		10	25	
V_O	Output Voltage		$8.0\ V \leqslant V_I \leqslant 20\ V$, $5.0\ mA \leqslant I_O \leqslant 350\ mA$		4.7		5.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	7.0	mA
ΔI_Q	Quiescent Current Change	with line	$8.0\ V \leqslant V_I \leqslant 25\ V$, $I_O = 200$ mA				0.8	mA
		with load	$5.0\ mA \leqslant I_O \leqslant 350\ mA$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leqslant f \leqslant 100\ kHz$			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 125$ mA, $T_J = 25°C$		62	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0	2.5	V

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μA78M05 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 10$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			300	600	mA
I_{pk}	Peak Output Current	$T_J = 25°C$		0.5	0.7	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/ V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

μA78M05C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 10$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$7.0\ V \leq V_I \leq 25$ V, $I_O = 200$ mA		3.0	100	mV
				$8.0\ V \leq V_I \leq 20$ V, $I_O = 200$ mA		1.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 500$ mA		20	100	mV
				$5.0\ mA \leq I_O \leq 200$ mA		10	50	
V_O	Output Voltage		$7.0\ V \leq V_I \leq 20$ V, $5.0\ mA \leq I_O \leq 350$ mA		4.75		5.25	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$8.0\ V \leq V_I \leq 25$ V, $I_O = 200$ mA				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 125$ mA, $T_J = 25°C$		62	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			300		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.0		mV/°C

μA78M06

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 11$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		5.75	6.0	6.25	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.0\ V \leq V_I \leq 25\ V$, $I_O = 200$ mA		5.0	60	mV
				$9.0\ V \leq V_I \leq 20\ V$, $I_O = 200$ mA		1.5	30	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 500$ mA		20	60	mV
				$5.0\ mA \leq I_O \leq 200$ mA		10	30	
V_O	Output Voltage		$9.0\ V \leq V_I \leq 21$ V, $5.0\ mA \leq I_O \leq 350$ mA		5.7		6.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	7.0	mA
ΔI_Q	Quiescent Current Change	with line	$9.0\ V \leq V_I \leq 25$ V, $I_O = 200$ mA				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$		59	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0	2.5	V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			300	600	mA
I_{pk}	Peak Output Current		$T_J = 25°C$		0.5	0.7	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/V_O
				$+25°C \leq T_A \leq +125°C$			0.3	

μA78M06C

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 11$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		5.75	6.0	6.25	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.0\ V \leq V_I \leq 25\ V$, $I_O = 200$ mA		5.0	100	mV
				$9.0\ V \leq V_I \leq 20\ V$, $I_O = 200$ mA		1.5	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 500$ mA		20	120	mV
				$5.0\ mA \leq I_O \leq 200$ mA		10	60	
V_O	Output Voltage		$8.0\ V \leq V_I \leq 21$ V, $5.0\ mA \leq I_O \leq 350$ mA		5.7		6.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$9.0\ V \leq V_I \leq 25$ V, $I_O = 200$ mA				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.5	

μA78M06C (Cont.)
Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 11 V, I_O = 350 mA, C_I = 0.33 μF, C_O = 0.1 μF unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
N_O	Noise	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		45		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, I_O = 125 mA, T_J = 25°C	59	80		dB
V_{DO}	Dropout Voltage	T_A = 25°C		2.0		V
I_{OS}	Output Short Circuit Current	T_J = 25°C, V_I = 35 V		270		mA
I_{pk}	Peak Output Current	T_J = 25°C		700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	I_O = 5.0 mA		0.5		mV/°C

μA78M08
Electrical Characteristics −55°C ≤ T_A ≤ 125°C, V_I = 14 V, I_O = 350 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	10.5 V ≤ V_I ≤ 25 V, I_O = 200 mA		6.0	60	mV
				11 V ≤ V_I ≤ 20 V, I_O = 200 mA		2.0	30	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	5.0 mA ≤ I_O ≤ 500 mA		25	80	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	40	
V_O	Output Voltage		11.5 V ≤ V_I ≤ 23 V, 5.0 mA ≤ I_O ≤ 350 mA		7.6		8.4	V
I_Q	Quiescent Current		T_J = 25°C			4.6	7.0	mA
ΔI_Q	Quiescent Current Change	with line	11.5 V ≤ V_I ≤ 25 V, I_O = 200 mA				0.8	mA
		with load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, T_J = 25°C		56	80		dB
V_{DO}	Dropout Voltage		T_A = 25°C			2.0	2.5	V
I_{OS}	Output Short Circuit Current		T_J = 25°C, V_I = 35 V			300	600	mA
I_{pk}	Peak Output Current		T_J = 25°C		0.5	0.7	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA	−55°C ≤ T_A ≤ +25°C			0.4	mV/°C
				+25°C ≤ T_A ≤ +125°C			0.3	

μA78M08C

Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 14 V, I_O = 350 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		T_J = 25°C		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	10.5 V ≤ V_I ≤ 25 V, I_O = 200 mA		6.0	100	mV
				11 V ≤ V_I ≤ 20 V, I_O = 200 mA		2.0	50	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	5.0 mA ≤ I_O ≤ 500 mA		25	160	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	80	
V_O	Output Voltage		10.5 V ≤ V_I ≤ 23 V, 5.0 mA ≤ I_O ≤ 350 mA		7.6		8.4	V
I_Q	Quiescent Current		T_J = 25°C			4.6	8.0	mA
ΔI_Q	Quiescent Current Change	with line	10.5 V ≤ V_I ≤ 25 V, I_O = 200 mA				0.8	mA
		with load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			52		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, T_J = 25°C		56	80		dB
V_{DO}	Dropout Voltage		T_A = 25°C			2.0		V
I_{OS}	Output Short Circuit Current		T_J = 25°C, V_I = 35 V			250		mA
I_{pk}	Peak Output Current		T_J = 25°C			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			0.5		mV/°C

μA78M12

Electrical Characteristics −55°C ≤ T_A ≤ 125°C, V_I = 19 V, I_O = 350 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		T_J = 25°C		11.5	12.0	12.5	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	14.5V ≤ V_I ≤ 30 V, I_O = 200 mA		8.0	60	mV
				16 V ≤ V_I ≤ 25 V, I_O = 200 mA		2.0	30	mV
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	5.0 mA ≤ I_O ≤ 500 mA		25	120	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	60	
V_O	Output Voltage		15.5 V ≤ V_I ≤ 27 V, 5.0 mA ≤ I_O ≤ 350 mA		11.4		12.6	V
I_Q	Quiescent Current		T_J = 25°C			4.8	7.0	mA
ΔI_Q	Quiescent Current Change	with line	15 V ≤ V_I ≤ 30 V, I_O = 200 mA				0.8	mA
		with load	5.0 mA ≤ I_O ≤ 350 mA				0.5	mA

μA78M12 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
N_O	Noise	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $V_I = 17$ V, $I_O = 125$ mA, $T_J = 25°C$		55	80		dB
V_{DO}	Dropout Voltage	$T_A = 25°C$			2.0	2.5	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			300	600	mA
I_{pk}	Peak Output Current	$T_J = 25°C$		0.5	0.7	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/ V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

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μA78M12C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		11.5	12.0	12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	14.5 V $\leq V_I \leq$ 30 V, $I_O = 200$ mA		8.0	100	mV
				16 V $\leq V_I \leq$ 25 V, $I_O = 200$ mA		2.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA $\leq I_O \leq$ 500 mA		25	240	mV
				5.0 mA $\leq I_O \leq$ 200 mA		10	120	
V_O	Output Voltage		14.5 V $\leq V_I \leq$ 27 V, 5.0 mA $\leq I_O \leq$ 350 mA		11.4		12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			4.8	8.0	mA
ΔI_Q	Quiescent Current Change	with line	14.5 V $\leq V_I \leq$ 30 V, $I_O = 200$ mA				0.8	mA
		with load	5.0 mA $\leq I_O \leq$ 350 mA				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz			75		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $V_I = 17$ V, $T_J = 25°C$		55	80		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			240		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.0		mV/°C

μA78M15
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		14.4	15.0	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	17.5 V ≤ V_I ≤ 30 V, I_O = 200 mA		10	60	mV
				20 V ≤ V_I ≤ 28 V, I_O = 200 mA		3.0	30	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 500 mA		25	150	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	75	
V_O	Output Voltage		18.5 V ≤ V_I ≤ 30 V, 5.0 mA ≤ I_O ≤ 350 mA		14.25		15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			4.8	7.0	mA
ΔI_Q	Quiescent Current Change	with line	18.5 V ≤ V_I ≤ 30 V, I_O = 200 mA				0.8	mA
		with load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, V_I = 20 V, T_J = 25°C		54	70		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0	2.5	V
I_{OS}	Output Short Circuit Current		T_J = 25°C, V_I = 35 V			300	600	mA
I_{pk}	Peak Output Current		$T_J = 25°C$		0.5	0.7	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA	−55°C ≤ T_A ≤ +25°C			0.4	mV/°C/V_O
				+25°C ≤ T_A ≤ +125°C			0.3	

μA78M15C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$		14.4	15.0	15.6	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	17.5 V ≤ V_I ≤ 30 V, I_O = 200 mA		10	100	mV
			20 V ≤ V_I ≤ 28 V, I_O = 200 mA		3.0	50	
$V_{R\ LOAD}$	Load Regulation	$T_J = 25°C$	5.0 mA ≤ I_O ≤ 500 mA		25	300	mV
			5.0 mA ≤ I_O ≤ 200 mA		10	150	
V_O	Output Voltage	17.5 V ≤ V_I ≤ 30 V, 5.0 mA ≤ I_O ≤ 350 mA		14.25		15.75	V
I_Q	Quiescent Current	$T_J = 25°C$			4.8	8.0	mA

μA78M15C (Cont.)
Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$, $V_I = 23$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]	Min	Typ	Max	Unit
ΔI_Q	Quiescent Current Change	with line	$17.5 V \leqslant V_I \leqslant 30 V$, $I_O = 200$ mA			0.8	mA
		with load	$5.0 mA \leqslant I_O \leqslant 350 mA$			0.5	
N_O	Noise		$T_A = 25°C$, $10 Hz \leqslant f \leqslant 100 kHz$		90		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $V_I = 20$ V, $T_J = 25°C$	54	70		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$		2.0		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V		240		mA
I_{pk}	Peak Output Current		$T_J = 25°C$		700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA		1.0		mV/°C

μA78M24
Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = 33$ V, $I_O = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$27 V \leqslant V_I \leqslant 38 V$, $I_O = 200$ mA		10	60	mV
				$30 V \leqslant V_I \leqslant 36 V$, $I_O = 200$ mA		5.0	30	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0 mA \leqslant I_O \leqslant 500 mA$		30	240	mV
				$5.0 mA \leqslant I_O \leqslant 200 mA$		10	120	
V_O	Output Voltage		$28 V \leqslant V_I \leqslant 38 V$, $5.0 mA \leqslant I_O \leqslant 350 mA$		22.8		25.2	V
I_Q	Quiescent Current		$T_J = 25°C$			5.0	7.0	mA
ΔI_Q	Quiescent Current Change	with line	$28 V \leqslant V_I \leqslant 38 V$, $I_O = 200$ mA				0.8	mA
		with load	$5.0 mA \leqslant I_O \leqslant 350 mA$				0.5	
N_O	Noise		$T_A = 25°C$, $10 Hz \leqslant f \leqslant 100 kHz$			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $V_I = 30$ V, $T_J = 25°C$		50	70		dB
V_{DO}	Dropout Voltage		$T_A = 25°C$			2.0	2.5	V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			300	600	mA
I_{pk}	Peak Output Current		$T_J = 25°C$		0.5	0.7	1.4	mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA	$-55°C \leqslant T_A \leqslant +25°C$			0.4	mV/°C/V_O
				$+25°C \leqslant T_A \leqslant +125°C$			0.3	

μA78M24C

Electrical Characteristics 0°C ≤ T_A ≤ 125°C, V_I = 33 V, I_O = 350 mA, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.

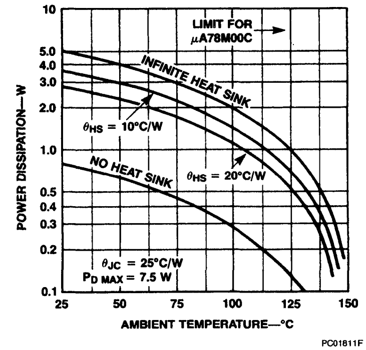
Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		T_J = 25°C		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		T_J = 25°C	27 V ≤ V_I ≤ 38 V, I_O = 200 mA		10	100	mV
				28 V ≤ V_I ≤ 36 V, I_O = 200 mA		5.0	50	
$V_{R\ LOAD}$	Load Regulation		T_J = 25°C	5.0 mA ≤ I_O ≤ 500 mA		30	480	mV
				5.0 mA ≤ I_O ≤ 200 mA		10	240	
V_O	Output Voltage		27 V ≤ V_I ≤ 38 V, 5.0 mA ≤ I_O ≤ 350 mA		22.8		25.2	V
I_Q	Quiescent Current		T_J = 25°C			5.0	8.0	mA
ΔI_Q	Quiescent Current Change	with line	27 V ≤ V_I ≤ 38 V, I_O = 200 mA				0.8	mA
		with load	5.0 mA ≤ I_O ≤ 350 mA				0.5	
N_O	Noise		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, I_O = 125 mA, V_I = 30 V, T_J = 25°C		50	70		dB
V_{DO}	Dropout Voltage		T_A = 25°C			2.0		V
I_{OS}	Output Short Circuit Current		T_J = 25°C, V_I = 35 V			240		mA
I_{pk}	Peak Output Current		T_J = 25°C			700		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		I_O = 5.0 mA			1.2		mV/°C

Note

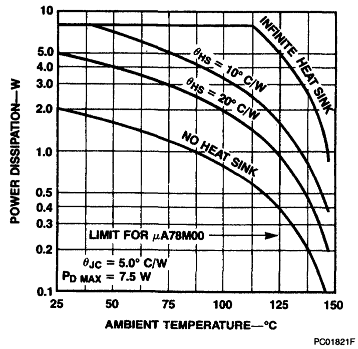
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (T_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves

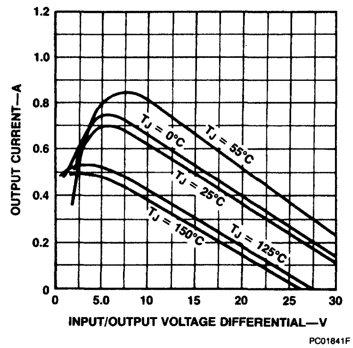
Worst Case Power Dissipation vs Ambient Temperature (TO-39)



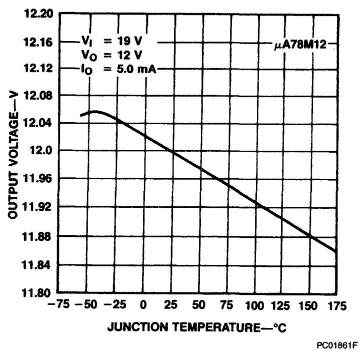
Worst Case Power Dissipation vs Ambient Temperature (TO-220)



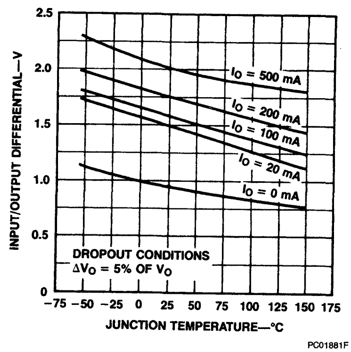
Peak Output Current vs Input/Output Voltage Differential



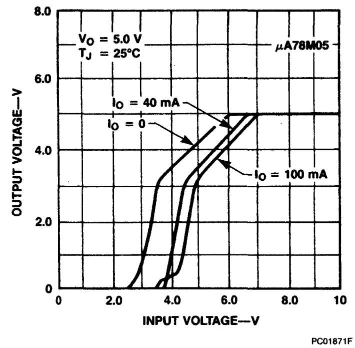
Output Voltage vs Junction Temperature



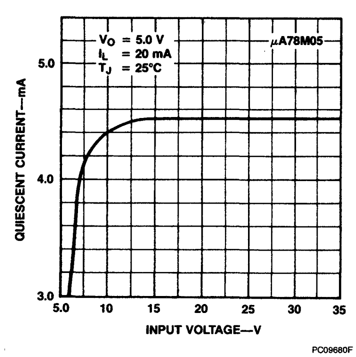
Dropout Voltage vs Junction Temperature



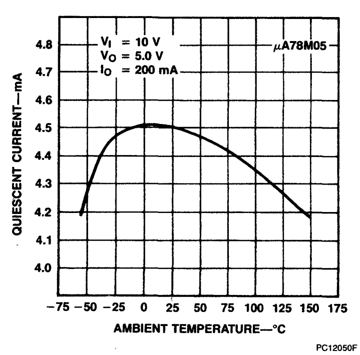
Dropout Characteristics



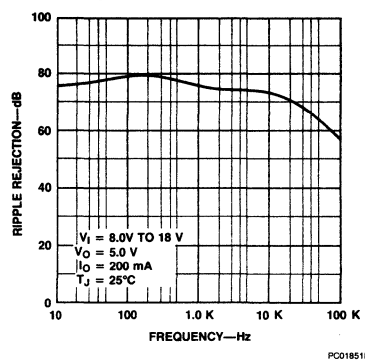
Quiescent Current vs Input Voltage



Quiescent Current vs Temperature



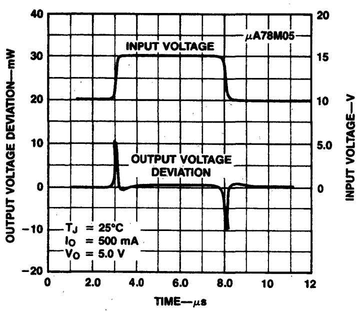
Ripple Rejection vs Frequency



Note
Other μA78M00 Series devices have similar curves.

Typical Performance Curves (Cont.)

Line Transient Response



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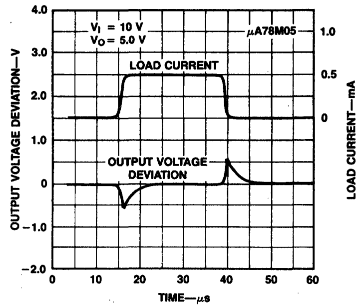
Load Transient Response



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Design Considerations

The μA78M00 fixed voltage regulator series has thermal-overload protection from excessive power, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output short circuit current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for μA78M00, 125°C for μA78M00C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC	Max θJC	Typ θJA	Max θJA
TO-39	18	25	120	140
TO-220	3.0	5.0	60	40

$$P_{D\ MAX} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\ Max} - T_A}{\theta J_A} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

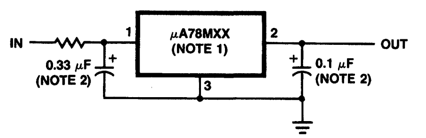
$= T_A + P_D\ \theta_{JA}$ (Without a heat sink)

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case-to-ambient thermal resistance
- θ_{CS} = Case-to-heat sink to resistance
- θ_{SA} = Heat sink-to-ambient thermal resistance
- θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

Fixed Output Regulator



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Notes

1. To specify an output voltage, substitute voltage value for "XX".
2. Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

FAIRCHILD
A Schlumberger Company

μA78S40 Universal Switching Regulator Subsystem

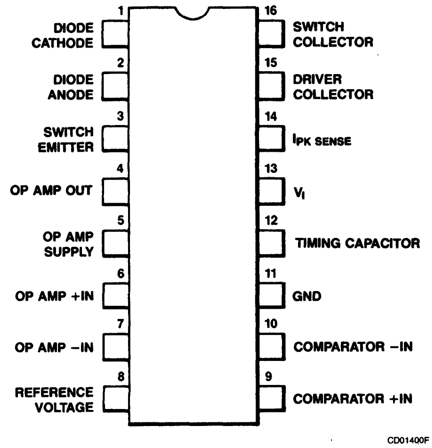
Linear Division Voltage Regulators

Description

The μA78S40 is a monolithic regulator subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high current, high voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external NPN or PNP transistors when currents in excess of 1.5 A or voltages in excess of 40 V are required. The device can be used for step-down, step-up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part count switching system and works extremely well in battery operated systems.

- **Step-Up, Step-Down or Inverting Switching Regulators**
- **Output Adjustable From 1.25 V to 40 V**
- **Peak Currents To 1.5 A Without External Transistors**
- **Operation From 2.5 V to 40 V Input**
- **Low Standby Current Drain**
- **80 dB Line And Load Regulation**
- **High Gain, High Current, Independent OP AMP**
- **Pulse Width Modulation With No Double Pulsing**

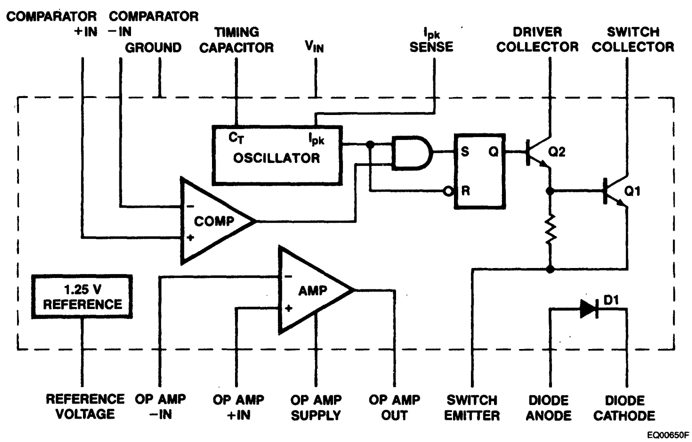
Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA78S40DM	7B	Ceramic DIP
μA78S40PV	9B	Molded DIP
μA78S40DC	7B	Ceramic DIP
μA78S40PC	9B	Molded DIP

Block Diagram



Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA78S40M)	−55°C to +125°C
Industrial (μA78S40V)	−40°C to +125°C
Commercial (μA78S40C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Input Voltage from V+ to V−	40 V
Input Voltage from V+ Op Amp to V−	40 V
Common Mode Input Range (Error Amplifier and Op Amp)	−0.3 to V+
Differential Input Voltage[3]	±30 V
Output Short Circuit Duration (Op Amp)	Indefinite
Current from V_{REF}	10 mA
Voltage from Switch Collectors to GND	40 V
Voltage from Switch Emitters to GND	40 V
Voltage from Switch Collectors to Emitter	40 V
Voltage from Power Diode to GND	40 V
Reverse Power Diode Voltage	40 V
Current through Power Switch	1.5 A
Current through Power Diode	1.5 A

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. For supply voltages less than 30 V, the absolute maximum voltage is equal to the supply voltage.

Functional Description

The μA78S40 is a variable frequency, variable duty cycle device. The initial switching frequency is set by the timing capacitor.[1] The initial duty cycle is 6:1. This switching frequency and duty cycle can be modified by two mechanisms — the current limit circuitry ($I_{pk\ sense}$) and the comparator.

The comparator modifies the OFF time. When the output voltage is correct, the comparator output is in the HIGH state and has no effect on the circuit operation. If the output voltage is too high then the comparator output goes LOW. In the LOW state the comparator inhibits the turn-on of the output stage switching transistors. As long as the comparator is LOW the system is in OFF time. As the output current rises the OFF time decreases. As the output current nears its maximum the OFF time approaches its minimum value. The comparator can inhibit several ON cycles, one ON cycle or any portion of an ON cycle. Once the ON cycle has begun the comparator cannot inhibit until the beginning of the next ON cycle.

The current limit modifies the ON time. The current limit is activated when a 300 mV potential appears between lead 13 (V_{CC}) and lead 14 (I_{pk}). This potential is intended to result when designed for peak current flows through R_{SC}. When the peak current is reached the current limit is turned on. The current limit circuitry provides for a quick end to ON time and the immediate start of OFF time.

Note
1. Oscillator frequency is set by a single external capacitor and may be varied over a range of 100 Hz to 100 kHz.

Generally the oscillator is free running but the current limit action tends to reset the timing cycle.

Increasing load results in more current limited ON time and less OFF time. The switching frequency increases with load current.

V_{FD} is the forward voltage drop across the internal power diode. It is listed on the data sheet as 1.25 V typical, 1.5 V maximum. If an external diode is used, then its own forward voltage drop must be used for V_{FD}.

V_{SAT} is the voltage across the switch element (output transistors Q1 and Q2) when the switch is closed or ON. This is listed on the data sheet as output saturation voltage.

Output saturation voltage 1 — defined as the switching element voltage for Q2 and Q1 in the Darlington configuration with collectors tied together. This applies to *Figure 1,* the step down mode.

Output saturation voltage 2 — switching element voltage for Q1 only when used as a transistor switch. This applies to *Figure 2,* the step up mode.

For the inverting mode, *Figure 3,* the saturation voltage of the external transistor should be used for V_{SAT}.

μA78S40

Electrical Characteristics T_A = Operating temperature range, V_I = 5.0 V, $V_{Op\ Amp}$ = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
General Characteristics							
I_{CC}	Supply Current (Op Amp Disconnected)	V_I = 5.0 V			1.8	3.5	mA
		V_I = 40 V			2.3	5.0	mA
I_{CC}	Supply Current (Op Amp Connected)	V_I = 5.0 V				4.0	mA
		V_I = 40 V				5.5	mA
Reference Section							
V_{REF}	Reference Voltage[1]	I_{REF} = 1.0 mA	Extend −55°C < T_A < +125°C, Comm 0 < T_A < +70°C, Indus −40°C < T_A < +85°C	1.180	1.245	1.310	V
$V_{R\ LINE}$	Reference Voltage Line Regulation	V_I = 3.0 V to V_I = 40 V, I_{REF} = 1.0 mA, T_A = 25°C			0.04	0.2	mV/V
$V_{R\ LOAD}$	Reference Voltage Load Regulation	I_{REF} = 1.0 mA to I_{REF} = 10 mA, T_A = 25°C			0.2	0.5	mV/mA
Oscillator Section							
I_{CHG}	Charging Current	V_I = 5.0 V, T_A = 25°C		20		50	μA
I_{CHG}	Charging Current	V_I = 40 V, T_A = 25°C		20		70	μA
I_{DISCHG}	Discharge Current	V_I = 5.0 V, T_A = 25°C		150		250	μA
I_{DISCHG}	Discharge Current	V_I = 40 V, T_A = 25°C		150		350	μA
V_{OSC}	Oscillator Voltage Swing	V_I = 5.0 V, T_A = 25°C			0.5		V
t_{on}/t_{off}	Ratio of Charge/ Discharge Time				6.0		μs/μs
Current Limit Section							
V_{CLS}	Current Limit Sense Voltage	T_A = 25°C		250		350	mV
Output Switch Section							
$V_{SAT\ 1}$	Output Saturation Voltage 1	I_{SW} = 1.0 A, *Figure 1*			1.1	1.3	V
$V_{SAT\ 2}$	Output Saturation Voltage 2	I_{SW} = 1.0 A, *Figure 2*			0.45	0.7	V
h_{FE}	Output Transistor Current Gain	I_C = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C			70		
I_L	Output Leakage Current	V_O = 40 V, T_A = 25°C			10		nA
Power Diode							
V_{FD}	Forward Voltage Drop	I_D = 1.0 A			1.25	1.5	V
I_{DR}	Diode Leakage Current	V_D = 40 V, T_A = 25°C			10		nA
Comparator							
V_{IO}	Input Offset Voltage	V_{CM} = V_{REF}			1.5	15	mV
I_{IB}	Input Bias Current	V_{CM} = V_{REF}			35	200	nA
I_{IO}	Input Offset Current	V_{CM} = V_{REF}			5.0	75	nA

μA78S40 (Cont.)

Electrical Characteristics T_A = Operating temperature range, V_I = 5.0 V, $V_{Op\ Amp}$ = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		V1 − 2	V
PSRR	Power Supply Rejection Ratio	V_I = 3.0 V to 40 V, T_A = 25°C	70	96		dB
Output Operational Amplifier						
V_{IO}	Input Offset Voltage	V_{CM} = 2.5 V		4.0	15	mV
I_{IB}	Input Bias Current	V_{CM} = 2.5 V		30	200	nA
I_{IO}	Input Offset Current	V_{CM} = 2.5 V		5.0	75	nA
A_{VS}+	Voltage Gain +	R_L = 2.0 kΩ to GND; V_O = 1.0 V to 2.5 V, T_A = 25°C	25	250		V/mV
A_{VS}−	Voltage Gain −	R_L = 2.0 kΩ to V+ (Op Amp) V_O = 1.0 V to 2.5 V, T_A = 25°C	25	250		V/mV
V_{CM}	Common Mode Voltage Range	T_A = 25°C	0		V_{CC} − 2	V
CMR	Common Mode Rejection	V_{CM} = 0 V to 3.0 V, T_A = 25°C	76	100		dB
PSRR	Power Supply Rejection Ratio	V+ Op Amp = 3.0 to 40 V, T_A = 25°C	76	100		dB
I_O+	Output Source Current	T_A = 25°C	75	150		mA
I_O−	Output Sink Current	T_A = 25°C	10	35		mA
SR	Slew Rate	T_A = 25°C		0.6		V/μs
V_{OL}	Output Voltage LOW	I_L = −5.0 mA, T_A = 25°C			1.0	V
V_{OH}	Output Voltage HIGH	I_L = 50 mA, T_A = 25°C	V + OP Amp −3.0 V			V

Note

1. Selected devices with tightened tolerance reference voltage available.

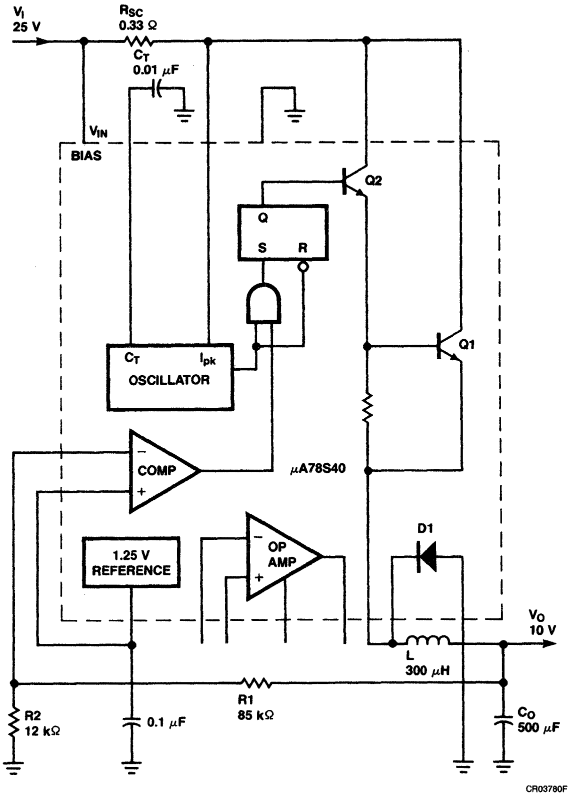
6

Design Formulas

CHARACTERISTIC	STEP-DOWN	STEP-UP	INVERTING	UNIT
$\frac{t_{on}}{t_{off}}$	$\frac{V_O + V_D}{V_I - V_{SAT} - V_O}$	$\frac{V_O + V_D - V_I}{V_I - V_{SAT}}$	$\frac{\lvert V_O \rvert + V_D}{V_I - V_{SAT}}$	
$(t_{on} + t_{off})$ Max	$\frac{1}{f_{Min}}$	$\frac{1}{f_{Min}}$	$\frac{1}{f_{Min}}$	μs
C_T	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$	$4 \times 10^{-5}\ t_{on}$	μF
I_{pk}	$2\ I_{O\ Max}$	$2\ I_{O\ Max} \cdot \frac{t_{on} + t_{off}}{t_{off}}$	$2\ I_{O\ Max} \cdot \frac{t_{on} + t_{off}}{t_{off}}$	A
L_{Min}	$\left(\frac{V_I - V_{SAT} - V_O}{I_{pk}}\right) t_{on\ Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\ Max}$	$\left(\frac{V_I - V_{SAT}}{I_{pk}}\right) t_{on\ Max}$	μH
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$	Ω
C_O	$\frac{I_{pk}\ (t_{on} + t_{off})}{8\ V_{ripple}}$	$\approx \frac{I_o}{V_{ripple}} \cdot t_{on}$	$\approx \frac{I_o}{V_{ripple}} \cdot t_{on}$	μF

Note
V_{SAT} = Saturation voltage of the switching element
V_D = Forward voltage of the flyback diode

Figure 1 Typical Step-Down Operational Performance (T_A = 25°C)

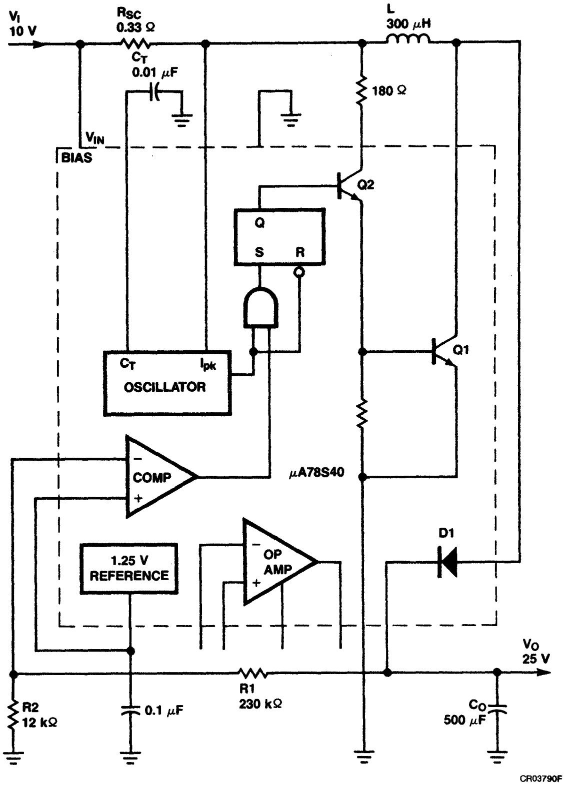


Characteristic	Condition	Typical Value
Output Voltage	I_O = 200 mA	10 V
Line Regulation	20 ≤ V_I ≤ 30 V	1.5 mV
Load Regulation	5.0 mA ≤ I_O	
	I_O ≤ 300 mA	3.0 mV
Max Output Current	V_O = 9.5 V	500 mA
Output Ripple	I_O = 200 mA	50 mV
Efficiency	I_O = 200 mA	74%
Standby Current	I_O = 200 mA	2.8 mA

Notes

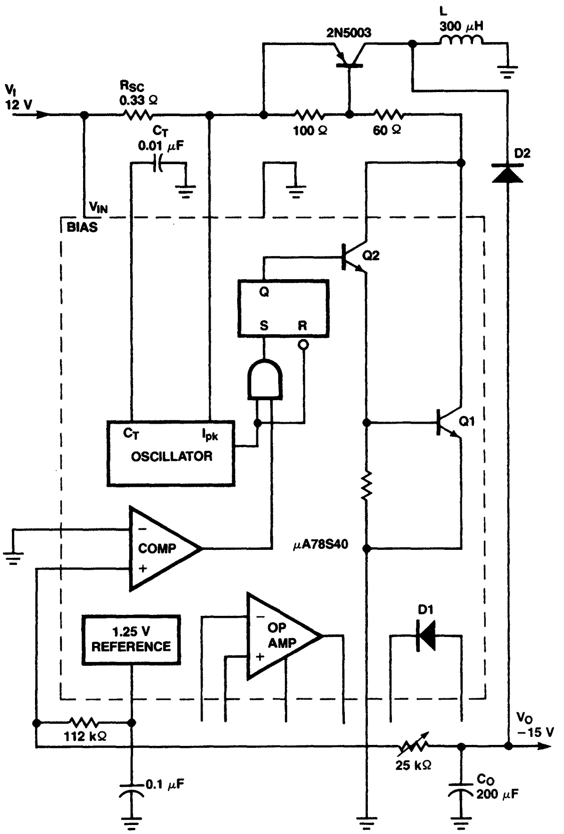
1. For I_O ≥ 200 mA use external diode to limit on-chip power dissipation.
2. It is recommended that the internal reference (lead 8) be bypassed by a 0.1 μF capacitor directly to (lead 11) the ground point of the μA78S40.

Figure 2 Typical Step-Up Operational Performance (T_A = 25°C)



Characteristic	Condition	Typical Value
Output Voltage	I_O = 50 mA	25 V
Line Regulation	5.0 V ≤ V_I ≤ 15 V	4.0 mV
Load Regulation	5.0 mA ≤ I_O	
	I_O ≤ 100 mA	2.0 mV
Max Output Current	V_O = 23.75 V	160 mA
Output Ripple	I_O = 50 mA	30 mV
Efficiency	I_O = 50 mA	79%
Standby Current	I_O = 50 mA	2.6 mA

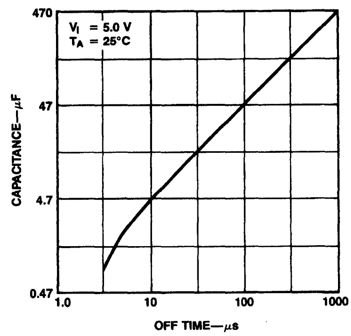
Figure 3 Typical Inversion Operational Performance (T_A = 25°C)



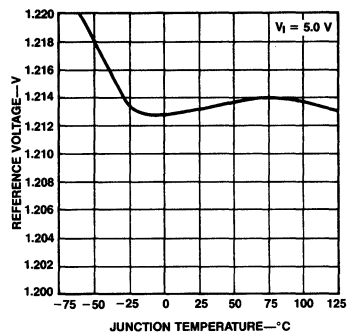
Characteristic	Condition	Typical Value
Output Voltage	I_O = 100 mA	−15 V
Line Regulation	8.0 V ⩽ V_I < 18 V	5.0 mV
Load Regulation	5.0 mA ⩽ I_O ⩽ 150 mA	3.0 mV
Max Output Current	V_O = 14.25 V	160 mA
Output Ripple	I_O = 100 mA	20 mV
Efficiency	I_O = 100 mA	70%
Standby Current	I_O = 100 mA	2.3 mA

Typical Performance Curves

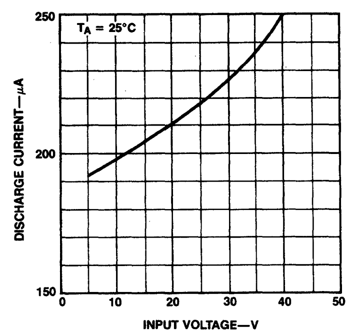
Capacitance vs OFF Time



Reference Voltage vs Junction Temperature

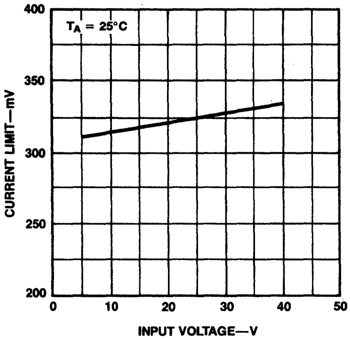


Discharge Current vs Input Voltage



Typical Performance Curves (Cont.)

Current Limit Sense Voltage vs Input Voltage



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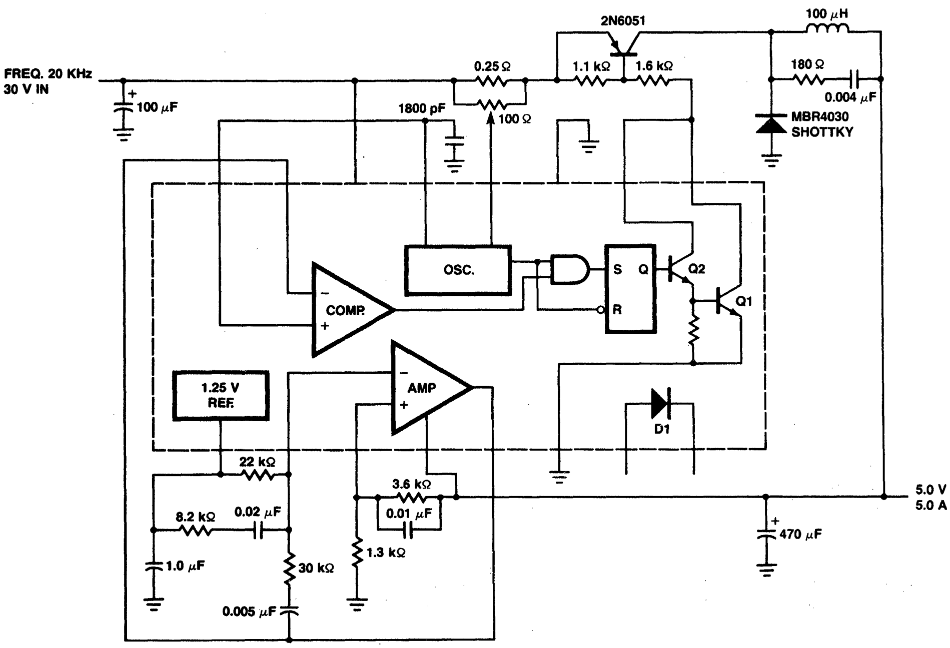
Typical Pulse Width Modulator Application



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μA7800 Series 3-Terminal Positive Voltage Regulators

Linear Division Voltage Regulators

Description

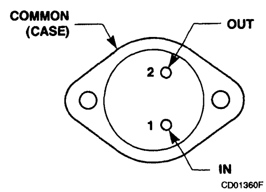
The μA7800 series of monolithic 3-terminal positive voltage regulators is constructed using the Fairchild Planar Epitaxial process. These regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **Output Current In Excess Of 1.0 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Available In JEDEC TO-220 And TO-3 Packages**
- **Output Voltages Of 5 V, 6 V, 8 V, 8.5 V, 12 V, 15 V, 18 V, And 24 V**
- **Available In Extended Temperature Range**

Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to +150°C
Operating Junction Temperature Range	
Extended (μA7800M)	−55°C to +150°C
Commercial (μA7800C)	0°C to +150°C
Lead Temperature	
TO-3 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
5.0 V to 18 V	35 V
24 V	40 V

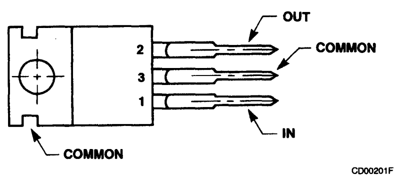
Connection Diagram TO-3 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA7805KM	HJ	Metal
μA7806KM	HJ	Metal
μA7808KM	HJ	Metal
μA7812KM	HJ	Metal
μA7815KM	HJ	Metal
μA7818KM	HJ	Metal
μA7824KM	HJ	Metal
μA7805KC	HJ	Metal
μA7806KC	HJ	Metal
μA7808KC	HJ	Metal
μA7812KC	HJ	Metal
μA7815KC	HJ	Metal
μA7818KC	HJ	Metal
μA7824KC	HJ	Metal

Connection Diagram TO-220 Package (Top View)

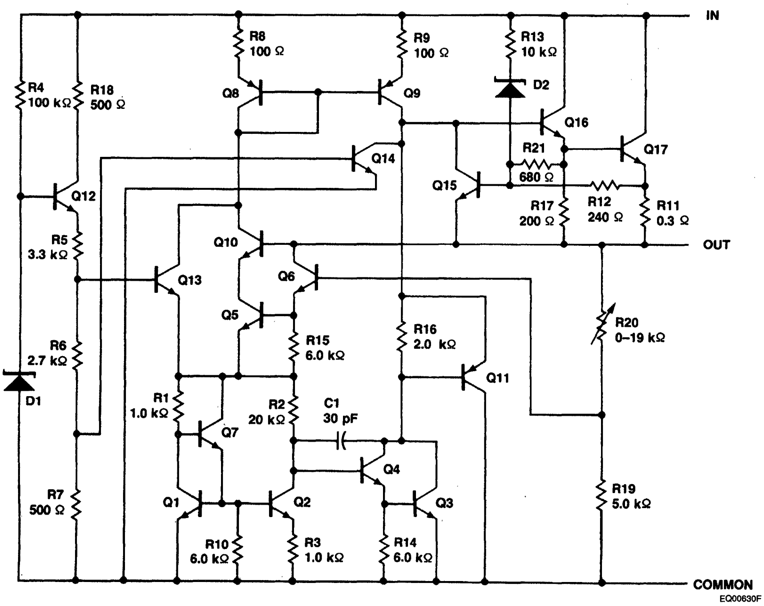


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA7805UC	GH	Molded Power Pack
μA7806UC	GH	Molded Power Pack
μA7808UC	GH	Molded Power Pack
μA7812UC	GH	Molded Power Pack
μA7815UC	GH	Molded Power Pack
μA7818UC	GH	Molded Power Pack
μA7824UC	GH	Molded Power Pack
μA7885UC	GH	Molded Power Pack
μA7805UC2	GH	Molded Power Pack
μA7812UC2	GH	Molded Power Pack

Equivalent Circuit



μA7805
Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = 10$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	$7.0\ V \leqslant V_I \leqslant 25\ V$		3.0	50	mV
			$8.0\ V \leqslant V_I \leqslant 12\ V$		1.0	25	
$V_{R\ LOAD}$	Load Regulation	$T_J = 25°C$	$5.0\ mA \leqslant I_O \leqslant 1.5\ A$		15	100	mV
			$250\ mA \leqslant I_O \leqslant 750\ mA$		5.0	25	
V_O	Output Voltage	$8.0\ V \leqslant V_I \leqslant 20\ V$ $5.0\ mA \leqslant I_O \leqslant 1.0\ A$ $P \leqslant 15\ W$		4.65		5.35	V
I_Q	Quiescent Current	$T_J = 25°C$			4.2	6.0	mA
ΔI_Q	Quiescent Current Change, with line	$8.0\ V \leqslant V_I \leqslant 25\ V$				0.8	mA
	Quiescent Current Change, with load	$5.0\ mA \leqslant I_O \leqslant 1.0\ A$				0.5	
N_O	Noise	$T_A = 25°C$, $10\ Hz \leqslant f \leqslant 100\ kHz$			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection	$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		68	78		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance	$f = 1.0$ kHz			17		mΩ

μA7805 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 10$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			0.75	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/ V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

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μA7805C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 10$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		4.8	5.0	5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$7.0\ V \leq V_I \leq 25$ V		3.0	100	mV
				$8.0\ V \leq V_I \leq 12$ V		1.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5$ A		15	100	mV
				$250\ mA \leq I_O \leq 750$ mA		5.0	50	
V_O	Output Voltage		$7.0\ V \leq V_I \leq 20$ V $5.0\ mA \leq I_O \leq 1.0$ A $P \leq 15$ W		4.75		5.25	V
I_Q	Quiescent Current		$T_J = 25°C$			4.2	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$7.0\ V \leq V_I \leq 25$ V				1.3	mA
		with load	$5.0\ mA \leq I_O \leq 1.0$ A				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			40		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		62	78		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0$ kHz			17		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			750		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$			1.1		mV/°C

μA7806C

Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$, $V_I = 11$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		5.75	6.0	6.25	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$8.0\ V \leqslant V_I \leqslant 25\ V$		5.0	120	mV
				$9.0\ V \leqslant V_I \leqslant 13\ V$		1.5	60	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leqslant I_O \leqslant 1.5\ A$		14	120	mV
				$250\ mA \leqslant I_O \leqslant 750\ mA$		4.0	60	
V_O	Output Voltage		$8.0\ V \leqslant V_I \leqslant 21\ V$ $5.0\ mA \leqslant I_O \leqslant 1.0\ A$ $P \leqslant 15\ W$		5.7		6.3	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$8.0\ V \leqslant V_I \leqslant 25\ V$				1.3	mA
		with load	$5.0\ mA \leqslant I_O \leqslant 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leqslant f \leqslant 100\ kHz$			45		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		59	75		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0$ kHz			19		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			550		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leqslant T_A \leqslant +125°C$			0.8		mV/°C

μA7808

Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = 14$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$10.5\ V \leqslant V_I \leqslant 25\ V$		6.0	80	mV
				$11\ V \leqslant V_I \leqslant 17\ V$		2.0	40	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leqslant I_O \leqslant 1.5\ A$		12	100	mV
				$250\ mA \leqslant I_O \leqslant 750\ mA$		4.0	40	
V_O	Output Voltage		$11.5\ V \leqslant V_I \leqslant 23\ V$ $5.0\ mA \leqslant I_O \leqslant 1.0\ A$ $P \leqslant 15\ W$		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	6.0	mA
ΔI_Q	Quiescent Current Change	with line	$11.5\ V \leqslant V_I \leqslant 25\ V$				0.8	mA
		with load	$5.0\ mA \leqslant I_O \leqslant 1.0\ A$				0.5	

μA7808 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 14$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
N_O	Noise	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		62	72		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance	f = 1.0 kHz			16		mΩ
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			0.75	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

μA7808C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 14$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		7.7	8.0	8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	10.5 V ≤ V_I ≤ 25 V		6.0	160	mV
				11 V ≤ V_I ≤ 17 V		2.0	80	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA ≤ I_O ≤ 1.5 A		12	160	mV
				250 mA ≤ I_O ≤ 750 mA		4.0	80	
V_O	Output Voltage		10.5 V ≤ V_I ≤ 23 V 5.0 mA ≤ I_O ≤ 1.0 A P ≤ 15 W		7.6		8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	with line	10.5 V ≤ V_I ≤ 25 V				1.0	mA
		with load	5.0 mA ≤ I_O ≤ 1.0 A				0.5	
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			52		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		56	72		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			16		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			450		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			0.8		mV/°C

μA7885C

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 15$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		8.15	8.5	8.85	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$10.5\ V \leq V_I \leq 25\ V$		6.0	170	mV
				$11\ V \leq V_I \leq 17\ V$		2.0	85	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	170	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	85	mV
V_O	Output Voltage		$11\ V \leq V_I \leq 23.5\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		8.1		8.9	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$10.5\ V \leq V_I \leq 25\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	mA
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			55		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		56	70		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0$ kHz			16		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			450		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			0.8		mV/°C

μA7812

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		11.5	12.0	12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$14.5\ V \leq V_I \leq 30\ V$		10	120	mV
				$16\ V \leq V_I \leq 22\ V$		3.0	60	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	120	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	60	
V_O	Output Voltage		$15.5\ V \leq V_I \leq 27\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		11.4		12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	6.0	mA
ΔI_Q	Quiescent Current Change	with line	$15\ V \leq V_I \leq 30\ V$				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	

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μA7812 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
N_O	Noise	$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		61	71		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance	f = 1.0 kHz			18		mΩ
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			0.75	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

μA7812C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 19$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		11.5	12.0	12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$14.5\ V \leq V_I \leq 30$ V		10	240	mV
				$16\ V \leq V_I \leq 22$ V		3.0	120	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5$ A		12	240	mV
				$250\ mA \leq I_O \leq 750$ mA		4.0	120	mV
V_O	Output Voltage		$14.5\ V \leq V_I \leq 27$ V $5.0\ mA \leq I_O \leq 1.0$ A $P \leq 15$ W		11.4		12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			4.3	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$14.5\ V \leq V_I \leq 30$ V				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0$ A				0.5	mA
N_O	Noise		$T_A = 25°C$, 10 Hz ≤ f ≤ 100 kHz			75		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		55	71		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			18		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			350		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.2		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.0		mV/°C

μA7815

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		14.4	15.0	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$17.5\ V \leq V_I \leq 30\ V$		11	150	mV
				$20\ V \leq V_I \leq 26\ V$		3.0	75	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	150	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	75	mV
V_O	Output Voltage		$18.5\ V \leq V_I \leq 30\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		14.25		15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			4.4	6.0	mA
ΔI_Q	Quiescent Current Change	with line	$18.5\ V \leq V_I \leq 30\ V$				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	mA
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			8.0	40	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400\ Hz$, $I_O = 350\ mA$, $T_J = 25°C$		60	70		dB
V_{DO}	Dropout Voltage		$I_O = 1.0\ A$, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance		$f = 1.0\ kHz$			19		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35\ V$			0.75		A
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0\ mA$	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/ V_O
				$+25°C \leq T_A \leq +125°C$			0.3	

μA7815C

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		14.4	15.0	15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$17.5\ V \leq V_I \leq 30\ V$		11	300	mV
				$20\ V \leq V_I \leq 26\ V$		3.0	150	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	300	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	150	mV
V_O	Output Voltage		$17.5\ V \leq V_I \leq 30\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		14.25		15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			4.4	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$17.5\ V \leq V_I \leq 30\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	mA

μA7815C (Cont.)

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 23$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
N_O	Noise	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz		90		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$	54	70		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$		2.0		V
R_O	Output Resistance	f = 1.0 kHz		19		mΩ
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V		230		A
I_{pk}	Peak Output Current	$T_J = 25°C$		2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA		1.0		mV/°C

μA7818

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 27$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		17.3	18.0	18.7	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	21 V $\leq V_I \leq$ 33 V		15	180	mV
				24 V $\leq V_I \leq$ 30 V		5.0	90	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA $\leq I_O \leq$ 1.5 A		12	180	mV
				250 mA $\leq I_O \leq$ 750 mA		4.0	90	mV
V_O	Output Voltage		22 V $\leq V_I \leq$ 33 V 5.0 mA $\leq I_O \leq$ 1.0 A P $\leq$ 15 W		17.1		18.9	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	6.0	mA
ΔI_Q	Quiescent Current Change	with line	22 V $\leq V_I \leq$ 33 V				0.8	mA
		with load	5.0 mA $\leq I_O \leq$ 1.0 A				0.5	mA
N_O	Noise		$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		59	69		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			22		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			0.75		A
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/V_O
				$+25°C \leq T_A \leq +125°C$			0.3	

μA7818C

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 27$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		17.3	18.0	18.7	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$21\ V \leq V_I \leq 33\ V$		15	360	mV
				$24\ V \leq V_I \leq 30\ V$		5.0	180	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	360	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	180	mV
V_O	Output Voltage		$21\ V \leq V_I \leq 33\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		17.1		18.9	V
I_Q	Quiescent Current		$T_J = 25°C$			4.5	8.0	mA
ΔI_Q	Quiescent Current Change	with line	$21\ V \leq V_I \leq 33\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	mA
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			110		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		53	69		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		$f = 1.0$ kHz			22		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			200		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.0		mV/°C

μA7824

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 33$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$27\ V \leq V_I \leq 38\ V$		18	240	mV
				$30\ V \leq V_I \leq 36\ V$		6.0	120	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	240	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	120	mV
V_O	Output Voltage		$28\ V \leq V_I \leq 38\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $P \leq 15\ W$		22.8		25.2	V
I_Q	Quiescent Current		$T_J = 25°C$			4.6	6.0	mA
ΔI_Q	Quiescent Current Change	with line	$28\ V \leq V_I \leq 38\ V$				0.8	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	mA

6

μA7824 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = 33$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]		Min	Typ	Max	Unit
N_O	Noise	$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz			8.0	40	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		56	66		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$			2.0	2.5	V
R_O	Output Resistance	f = 1.0 kHz			28		mΩ
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = 35$ V			0.75	1.2	A
I_{pk}	Peak Output Current	$T_J = 25°C$		1.3	2.2	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA	$-55°C \leq T_A \leq +25°C$			0.4	mV/°C/V_O
			$+25°C \leq T_A \leq +125°C$			0.3	

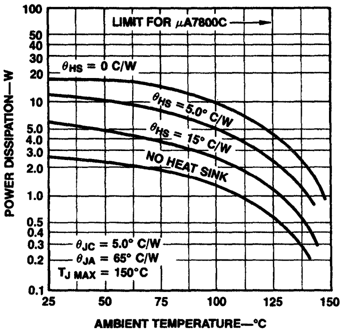
μA7824C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = 33$ V, $I_O = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		23.0	24.0	25.0	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	27 V $\leq V_I \leq$ 38 V		18	480	mV
				30 V $\leq V_I \leq$ 36 V		6.0	240	mV
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	5.0 mA $\leq I_O \leq$ 1.5 A		12	480	mV
				250 mA $\leq I_O \leq$ 750 mA		4.0	240	mV
V_O	Output Voltage		27 V $\leq V_I \leq$ 38 V, 5.0 mA $\leq I_O \leq$ 1.0 A, P $\leq$ 15 W		22.8		25.2	V
I_Q	Quiescent Current		$T_J = 25°C$			4.6	8.0	mA
ΔI_Q	Quiescent Current Change	with line	27 V $\leq V_I \leq$ 38 V				1.0	mA
		with load	5.0 mA $\leq I_O \leq$ 1.0 A				0.5	mA
N_O	Noise		$T_A = 25°C$, 10 Hz $\leq f \leq$ 100 kHz			170		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$		50	66		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			2.0		V
R_O	Output Resistance		f = 1.0 kHz			28		mΩ
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = 35$ V			150		mA
I_{pk}	Peak Output Current		$T_J = 25°C$			2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA			1.5		mV/°C

Note
1. For all tables, all characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

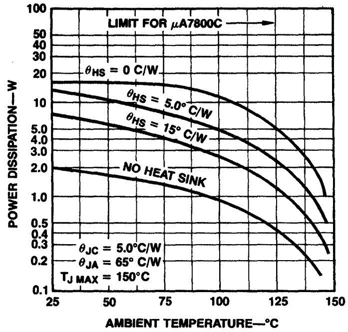
Typical Performance Curves

Worst Case Power Dissipation vs Ambient Temperature (TO-3)



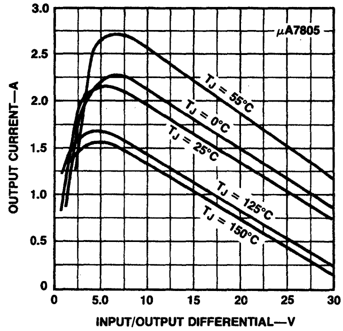
PC09260F

Worst Case Power Dissipation vs Ambient Temperature (TO-220)



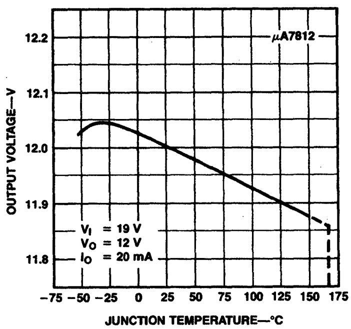
PC09270F

Peak Output Current vs Input/Output Voltage Differential



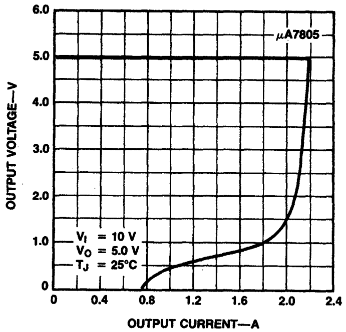
PC09320F

Output Voltage vs Junction Temperature



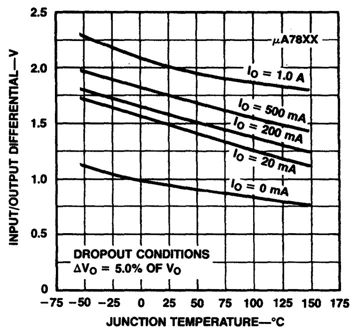
PC09350F

Current-Limiting Characteristics



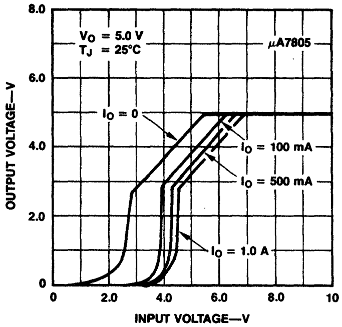
PC09360F

Dropout Voltage vs Junction Temperature



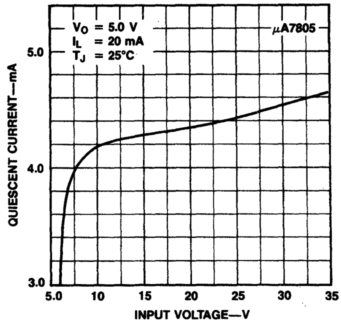
PC09280F

Dropout Characteristics



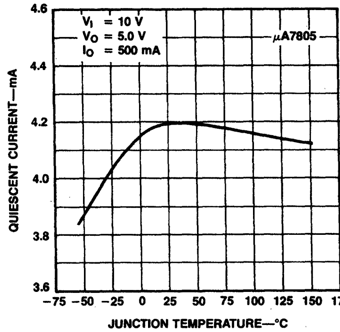
PC09300F

Quiescent Current vs Input Voltage



PC09340F

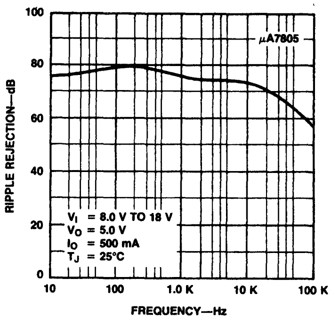
Quiescent Current vs Junction Temperature



PC09380F

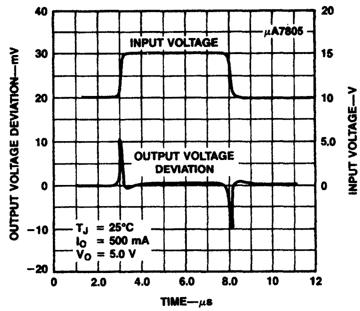
Typical Performance Curves (Cont.)

Ripple Rejection vs Frequency



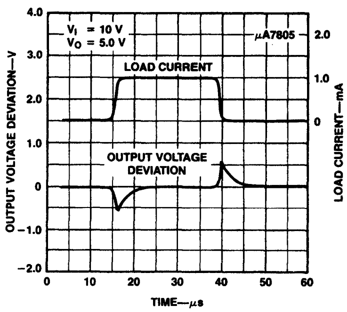
PC09290F

Line Transient Response



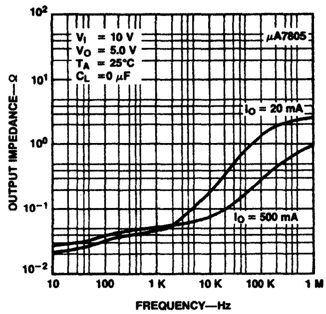
PC09310F

Load Transient Response



PC09330F

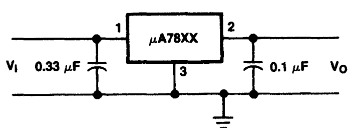
Output Impedance vs Frequency



PC09370F

Note
The other μA7800 series devices have similar curves.

DC Parameter Test Circuit



CR03630F

Design Considerations

The μA7800 fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the regulator's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for μA7800, 125°C for μA7800C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
TO-3	3.5	5.5	35	40
TO-220	3.0	5.0	40	60

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}}.\ \text{or}$$

$$= \frac{T_{J\ Max} T_A}{\theta_{JA}}\ \text{(Without heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$T_J = T_A + P_D(\theta_{JC} + \theta_{CA})$ or

$= T_A + P_D\theta_{JA}$ (Without heat sink)

Where:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Power Dissipation

θ_{JC} = Junction-to-case thermal resistance

θ_{CA} = Case-to-ambient thermal resistance

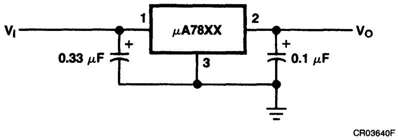
θ_{CS} = Case-to-heat sink to thermal resistance

θ_{SA} = Heat sink-to-ambient thermal resistance

θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

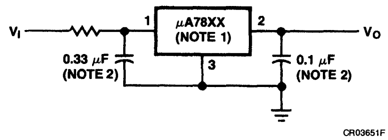
Fixed Output Regulator

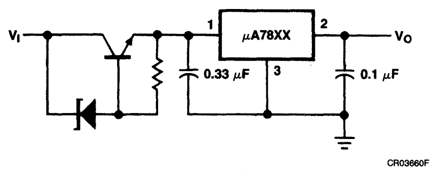


Notes

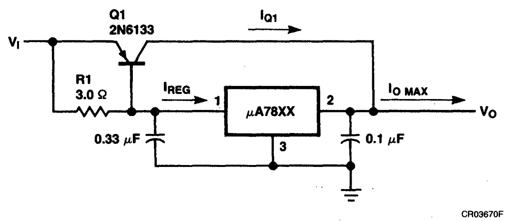
1. To specify an output voltage, substitute voltage value for "XX."
2. Bypass capacitors are recommended for optimum stability and transient response, and should be located as close as possible to the regulator.

High Input Voltage Circuits





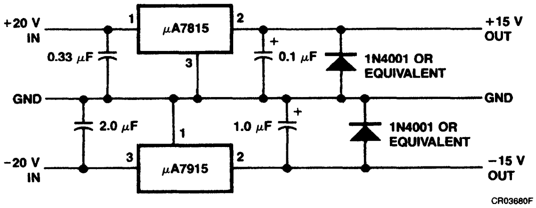
High Current Voltage Regulator



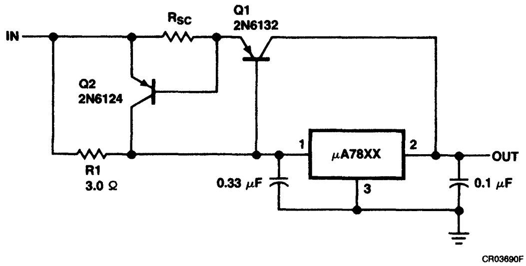
$$\beta(Q1) \geqslant \frac{I_{O\ Max}}{I_{REG\ Max}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)V_{BE(Q1)}}{I_{REG\ Max}\ (\beta + 1) - I_{O\ Max}}$$

Dual Supply Operational Amplifier Supply
(± 15 V@1.0 A)



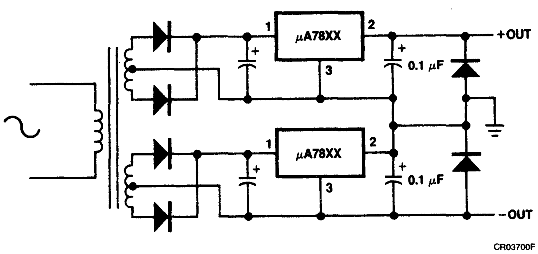
High Output Current, Short Circuit Protected



$$R_{SC} = \frac{0.8}{I_{SC}}$$

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REG\ Max}\ (\beta + 1) - I_{O\ Max}}$$

Positive and Negative Regulator



FAIRCHILD

A Schlumberger Company

μA79M00 Series 3-Terminal Negative Voltage Regulators

Linear Division Voltage Regulators

Description

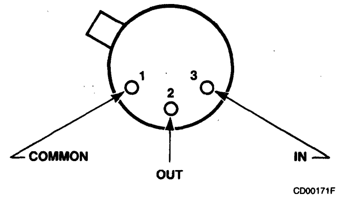
The μA79M00 series of 3-Terminal Medium Current Negative Voltage Regulators are constructed using the Fairchild Planar Epitaxial process. These regulators employ internal current-limiting, thermal shutdown, and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 0.5 A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

- **Output Current In Excess Of 0.5 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Available In JEDEC TO-220 And TO-39 Packages**
- **Output Voltages Of -5 V, -8 V, -12 V, and -15 V**

Absolute Maximum Ratings

Storage Temperature Range	
TO-39 Metal Can	-65°C to +175°C
TO-220 Package	-65°C to +150°C
Operating Junction Temperature Range	
Extended (μA79M00M)	-55°C to +150°C
Commercial (μA79M00AC)	0°C to +150°C
Lead Temperature	
TO-39 Metal Can (soldering, 60 s)	300°C
TO-220 Package (soldering, 60 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
-5.0 V to -15 V	-35 V

Connection Diagram
TO-39 Package
(Top View)

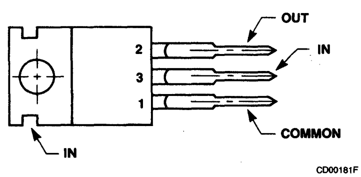


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA79M05HM	FC	Metal
μA79M08HM	FC	Metal
μA79M12HM	FC	Metal
μA79M15HM	FC	Metal
μA79M05AHC	FC	Metal
μA79M08AHC	FC	Metal
μA79M12AHC	FC	Metal
μA79M15AHC	FC	Metal

Connection Diagram
TO-220 Package
(Top View)

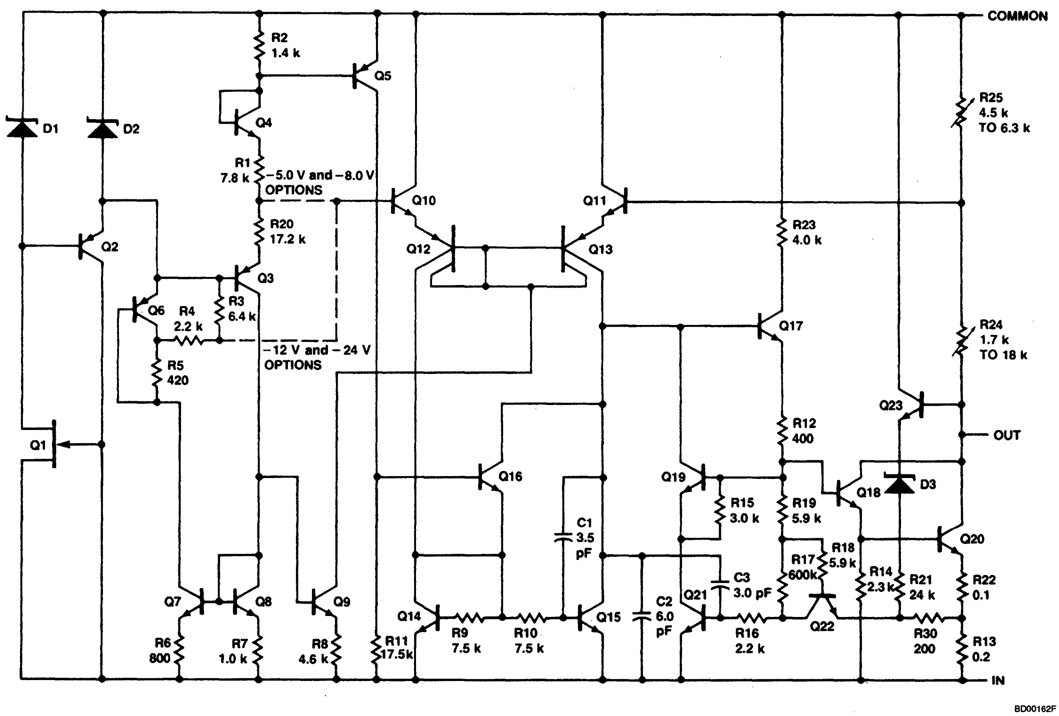


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA79M05AUC	GH	Molded Power Pack
μA79M08AUC	GH	Molded Power Pack
μA79M12AUC	GH	Molded Power Pack
μA79M15AUC	GH	Molded Power Pack

Equivalent Circuit



μA79M05H

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -10$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		−5.2	−5.0	−4.8	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-25\ V \leq V_I \leq -7.0$ V		7.0	50	mV
				$-18\ V \leq V_I \leq -8.0$ V		3.0	30	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500$ mA			75	100	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350$ mA			50		
V_O	Output Voltage		$-25\ V \leq V_I \leq -7.0$ V, $5.0\ mA \leq I_O \leq 350$ mA, $P_D \leq 4.0$ W		−5.25		−4.75	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-25\ V \leq V_I \leq -8.0$ V				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			25	80	$\mu V/V_O$

μA79M05H (Cont.)

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -10$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic	Condition[3]	Min	Typ	Max	Unit
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$	50			dB
V_{DO}	Dropout Voltage	$T_J = 25°C$		1.1	2.3	V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = -35$ V			0.6	A
I_{pk}	Peak Output Current	$V_I - V_O = 10$ V, $T_J = 25°C$	0.5	0.65	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$			0.3	mV/°C/ V_O

μA79M05AC

Electrical Characteristics $-0°C \leq T_A \leq 125°C$, $V_I = -10$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-5.2	-5.0	-4.8	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-25\ V \leq V_I \leq -7.0$ V		7.0	50	mV
				$-18\ V \leq V_I \leq -8.0$ V		3.0	30	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500$ mA			75	100	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350$ mA				50	
V_O	Output Voltage		$-25\ V \leq V_I \leq -7.0$ V, $5.0\ mA \leq I_O \leq 350$ mA, $P_D \leq 4.0$ W		-5.25		-4.75	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-25\ V \leq V_I \leq -8.0$ V				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			125		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$		50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.1		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -30$ V			140		mA
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$			650		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$			0.4		mV/°C

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μA79M08H

Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -14$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-8.3	-8.0	-7.7	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-25\ V \leq V_I \leq -10.5\ V$		8.0	80	mV
				$-21\ V \leq V_I \leq -11\ V$		4.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500\ mA$			90	160	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350\ mA$			60		
V_O	Output Voltage		$-25\ V \leq V_I \leq -10.5\ V$, $5.0\ mA \leq I_O \leq 350\ mA$, $P_D \leq 4.0\ W$		-8.4		-7.6	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-25\ V \leq V_I \leq -10.5\ V$				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350\ mA$				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -13$ V, $I_O = 125$ mA, $T_J = 25°C$		50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -35$ V				0.6	A
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$		0.5	0.65	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$				0.3	$mV/°C/V_O$

μA79M08AC

Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -14$ V, $I_O = 350$ mA, $C_I = 2$ μF, $C_O = 1$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-8.3	-8.0	-7.7	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-25\ V \leq V_I \leq -10.5\ V$		8.0	80	mV
				$-21\ V \leq V_I \leq -11\ V$		4.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500\ mA$			90	160	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350\ mA$			60		
V_O	Output Voltage		$-25\ V \leq V_I \leq -10.5\ V$, $5.0\ mA \leq I_O \leq 350\ mA$, $P_D \leq 4.0\ W$		-8.4		-7.6	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-25\ V \leq V_I \leq -10.5\ V$				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350\ mA$				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			200		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f=2400$ Hz, $V_I = -13$ V, $I_O = 125$ mA, $T_J = 25°C$		50			dB

μA79M08AC (Cont.)
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -14$ V, $I_O = 350$ mA, $C_I = 2$ μF, $C_O = 1$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic	Condition[3]	Min	Typ	Max	Unit
V_{DO}	Dropout Voltage	$T_J = 25°C$		1.1		V
I_{OS}	Output Short Circuit Current	$T_J = 25°C$, $V_I = -30$ V		140		mA
I_{pk}	Peak Output Current	$V_I - V_O = 10$ V, $T_J = 25°C$		650		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$		0.6		mV/°C

μA79M12H
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-12.5	-12	-11.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-30\ V \leq V_I \leq -14.5$ V		9.0	80	mV
				$-25\ V \leq V_I \leq -15$ V		5.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500$ mA			65	240	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350$ mA			45		
V_O	Output Voltage		$-30\ V \leq V_I \leq -14.5$ V, $5.0\ mA \leq I_O \leq 350$ mA, $P_D \leq 4.0$ W		-12.6		-11.4	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-30\ V \leq V_I \leq -14.5$ V				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350$ mA				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			25	80	$\mu V/V_O$
$\Delta V_I - \Delta V_O$	Ripple Rejection		$V_I \leq -17$ V, $f = 2400$ Hz, $I_O = 125$ mA, $T_J = 25°C$		50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -35$ V				0.6	A
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$		0.5	0.65	1.4	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$				0.3	mV/°C/V_O

μA79M12AC
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic	Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$		-12.5	-12	-11.5	V
$V_{R\ LINE}$	Line Regulation	$T_J = 25°C$	$-30\ V \leq V_I \leq -14.5$ V		9.0	80	mV
			$-25\ V \leq V_I \leq -15$ V		5.0	50	

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μA79M12AC (Cont.)
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]	Min	Typ	Max	Unit
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500\ mA$		65	240	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350\ mA$		45		
V_O	Output Voltage		$-30\ V \leq V_I \leq -14.5\ V$, $5.0\ mA \leq I_O \leq 350\ mA$, $P_D \leq 4.0\ W$	−12.6		−11.4	V
I_Q	Quiescent Current		$T_J = 25°C$		1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-30\ V \leq V_I \leq -14.5\ V$			0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350\ mA$			0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$		300		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$V_I = -17$ V, f = 2400 Hz, $I_O = 125$ mA, $T_J = 25°C$	50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$		1.1		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -30$ V		140		mA
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$		650		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$		0.8		mV/°C

μA79M15H
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -23$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		−15.6	−15	−14.4	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-30\ V \leq V_I \leq -17.5\ V$		9.0	80	mV
				$-28\ V \leq V_I \leq -18\ V$		7.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leq I_O \leq 500\ mA$			65	240	mV
			$T_J = 25°C$, $5.0\ mA \leq I_O \leq 350\ mA$			45		
V_O	Output Voltage		$-30\ V \leq V_I \leq -17.5\ V$, $5.0\ mA \leq I_O \leq 350\ mA$, $P_D \leq 4.0\ W$		−15.75		−14.25	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-30\ V \leq V_I \leq -17.5\ V$				0.4	mA
		with load	$5.0\ mA \leq I_O \leq 350\ mA$				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $V_I = -20$ V, $I_O = 125$ mA, $T_J = 25°C$		50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.1	2.3	V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -35$ V				0.6	A
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$		0.5	0.65	1.4	A

μA79M15H (Cont.)
Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = -23$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic	Condition[3]	Min	Typ	Max	Unit
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $0°C \leqslant T_A \leqslant 125°C$			0.3	mV/°C/V_O

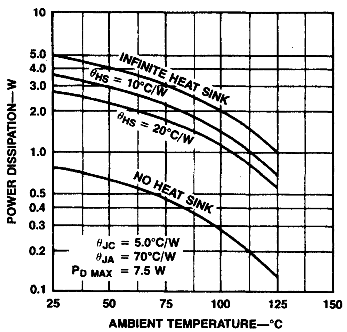
μA79M15AC
Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$, $V_I = -23$ V, $I_O = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[1,2]

Symbol	Characteristic		Condition[3]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		−15.6	−15	−14.4	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-30\ V \leqslant V_I \leqslant -17.5\ V$		9.0	80	mV
				$-28\ V \leqslant V_I \leqslant -18\ V$		7.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$, $5.0\ mA \leqslant I_O \leqslant 500\ mA$			65	240	mV
			$T_J = 25°C$, $5.0\ mA \leqslant I_O \leqslant 350\ mA$			45		
V_O	Output Voltage		$-30\ V \leqslant V_I \leqslant -17.5\ V$, $5.0\ mA \leqslant I_O \leqslant 350\ mA$, $P_D \leqslant 4.0\ W$		−15.75		−14.25	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-30\ V \leqslant V_I \leqslant -17.5\ V$				0.4	mA
		with load	$5.0\ mA \leqslant I_O \leqslant 350\ mA$				0.4	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leqslant f \leqslant 100\ kHz$			375		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -20$ V, $I_O = 125$ mA, $T_J = 25°C$		50			dB
V_{DO}	Dropout Voltage		$T_J = 25°C$			1.1		V
I_{OS}	Output Short Circuit Current		$T_J = 25°C$, $V_I = -30$ V			140		mA
I_{pk}	Peak Output Current		$V_I - V_O = 10$ V, $T_J = 25°C$			650		mA
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leqslant T_A \leqslant 125°C$			1.0		mV/°C

Notes
1. See Test Circuit.
2. The convention for negative regulators is the algebraic values, thus −15 V is less than −10 V.
3. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

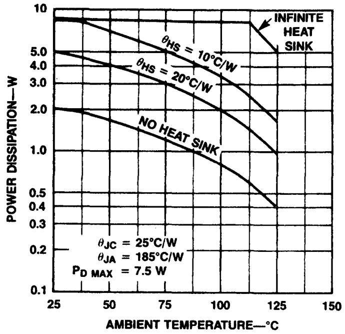
Typical Performance Curves

Worst Case Power Dissipation vs Ambient Temperature (TO-39)



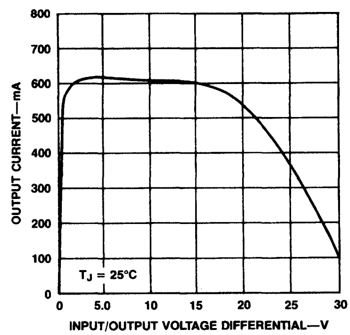
PC01791F

Worst Case Power Dissipation vs Ambient Temperature (TO-220)



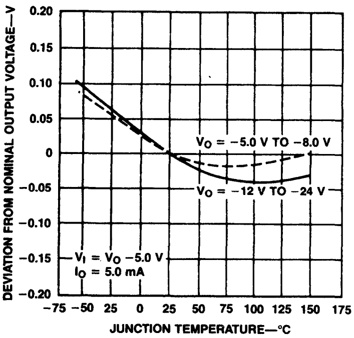
PC01801F

Peak Output Current vs Input/Output Voltage Differential



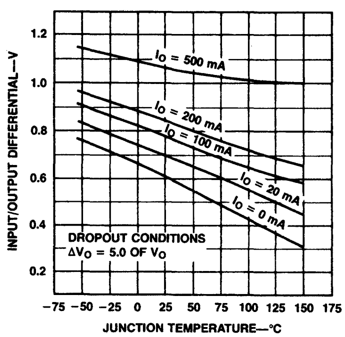
PC01711F

Output Voltage vs Junction Temperature



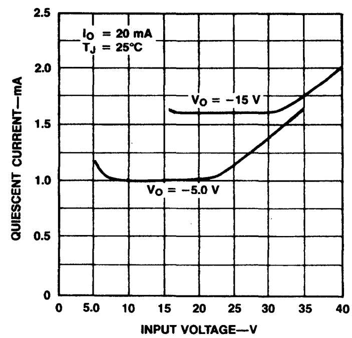
PC01721F

Dropout Voltage vs Junction Temperature



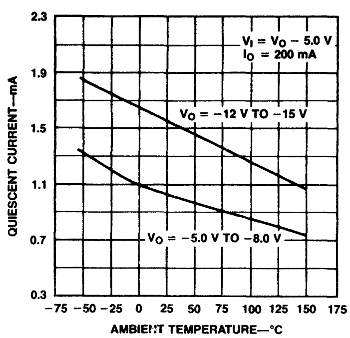
PC01691F

Quiescent Current vs Input Voltage



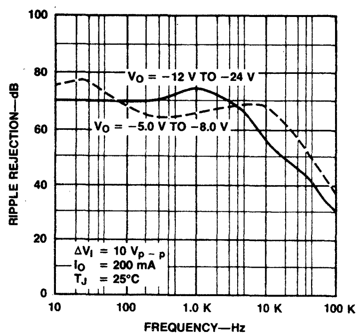
PC01771F

Quiescent Current vs Ambient Temperature



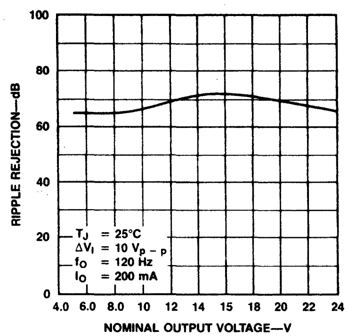
PC01781F

Ripple Rejection vs Frequency



PC01731F

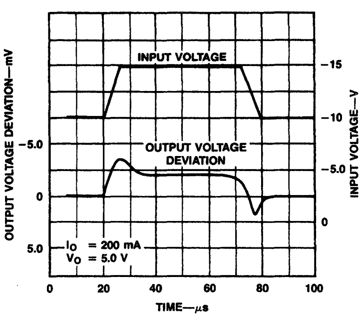
Ripple Rejection vs Output Voltages



PC01741F

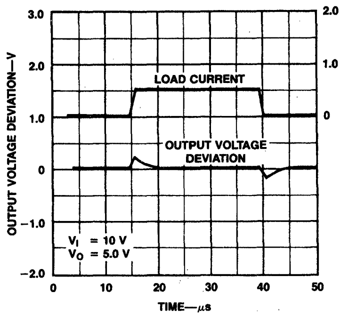
Typical Performance Curves (Cont.)

Line Transient Response



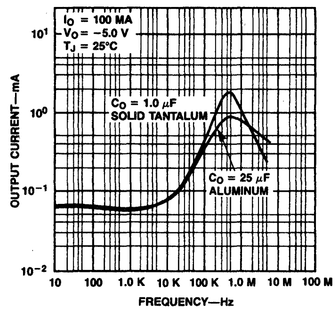
PC01761F

Load Transient Response



PC01751F

Output Impedance vs Frequency



PC01701F

Design Considerations

The μ79M00 fixed voltage regulator series have thermal-overload protection from excessive power, internal short-circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

The safe-area protection network may cause the device to latch-up if the output is shorted and the regulator is operating with high input voltages. This mode of operation will not damage the device. However, power (input voltage or the load) must be interrupted momentarily for the device to recover from the latched condition.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for μA79M00, 125°C for μA79M00C and μA7900MAC) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θ_{JC}	Max θ_{JC}	Typ θ_{JA}	Max θ_{JA}
TO-39	18.0	25	120	140
TO-220	3.0	5.0	60	40

$$P_{DMAX} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or} \qquad (1)$$

$$= \frac{T_{J\ Max} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving for T_J:

$$T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D\theta_{JA} \text{ (Without a heat sink)}$$

Where:

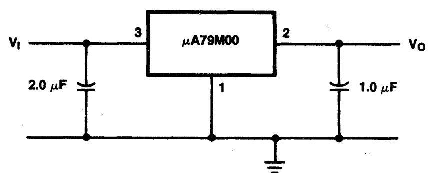
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JC} = Junction-to-case thermal resistance
- θ_{CA} = Case-to-ambient thermal resistance
- θ_{CS} = Case-to-heat sink thermal resistance
- θ_{SA} = Heat sink-to-ambient thermal resistance
- θ_{JA} = Junction-to-ambient thermal resistance

Typical Applications

Bypass capacitors are necessary for stable operation of the μA79M00 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.0 μF on the input, 1.0 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator Test Circuit



CR00341F

FAIRCHILD
A Schlumberger Company

μA7900 Series 3-Terminal Negative Voltage Regulators

Linear Division Voltage Regulators

Description

The μA7900 series of monolithic 3-terminal negative regulators is manufactured using the Fairchild Planar Epitaxial process. These negative regulators are intended as complements to the popular μA7800 series of positive voltage regulators, and they are available in voltage options from −5.0 V to −15 V. The μA7900 series employ internal current-limiting, thermal shutdown, and safe-area compensation, making them virtually indestructible.

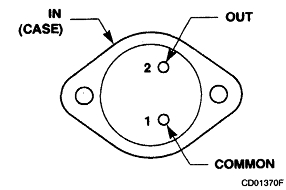
- **Output Current In Excess Of 1.0 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Available In JEDEC TO-220 And TO-3 Packages**
- **Output Voltages of −5 V, −8 V, −12 V, and −15 V**

Absolute Maximum Ratings

Storage Temperature Range	
TO-3 Metal Can	−65°C to +175°C
TO-220 Package	−65°C to +150°C
Operating Junction Temperature Range	
Extended (μA7900M)	−55°C to +150°C
Commercial (μA7900C)	0°C to +150°C
Lead Temperature	
TO-3 Metal (soldering, 60 s)	300°C
TO-220 Package (soldering, 10 s)	265°C
Power Dissipation	Internally Limited
Input Voltage	
−5 V to −15 V	−35 V

Note
1. The convention for Negative Regulators is the Algebraic value, thus −15 is less then −10 V.

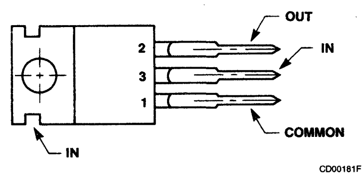
Connection Diagram TO-3 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA7905KM	HJ	Metal
μA7908KM	HJ	Metal
μA7912KM	HJ	Metal
μA7915KM	HJ	Metal
μA7905KC	HJ	Metal
μA7908KC	HJ	Metal
μA7912KC	HJ	Metal
μA7915KC	HJ	Metal

Connection Diagram TO-220 Package (Top View)

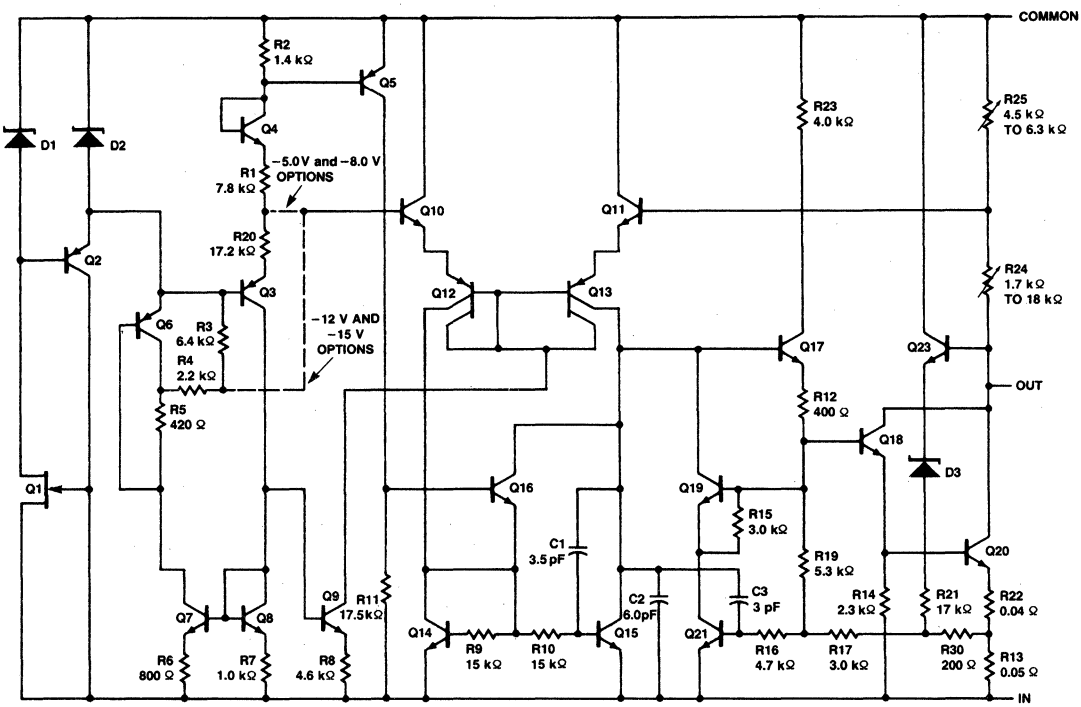


Lead 3 connected to case.

Order Information

Device Code	Package Code	Package Description
μA7905UC	GH	Molded Power Pack
μA7908UC	GH	Molded Power Pack
μA7912UC	GH	Molded Power Pack
μA7915UC	GH	Molded Power Pack

Equivalent Circuit



EQ00641F

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μA7905
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -10$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-4.8	-5.0	-5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-7.0\ V \leq V_I \leq -25\ V$		3.0	50	mV
				$-2.0\ V \leq V_I \leq -12\ V$		1.0	25	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		15	100	mV
				$250\ mA \leq I_O \leq 750\ mA$		5.0	25	
V_O	Output Voltage		$-8.0\ V \leq V_I \leq -20\ V$ $5.0\ mA \leq I_O \leq 1.0\ A$ $p \leq 15\ W$		-4.70		-5.30	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-8.0\ V \leq V_I \leq -25\ V$				1.3	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			1.1	2.3	V
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $-55°C \leq T_A \leq 125°C$				0.3	$mV/°C/V_O$
I_{OS}	Output Short Circuit Current		$V_I = -35$ V, $T_J = 25°C$				1.2	A

μA7905C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -10$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-4.8	-5.0	-5.2	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-7.0\ V \leq V_I \leq -25\ V$		3.0	100	mV
				$-8.0\ V \leq V_I \leq -12\ V$		1.0	50	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		15	100	mV
				$250\ mA \leq I_O \leq 750\ mA$		5.0	50	
V_O	Output Voltage		$-7.0\ V \leq V_I \leq -20\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $p \leq 15\ W$		-4.75		-5.25	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-7.0\ V \leq V_I \leq -25\ V$				1.3	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			125		μV

μA7905C (Cont.)
Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$, $V_I = -10$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $I_O = 350$ mA, $T_J = 25°C$	54	60		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$		1.1		V
I_{pk}	Peak Output Current	$T_J = 25°C$		2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $0°C \leqslant T_A \leqslant 125°C$		0.4		mV/°C

μA7908
Electrical Characteristics $-55°C \leqslant T_A \leqslant 125°C$, $V_I = -14$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-7.7	-8.0	-8.3	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-10.5\ V \leqslant V_I \leqslant -25$ V		6.0	80	mV
				$-11\ V \leqslant V_I \leqslant -17$ V		2.0	40	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leqslant I_O \leqslant 1.5$ A		12	100	mV
				$250\ mA \leqslant I_O \leqslant 750$ mA		4.0	40	
V_O	Output Voltage		$-11.5\ V \leqslant V_I \leqslant -23$ V, $5.0\ mA \leqslant I_O \leqslant 1.0$ A, $p \leqslant 15$ W		-7.6		-8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-11.5\ V \leqslant V_I \leqslant -25$ V				1.0	mA
		with load	$5.0\ mA \leqslant I_O \leqslant 1.0$ A				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leqslant f \leqslant 100$ kHz			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		f = 2400 Hz, $V_I = -13$ V, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			1.1	2.3	V
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $-55°C \leqslant T_A \leqslant 125°C$				0.3	$mV/°C/V_O$
I_{OS}	Output Short Circuit Current		$V_I = -35$ V, $T_J = 25°C$				1.2	A

μA7908C
Electrical Characteristics $0°C \leqslant T_A \leqslant 125°C$, $V_I = -14$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$	-7.7	-8.0	-8.3	V

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μA7908C (Cont.)
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -14$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-10.5\ V \leq V_I \leq -25\ V$		6.0	160	mV
				$-11\ V \leq V_I \leq -17\ V$		2.0	80	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	160	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	80	
V_O	Output Voltage		$-10.5\ V \leq V_I \leq -23\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $p \leq 15\ W$		-7.6		-8.4	V
I_Q	Quiescent Current		$T_J = 25°C$			1.0	2.0	mA
ΔI_Q	Quiescent Current Change	with line	$-10.5\ V \leq V_I \leq -25\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			200		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -13$ V, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			1.1		V
I_{pk}	Peak Output Current		$T_J = 25°C$			2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$			0.6		mV/°C

μA7912
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		-11.5	-12.0	-12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-14.5\ V \leq V_I \leq -30\ V$		10	120	mV
				$-16\ V \leq V_I \leq -22\ V$		3.0	60	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ mA$		12	120	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	60	
V_O	Output Voltage		$-15.5\ V \leq V_I \leq -27\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $p \leq 15\ W$		-11.4		-12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-15\ V \leq V_I \leq -30\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	$\mu V/V_O$
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -17$ V, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB

μA7912 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$		1.1	2.3	V
I_{pk}	Peak Output Current	$T_J = 25°C$	1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $-55°C \leq T_A \leq 150°C$			0.3	mV/°C/V_O
I_{OS}	Output Short Circuit Current	$V_I = -35$ V, $T_J = 25°C$			1.2	A

μA7912C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -19$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		−11.5	−12.0	−12.5	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-14.5\ V \leq V_I \leq -30$ V		10	240	mV
				$-16\ V \leq V_I \leq -22$ V		3.0	120	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5$ A		12	240	mV
				$250\ mA \leq I_O \leq 750$ mA		4.0	120	
V_O	Output Voltage		$-14.5\ V \leq V_I \leq -27$ V, $5.0\ mA \leq I_O \leq 1.0$ A, $p \leq 15$ W		−11.4		−12.6	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-14.5\ V \leq V_I \leq -30$ V				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0$ A				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100$ kHz			300		μV
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -17$ V, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			1.1		V
I_{pk}	Peak Output Current		$T_J = 25°C$			2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$			0.8		mV/°C

Notes
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

μA7915
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -23$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_O	Output Voltage	$T_J = 25°C$	−14.4	−15.0	−15.6	V

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μA7915 (Cont.)
Electrical Characteristics $-55°C \leq T_A \leq 125°C$, $V_I = -23$ V, $I_O = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-17.5\ V \leq V_I \leq -30\ V$		11	150	mV
				$-20\ V \leq V_I \leq -26\ V$		3.0	75	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	150	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	75	
V_O	Output Voltage		$-18.5\ V \leq V_I \leq -30\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $p \leq 15\ W$		−14.25		−15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-18.5\ V \leq V_I \leq -30\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			25	80	μV/V_O
$\Delta V_I/\Delta V_O$	Ripple Rejection		$f = 2400$ Hz, $V_I = -20$ V, $I_O = 350$ mA, $T_J = 25°C$		54	60		dB
V_{DO}	Dropout Voltage		$I_O = 1.0$ A, $T_J = 25°C$			1.1	2.3	V
I_{pk}	Peak Output Current		$T_J = 25°C$		1.3	2.1	3.3	A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage		$I_O = 5.0$ mA, $-55°C \leq T_A \leq 125°C$				0.3	mV/°C/V_O
I_{OS}	Output Short Circuit Current		$V_I = -35$ V, $T_J = 25°C$				1.2	A

μA7915C
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -23$ V, $I_O = 500$ mA, $C_I = 2$ μF, $C_O = 1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition[1]		Min	Typ	Max	Unit
V_O	Output Voltage		$T_J = 25°C$		−14.4	−15.0	−15.6	V
$V_{R\ LINE}$	Line Regulation		$T_J = 25°C$	$-17.5\ V \leq V_I \leq -30\ V$		11	300	mV
				$-20\ V \leq V_I \leq -26\ V$		3.0	150	
$V_{R\ LOAD}$	Load Regulation		$T_J = 25°C$	$5.0\ mA \leq I_O \leq 1.5\ A$		12	300	mV
				$250\ mA \leq I_O \leq 750\ mA$		4.0	150	
V_O	Output Voltage		$-17.5\ V \leq V_I \leq -30\ V$, $5.0\ mA \leq I_O \leq 1.0\ A$, $p \leq 15\ W$		−14.25		−15.75	V
I_Q	Quiescent Current		$T_J = 25°C$			1.5	3.0	mA
ΔI_Q	Quiescent Current Change	with line	$-17.5\ V \leq V_I \leq -30\ V$				1.0	mA
		with load	$5.0\ mA \leq I_O \leq 1.0\ A$				0.5	
N_O	Noise		$T_A = 25°C$, $10\ Hz \leq f \leq 100\ kHz$			375		μV

μA7915C (Cont.)
Electrical Characteristics $0°C \leq T_A \leq 125°C$, $V_I = -23$ V, $I_O = 500$ mA, $C_I = 2$ μF, $C_O = 1$ μF, unless otherwise specified.

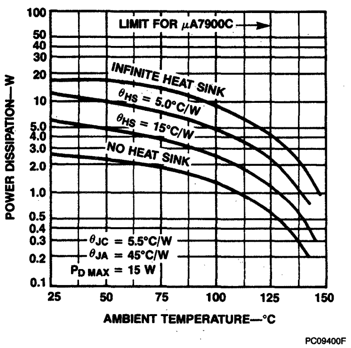
Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 2400 Hz, $V_I = -20$ V, $I_O = 350$ mA, $T_J = 25°C$	54	60		dB
V_{DO}	Dropout Voltage	$I_O = 1.0$ A, $T_J = 25°C$		1.1		V
I_{pk}	Peak Output Current	$T_J = 25°C$		2.1		A
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_O = 5.0$ mA, $0°C \leq T_A \leq 125°C$		1.0		mV/°C

Notes

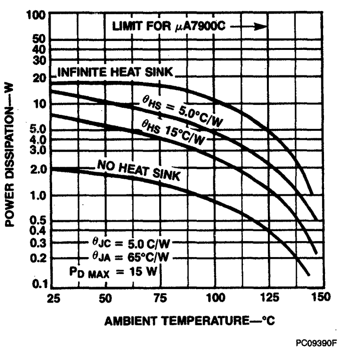
1. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Curves

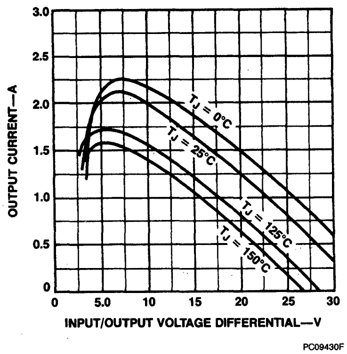
Worst Case Power Dissipation vs Ambient Temperature (TO-3)



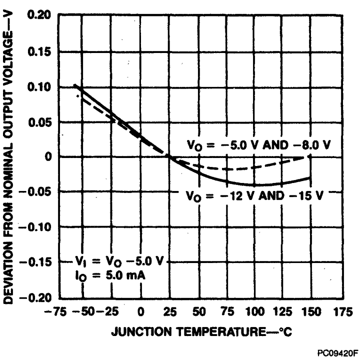
Worst Case Power Dissipation vs Ambient Temperature (TO-220)



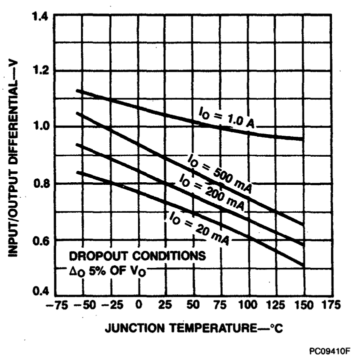
Peak Output Current vs Input/Output Voltage Differential



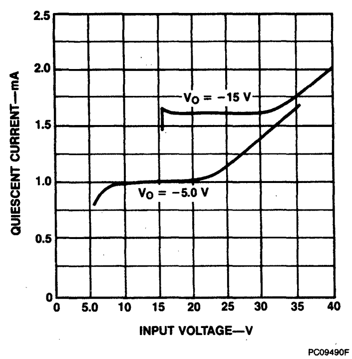
Output Voltage vs Junction Temperature



Dropout Voltage vs Junction Temperature



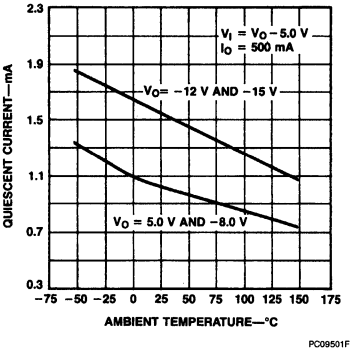
Quiescent Current vs Input Voltage



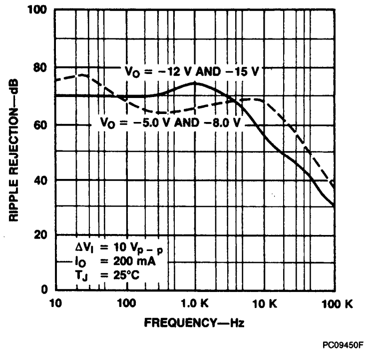
6

Typical Performance Curves (Cont.)

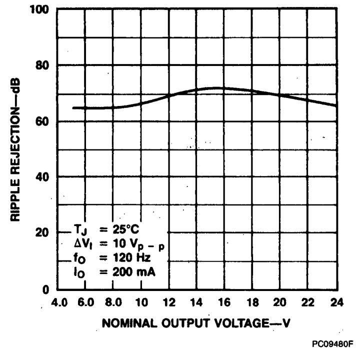
Quiescent Current vs Temperature



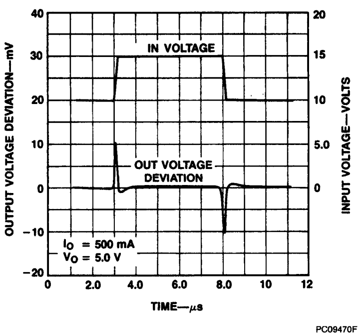
Ripple Rejection vs Frequency



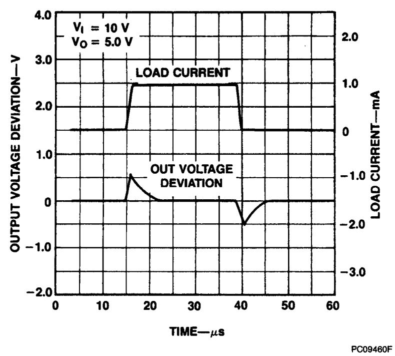
Ripple Rejection vs Output Voltages



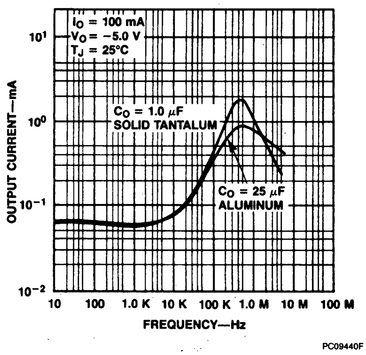
Line Transient Response



Load Transient Response



Output Impedance vs Frequency



Design Considerations

The µA7900 fixed voltage regulator series has thermal overload protection from excessive power dissipation, internal short circuit protection which limits the circuit's maximum current, and output transistor safe-area compensation for reducing the output current as the voltage across the pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (150°C for µA7900, 125°C for µA7900C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Package	Typ θJC °C/W	Max θJC °C/W	Typ θJA °C/W	Max θJA °C/W
TO-3	3.5	5.5	40	35
TO-220	3.0	5.0	60	40

$$P_{D\ Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or } \frac{T_{J\ Max} T_A}{\theta_{JA}}$$

$\theta_{CA} = \theta_{CS} + \theta_{SA}$ (Without heat sink)

Solving for T_J:

$T_J = T_A + P_D\ (\theta_{JC} + \theta_{CA})$ or

$= T_A + P_D \theta_{JA}$ (Without heat sink)

Where:

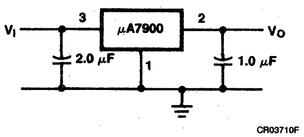
- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction-to-Ambient Thermal Resistance
- θ_{JC} = Junction-to-Case Thermal Resistance
- θ_{CA} = Case-to-Ambient Thermal Resistance
- θ_{CS} = Case-to-Heat Sink Thermal Resistance
- θ_{SA} = Heat Sink-to-Ambient Thermal Resistance

Typical Applications

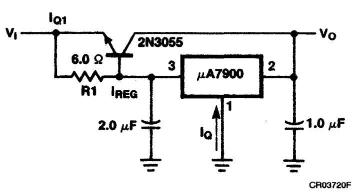
Bypass capacitors are necessary for stable operation of the μA7900 series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors, (2.0 μF on the input, 1.0 μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10 μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

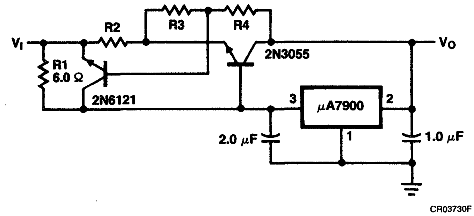
Fixed Output Regulator



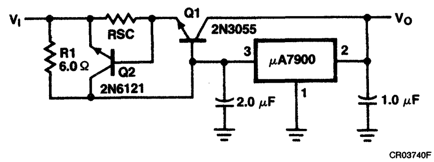
High Current Voltage Regulator



Output Current HIGH, Foldback Current-Limited

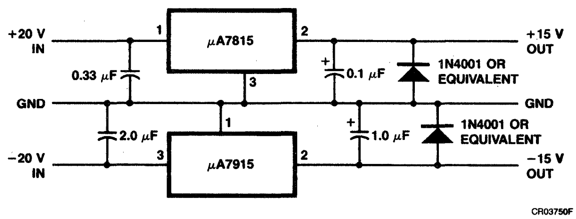


Output Current HIGH, Short Circuit Protected



$$RSC = \frac{V_{BE(Q2)}}{I_{OS}}$$

Operational Amplifier Supply (± 15 V at 1.0 A)



FAIRCHILD

A Schlumberger Company

μA101A • μA201A • μA301A General Purpose Operational Amplifiers

Linear Division Operational Amplifiers

Description

The μA101A, μA201A, and μA301A are general purpose monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers, and sample-and-hold circuits is improved due to the low drift and low bias currents of the μA101A, μA201A, or μA301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of latch up coupled with internal short circuit protection make the μA101A, μA201A and μA301A virtually foolproof.

- **Low Offset Current And Voltage**
- **Low Offset Current Drift**
- **Low Bias Current**
- **Short Circuit Protected**
- **Low Power Consumption**

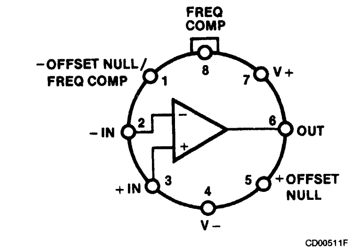
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (μA101AM)	-55°C to +125°C
Industrial (μA201AV)	-25°C to +85°C
Commercial (μA301AC)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	
μA101A, μA201A	±22 V
μA301A	±18 V
Differential Input Voltage	±30 V
Input Voltage[3]	±15 V
Output Short Circuit Duration[4]	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C and the SO-8 at 6.5 mW/°C.
3. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be ground or either supply. μA101A and μA201A ratings apply to +125°C case temperature or +75°C ambient temperature. μA301A ratings apply for case temperatures to 70°C.

Connection Diagram 8-Lead Metal Package (Top View)

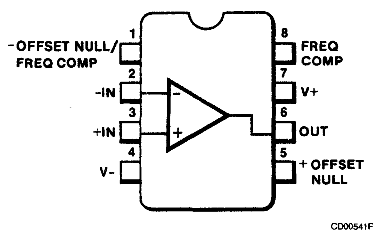


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA101AHM	5W	Metal
μA201AHV	5W	Metal
μA301AHC	5W	Metal

Connection Diagram 8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA301ASC	KC	Molded Surface Mount
μA301ATC	9T	Molded DIP

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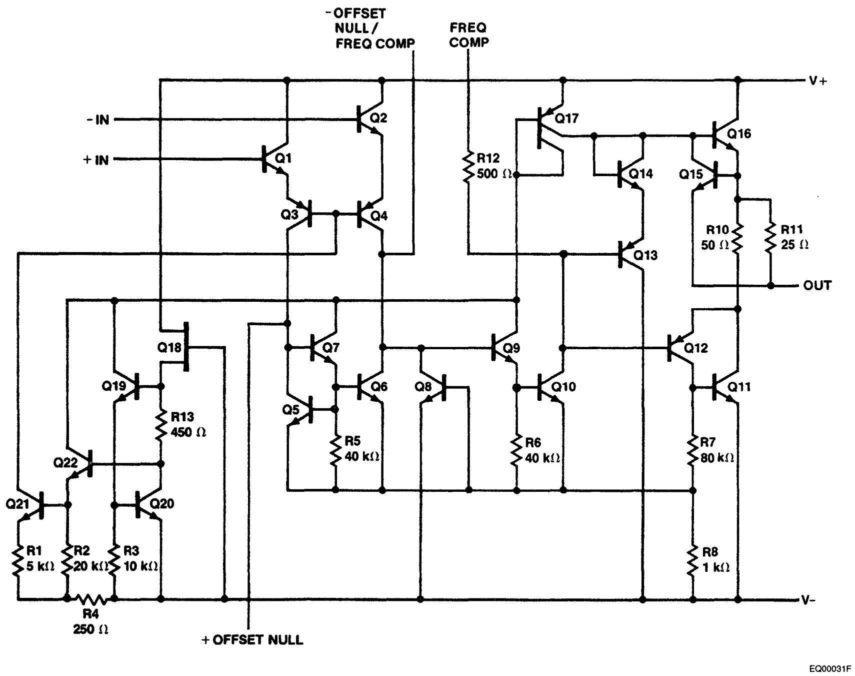
Equivalent Circuit

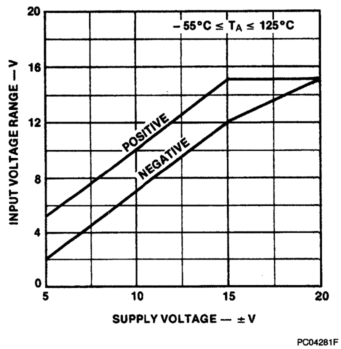


μA101A, μA201A and μA301A
Electrical Characteristics $T_A = 25°C$, $\pm 5.0\ V \leq V_{CC} \leq \pm 20\ V$ for the μA101A and μA201A, $\pm 5.0\ V \leq V_{CC} \leq \pm 15\ V$ for the μA301A, unless otherwise specified.

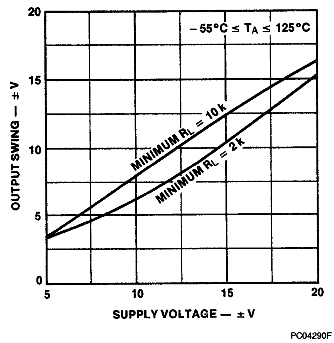
Symbol	Characteristic	Condition	μA101A, μA201A			μA301A			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
I_{IO}	Input Offset Current			1.5	10		3.0	50	nA
I_{IB}	Input Bias Current			30	75		70	250	nA
Z_I	Input Impedance		1.5	4.0		0.5	2.0		MΩ
I_{CC}	Supply Current	$V_{CC} = \pm 20\ V$		1.8	3.0				mA
		$V_{CC} = \pm 15\ V$					1.8	3.0	
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geq 2.0\ k\Omega$	50	160		25	160		V/mV
The following specifications apply over the range of $-55°C \leq T_A \leq +125°C$ for the μA101A, and $-25°C \leq T_A \leq +85°C$ for the μA201A, and $0°C \leq T_A \leq +70°C$ for the μA301A.									
V_{IO}	Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$T_{A\ Min} \leq T_A \leq T_{A\ Max}$		6.0	15		6.0	30	μV/°C
I_{IO}	Input Offset Current				20			70	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leq T_A \leq T_{A\ Max}$		0.01	0.1		0.01	0.3	nA/°C
		$T_{A\ Min} \leq T_A \leq 25°C$		0.02	0.2		0.02	0.6	
I_{IB}	Input Bias Current				100			300	nA
I_{CC}	Supply Current	$T_A = T_{A\ Max}$, $V_{CC} = \pm 20\ V$		1.2	2.5				mA
CMR	Common Mode Rejection	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
V_{IR}	Input Voltage Range	$V_{CC} = \pm 20\ V$	±15						V
		$V_{CC} = \pm 15\ V$				±12			
PSRR	Power Supply Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geq 2.0\ k\Omega$	25			15			V/mV
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$V_{CC} = \pm 15\ V$, $R_L = 2.0\ k\Omega$	±10	±13		±10	±13		

Typical Performance Curves

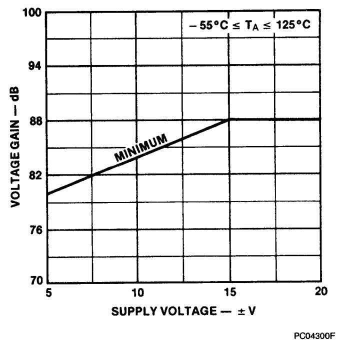
Input Voltage Range vs Supply Voltage (μA101A and 201A)



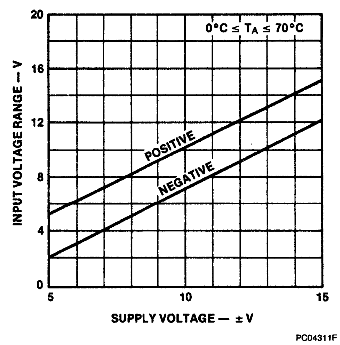
Output Swing vs Supply Voltage (μA101A and 201A)



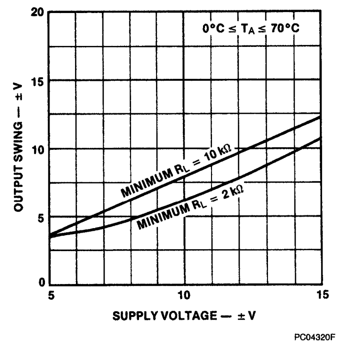
Voltage Gain vs Supply Voltage (μA101A and 201A)



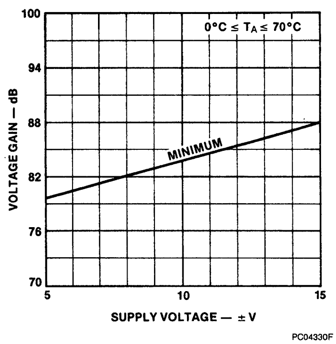
Input Voltage Range vs Supply Voltage (μA301A)



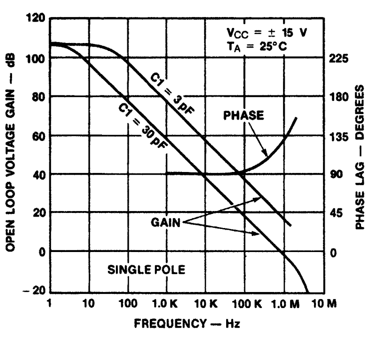
Output Swing vs Supply Voltage (μA301A)



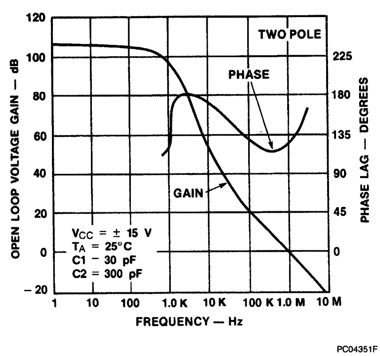
Voltage Gain vs Supply Voltage (μA301A)



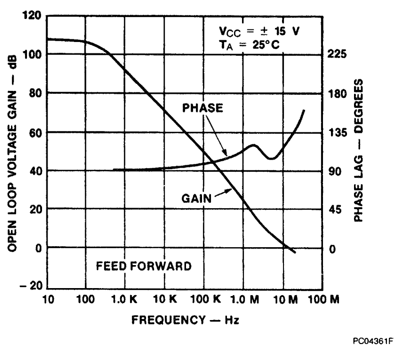
Open Loop Frequency Response (μA101A, 201A, and 301A)



Open Loop Frequency Response (μA101A, 201A, and 301A)

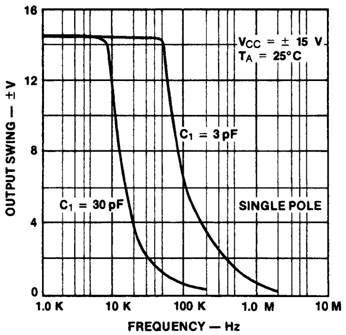


Open Loop Frequency Response (μA101A, 201A, and 301A)



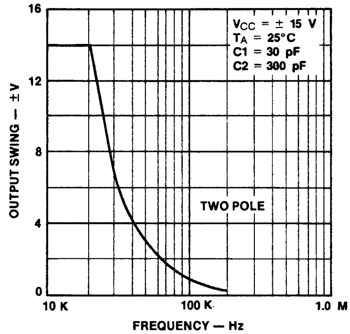
Typical Performance Curves for μA101A, μA201A, and μA301A (Cont.)

Large Signal Frequency Response



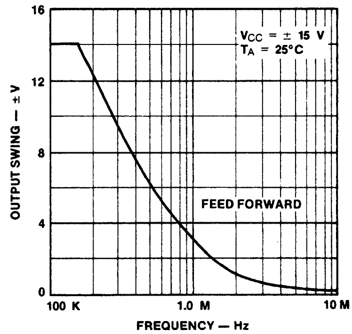
PC04371F

Large Signal Frequency Response



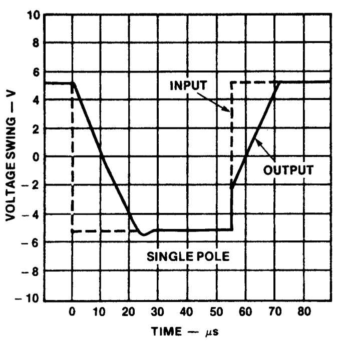
PC04381F

Large Signal Frequency Response



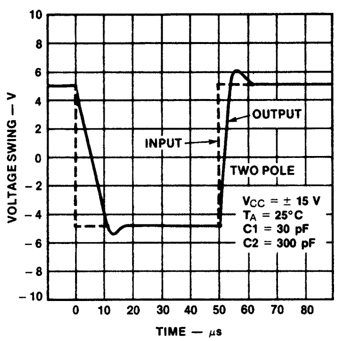
PC04391F

Voltage Follower Pulse Response



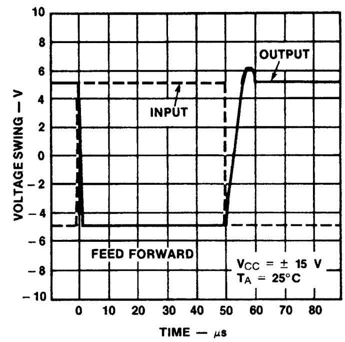
PC04400F

Voltage Follower Pulse Response



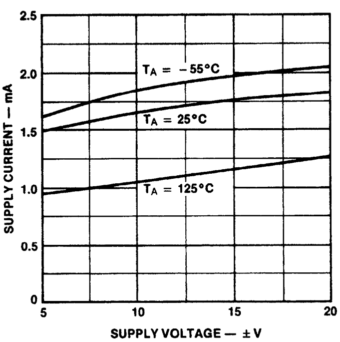
PC04410F

Voltage Follower Pulse Response



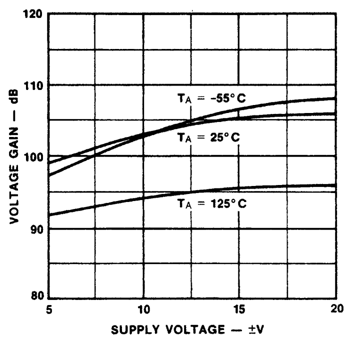
PC04421F

Supply Voltage Current vs Supply Voltage



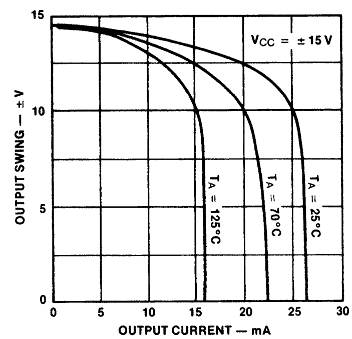
PC04431F

Voltage Gain vs Supply Voltage



PC04441F

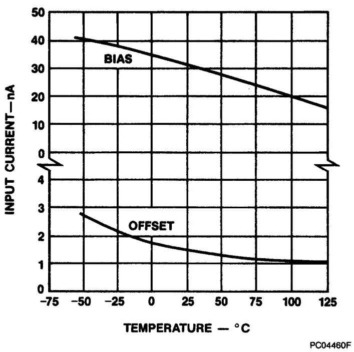
Current Limiting



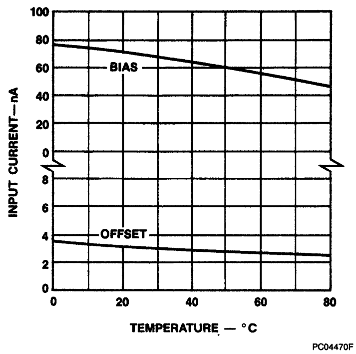
PC04450F

Typical Performance Curves for μA101A, μA201A, and μA301A (Cont.)

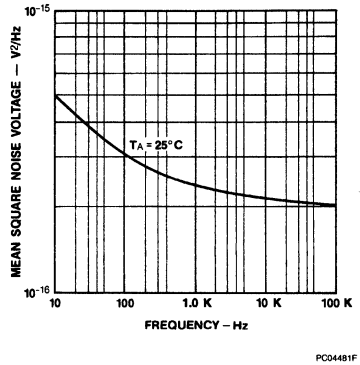
Input Current vs Temperature (μA101A and μA201A)



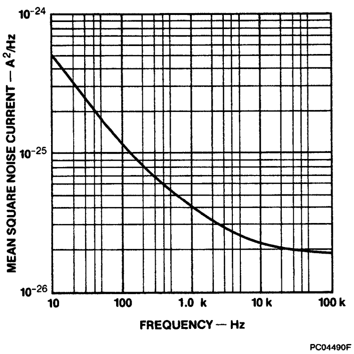
Input Current vs Temperature (μA301A only)



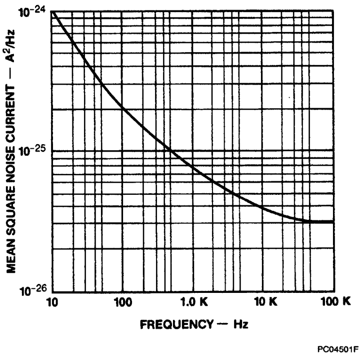
Input Noise Voltage vs Frequency



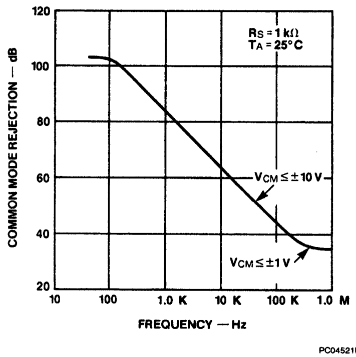
Input Noise Current vs Frequency (μA101A and μA201A)



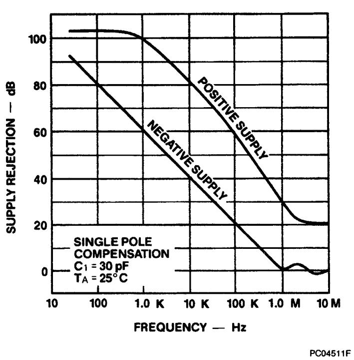
Input Noise Current vs Frequency (μA301A)



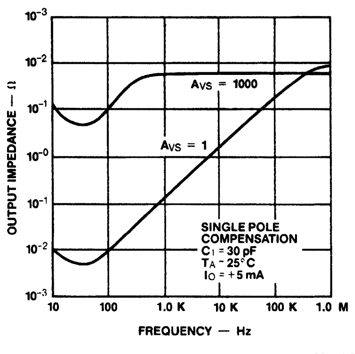
Common Mode Rejection vs Frequency



Supply Rejection vs Frequency

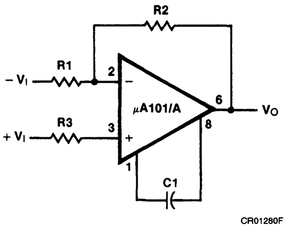


Closed Loop Output Impedance vs Frequency



Compensation Circuits (Note 2)

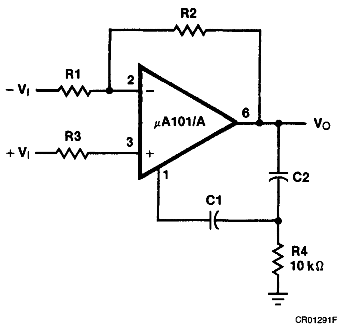
Single Pole Compensation



$$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$$

$C_s = 30$ pF

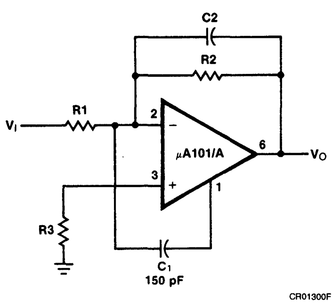
Two Pole Compensation



$$C_1 \geq \frac{R_1 C_s}{R_1 + R_2}$$

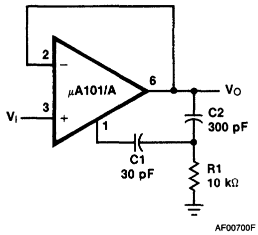
$C_s = 30$ pF
$C_2 = 10\ C_1$

Feed Forward Compensation



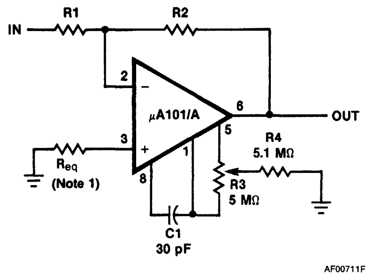
Typical Applications (Note 2)

Fast Voltage Follower

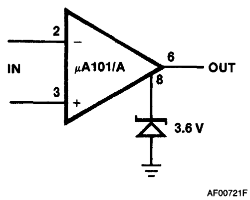


Power Bandwidth: 15 kHz
Slew Rate: 1 V/μs

Inverting Amplifier With Balancing Circuit



Voltage Comparator For Driving Or DTL Integrated Circuits

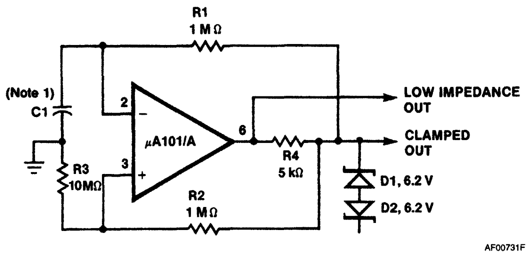


Notes

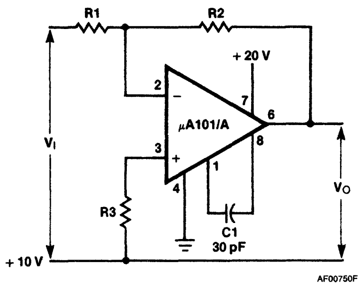
1. May be zero or equal to parallel combination of R1 and R2 for minimum offset.
2. All lead numbers shown refer to 8-lead metal package.

Typical Applications (Cont.) (Note 2)

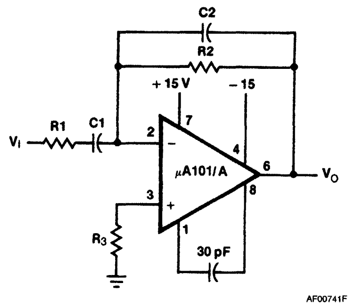
Low Frequency Square Wave Generator



Circuit For Operating Without A Negative Supply



Practical Differentiator



$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$$f_c < f_h < f_{unity\ gain}$$

Notes

1. Adjust C_1 for frequency
2. All lead numbers shown refer to 8-lead metal package

FAIRCHILD

A Schlumberger Company

μA101 • μA201 General Purpose Operational Amplifiers

Linear Division Operational Amplifiers

Description

The μA101 and μA201 are general purpose monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. The μA101 and μA201 compensate easily with a single external component. High common mode voltage range and absence of latch up make the μA101 and μA201 ideal for use as voltage followers. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA101 and μA201 are short circuit protected and have the same lead configuration as the popular μA741, μA748 and μA709.

- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

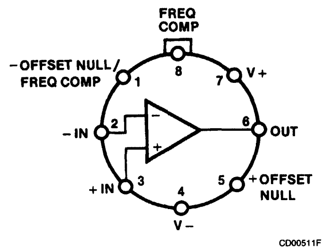
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range[1]	
Extended (μA101M)	-55°C to +125°C
Commercial (μA201C)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[2, 3]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[4]	±15 V

Notes

1. Short circuit may be to ground or either supply. The μA101 ratings apply to +125°C case temperature or +75°C ambient temperature. The μA201 ratings apply to case temperatures up to +70°C.
2. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can.
3. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
4. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 8-Lead Metal Package (Top View)

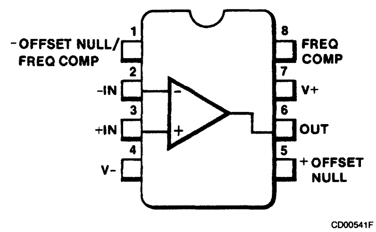


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA101HM	5W	Metal
μA201HC	5W	Metal

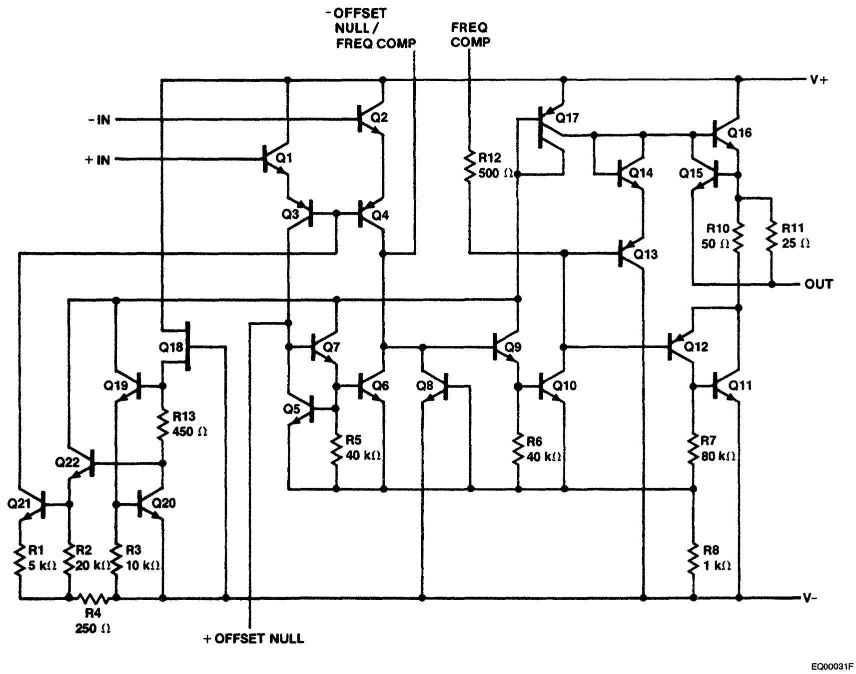
Connection Diagram 8-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA201TC	9T	Molded DIP

Equivalent Circuit



µA101 and µA201
Electrical Characteristics $T_A = 25°C$, $\pm 5.0\ V \leq V_{CC} \leq \pm 20\ V$ for µA101, and $\pm 5.0\ V \leq V_{CC} \leq \pm 15\ V$ for µA201, unless otherwise specified.

Symbol	Characteristic	Condition	µA101 Min	µA101 Typ	µA101 Max	µA201 Min	µA201 Typ	µA201 Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.0	5.0		2.0	7.5	mV
I_{IO}	Input Offset Current			40	200		100	500	nA
I_{IB}	Input Bias Current			120	500		250	1500	nA
Z_I	Input Impedance		300	800		100	400		kΩ
I_{CC}	Supply Current	$V_{CC} = \pm 20\ V$		1.8	3.0				mA
		$V_{CC} = \pm 15\ V$					1.8	3.0	
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geq 2.0\ k\Omega$	50	160		20	150		V/mV
The following specifications apply over the range of $-55°C \leq T_A \leq +125°C$ for µA101, and $0°C \leq T_A \leq +70°C$ for µA201.									
V_{IO}	Input Offset Voltage	$R_S \leq 50\ k\Omega$			6.0			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S \leq 50\ \Omega$		3.0			6.0		µV/°C
		$R_S \leq 50\ k\Omega$		6.0			10.0		
I_{IO}	Input Offset Current	$T_A = T_{A\ Min}$		10	200		50	400	nA
		$T_A = T_{A\ Max}$		100	500		150	750	
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leq T_A \leq T_{A\ Max}$		0.01	0.1		0.01	0.3	nA/°C
		$T_{A\ Min} \leq T_A \leq 25°C$		0.02	0.2		0.02	0.6	
I_{IB}	Input Bias Current			0.28	1.5		0.32	2.0	µA
I_{CC}	Supply Current	$T_A = 125°C$, $V_{CC} = \pm 20\ V$		1.2	2.5				mA
CMR	Common Mode Rejection	$R_S \leq 50\ k\Omega$	70	90		65	90		dB
V_{IR}	Input Voltage Range	$V_{CC} = \pm 15\ V$	±12			±12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 50\ k\Omega$	70	90		70	90		dB
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geq 2.0\ k\Omega$	25			15			V/mV
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$V_{CC} = \pm 15\ V$, $R_L = 2.0\ k\Omega$	±10	±13		±10	±13		

FAIRCHILD
A Schlumberger Company

μA108/A • μA208/A • μA308/A Super Beta Operational Amplifiers

Description

The μA108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar Epitaxial process. High input impedance, low noise, low input offsets, and low temperature drifts are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA108 series is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feed forward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **Guaranteed Low Input Offset Characteristics**
- **High Input Impedance**
- **Low Offset Current**
- **Low Bias Current**
- **Operation Over Wide Supply Range**

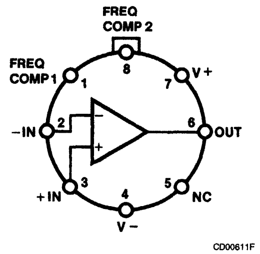
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (μA108AM, μA108M)	-55°C to +125°C
Industrial (μA208AV, μA108V)	-25°C to +85°C
Commercial (μA308AC, μA308C)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	
μA108/A, μA208/A	±20 V
μA308/A	±18 V
Differential Input Current [3]	±10 mA
Input Voltage[4]	±15 V
Output Short Circuit Duration[5]	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless adequate limiting resistance is used.
4. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
5. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.

Connection Diagram
8-Lead Metal Package
(Top View)

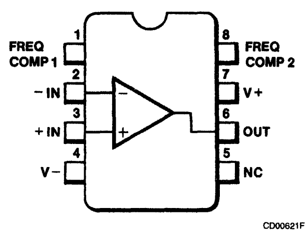


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA108HM	5W	Metal
μA108AHM	5W	Metal
μA208HV	5W	Metal
μA208AHV	5W	Metal
μA308HC	5W	Metal
μA308AHC	5W	Metal

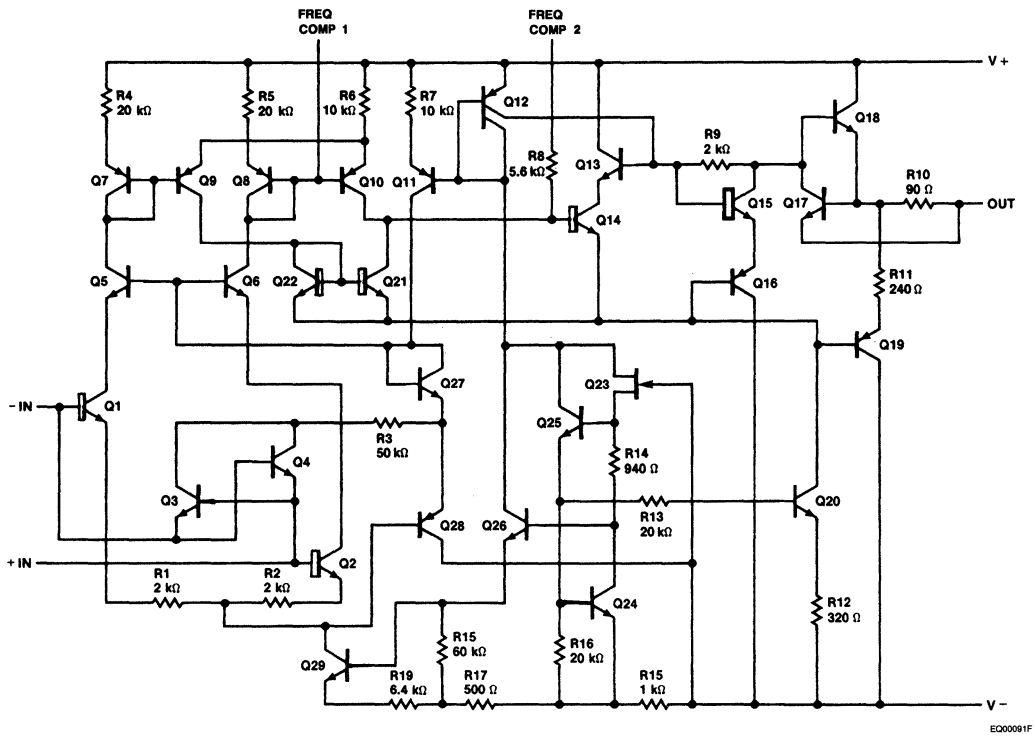
Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA308SC	KC	Molded Surface Mount
μA308TC	9T	Molded DIP
μA308ASC	KC	Molded Surface Mount
μA308ATC	9T	Molded DIP

Equivalent Circuit



7

μA108/A and μA208/A
Electrical Characteristics $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, $T_A = 25°C$, unless otherwise specified.

Symbol	Characteristic	Condition	μA108A μA208A Min	Typ	Max	μA108 μA208 Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage			0.3	0.5		0.7	2.0	mV
I_{IO}	Input Offset Current			0.05	0.2		0.05	0.2	nA
I_{IB}	Input Bias Current			0.8	2.0		0.8	2.0	nA
Z_I	Input Impedance		30	70		30	70		MΩ
I_{CC}	Supply Current	$V_{CC} = \pm 20\ V$		.03	0.6		0.3	0.6	mA
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geqslant 10\ \Omega$	80	300		50	300		V/mV
The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$ for the μA108/A, and $-25°C \leqslant T_A \leqslant +85°C$ for the μA208/A, unless otherwise specified.									
V_{IO}	Input Offset Voltage				1.0			3.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			1.0	5.0		3.0	15	μV/°C
I_{IO}	Input Offset Current				0.4			0.4	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			0.5	2.5		0.5	2.5	pA/°C
I_{IB}	Input Bias Current			0.8	3.0			3.0	nA
I_{CC}	Supply Current	$V_{CC} = \pm 20\ V$, $T_A = 125°C$		0.15	0.4		0.15	0.4	mA
CMR	Common Mode Rejection		96	110		85	100		dB
V_{IR}	Input Voltage Range	$V_{CC} = \pm 15\ V$	±13.5			±13.5			V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 5.0\ V$ to $\pm 20\ V$	96	110		80	96		dB
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geqslant 10\ \Omega$	40			25			V/mV
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V

μA308/A
Electrical Characteristics $T_A = 25°C$, $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$, unless otherwise specified.

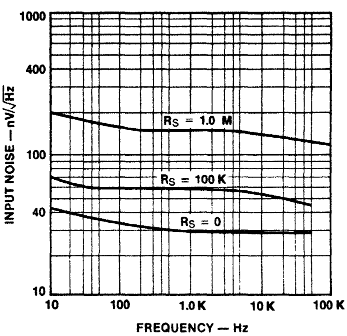
Symbol	Characteristic	Condition	μA308A Min	Typ	Max	μA308 Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage			0.3	0.5		2.0	7.5	mV
I_{IO}	Input Offset Current			0.2	1.0		0.2	1.0	nA
I_{IB}	Input Bias Current			1.5	7.0		1.5	7.0	nA
Z_I	Input Impedance		10	40		10	40		MΩ

μA308/A (Cont.)
Electrical Characteristics $T_A = 25°C$, $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$, unless otherwise specified.

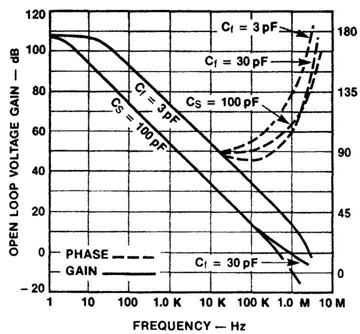
Symbol	Characteristic	Condition	μA308A Min	μA308A Typ	μA308A Max	μA308 Min	μA308 Typ	μA308 Max	Unit
I_{CC}	Supply Current	$V_{CC} = \pm 15\ V$		0.3	0.8		0.3	0.8	mA
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geqslant 10\ \Omega$	80	300		25	300		V/mV
The following specifications apply over the range of $0°C \leqslant T_A \leqslant +70°C$									
V_{IO}	Input Offset Voltage				0.73			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			1.0	5.0		6.0	30	μV/°C
I_{IO}	Input Offset Current				1.5			1.5	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			2.0	10		2.0	10	pA/°C
I_{IB}	Input Bias Current				10			10	nA
CMR	Common Mode Rejection		96	110		80	100		dB
V_{IR}	Input Voltage Range	$V_{CC} = \pm 15\ V$	±13.5			±13.5			V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 5.0\ V$ to $\pm 18\ V$	96	110		80	96		dB
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \geqslant 10\ k\Omega$	60			15			V/mV
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Typical Performance Curves for μA108 Series

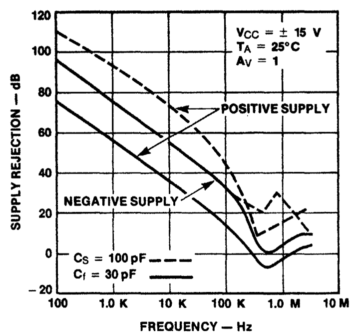
Input Noise Voltage vs Frequency



Open Loop Frequency Response

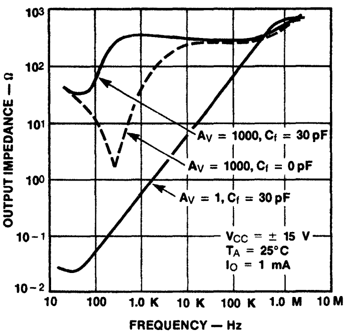


Supply Rejection vs Frequency

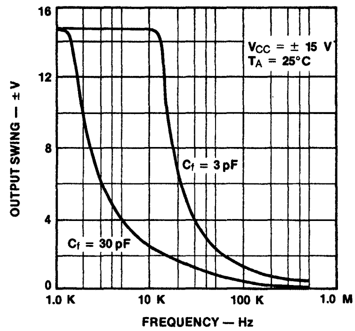


Typical Performance Curves for μA108 Series (Cont.)

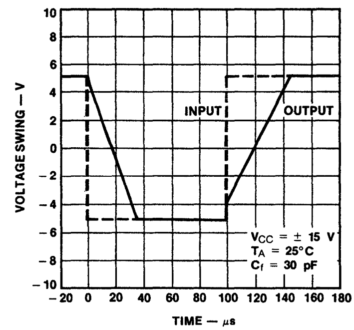
Closed Loop Output Impedance vs Frequency



Large Signal Frequency Response

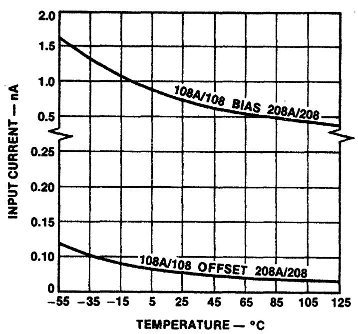


Voltage Follower Pulse Response

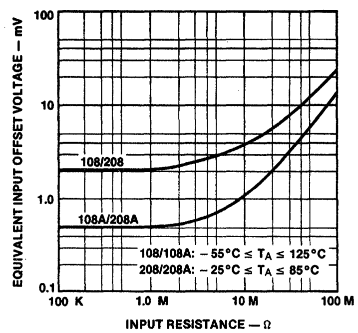


Typical Performance Curves for μA108/A, and μA208/A (Unless otherwise specified)

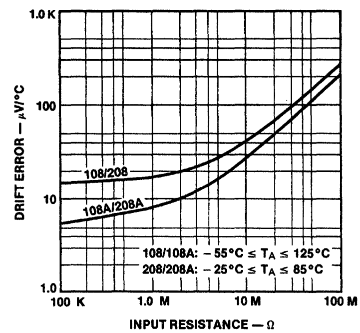
Input Currents vs Temperature



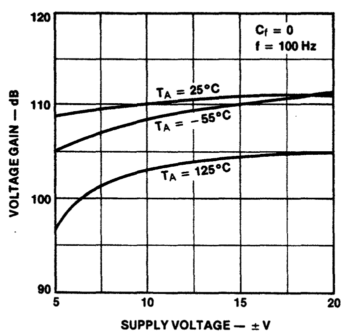
Maximum Offset Error



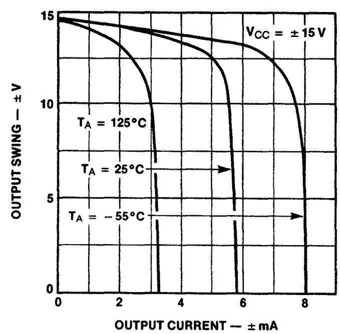
Maximum Drift Error



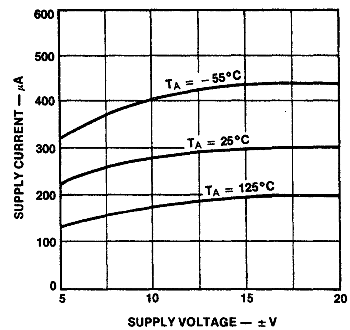
Voltage Gain vs Supply Voltage (μA108)



Output Swing vs Output Current (μA108)

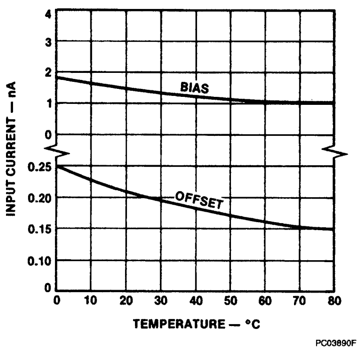


Supply Current vs Supply Voltage (μA108)

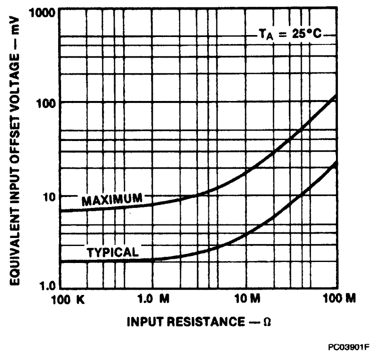


Typical Performance Curves for μA308/A (Unless otherwise specified)

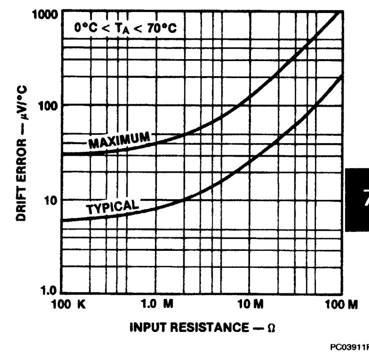
Input Current vs Temperature



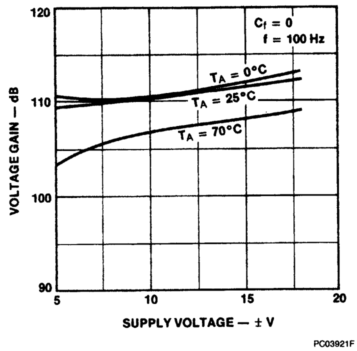
Maximum Offset Error (μA308)



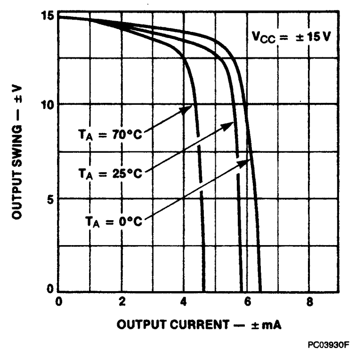
Maximum Drift Error (μA308)



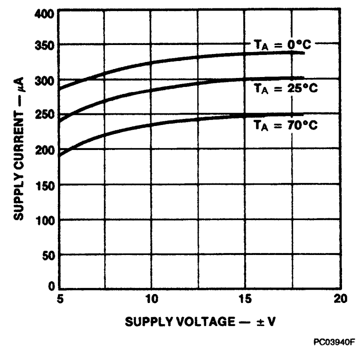
Voltage Gain vs Supply Voltage



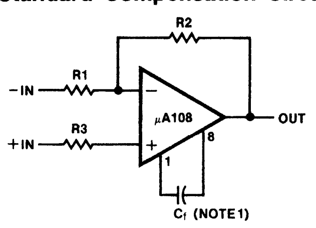
Output Swing vs Output Current

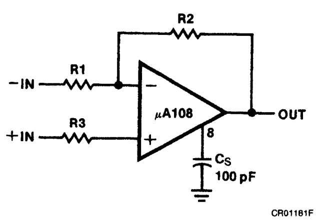


Supply Current vs Supply Voltage



Standard Compensation Circuits



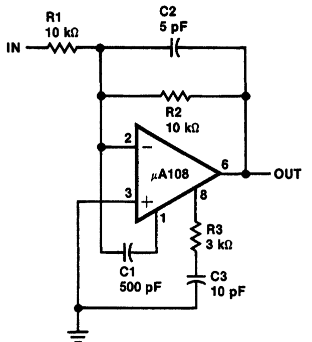


Note

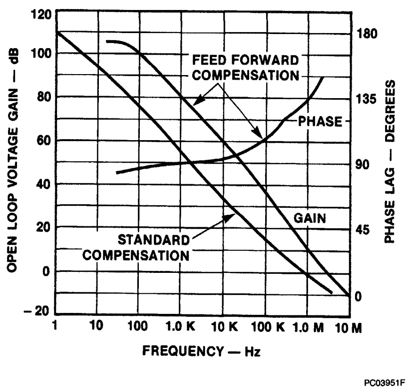
1. $C_F \geqslant 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$

Feed Forward Compensation Higher Slew Rate and Wider Bandwidth

Standard Feed Forward



Open Loop Frequency Response

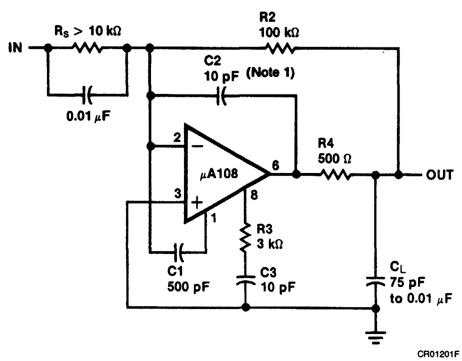


Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the μA108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination. Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input leads are adjacent to leads that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage leads are then absorbed by the guard.

The lead configuration of the dual-in-line package is designed to facilitate guarding, since the leads adjacent to the inputs are not used (this is different from the standard μA741 and μA101A lead configuration).

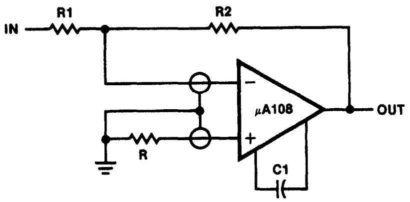
Feed Forward Compensation for Decoupling Load Capacitance



Note

1. $C_2 > \frac{5 \times 10^5}{R_2}$ pF

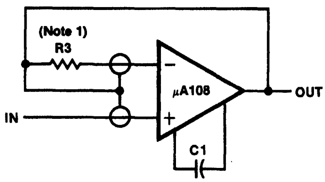
Inverting Amplifier



CR01211F

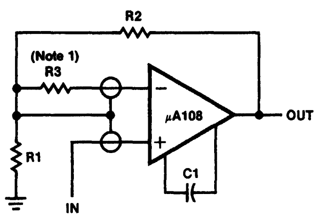
$R = R_1 || R_2$ (must be low impedance)

Follower



CR01221F

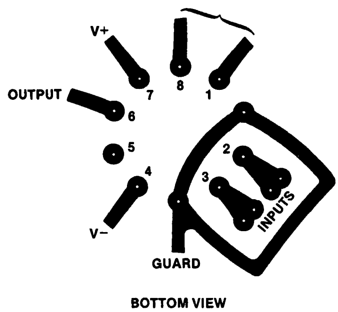
Non-Inverting Amplifier



CR01231F

Note
1. Use to compensate for large source resistances.

Board Layout for Input Guarding With Metal Package



CR01240F

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FAIRCHILD

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μA124 • μA224 • μA324 • μA2902 Quad Operational Amplifiers

Description

The μA124 series of quad operational amplifiers consists of four independent high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. They are constructed using the Fairchild Planar Epitaxial process.

- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**
- **Output Voltage Can Swing To Ground Or Negative Supply**
- **Four Internally Compensated Operational Amplifiers In A Single Package**
- **Wide Power Supply Range; Single Supply Of 3.0 V to 30 V, Dual Supply of ± 1.5 V to ± 16 V**
- **Power Drain Suitable For Battery Operation**

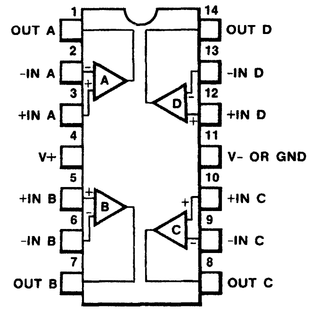
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA124M)	-55°C to +125°C
Automotive (μA2902V)	-40°C to +85°C
Industrial (μA224V)	-25°C to +85°C
Commercial (μA324C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage Between V+ and V-	32 V
Differential Input Voltage[3]	32 V
Input Voltage[3]	-0.3 V (V-) to V+

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} - 1.5 V, but either or both inputs can go to +32 V without damage (+26 V for μA2902).
4. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Connection Diagram
14-Lead DIP and SO-14 Package
(Top View)



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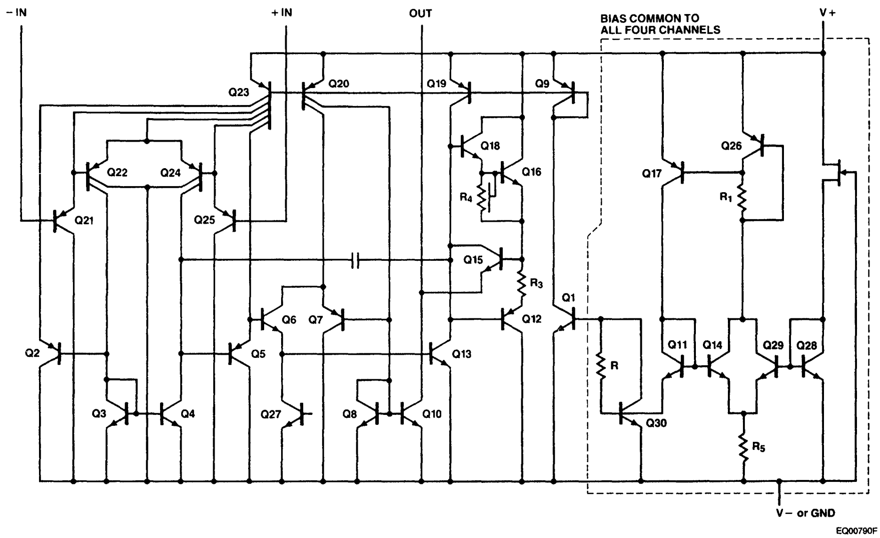
Order Information

Device Code	Package Code	Package Description
μA124DM	6A	Ceramic DIP
μA224DV	6A	Ceramic DIP
μA224PV	9A	Molded DIP
μA324DC	6A	Ceramic DIP
μA324PC	9A	Molded DIP
μA324SC	KD	Molded Surface Mount
μA2902PV	9A	Molded DIP

Equivalent Circuit (1/4 of Circuit)



μA124, μA224 and μA324
Electrical Characteristics T_A = 25°C, V+ = 5.0 V, V− = GND, unless otherwise specified.

Symbol	Characteristic	Condition	μA124/A224			μA324			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	V+ = 5.0 V to 30 V V_{CM} = 0 V to (V−) − 1.5 V, $V_O \simeq 1.4$ V, $R_S \leqslant 50\ \Omega$		2.0	5.0		2.0	7.0	mV
I_{IO}	Input Offset Current			3.0	30		5.0	50	nA
I_{IB}	Input Bias Current			45	150		45	250	nA
CMR	Common Mode Rejection	$R_S \leqslant 10$ kΩ	70	85		65	70		dB
V_{IR}	Input Voltage Range	V+ = 30 V	0		28.5	0		28.5	V
PSRR	Power Supply Rejection Ratio		65	100		65	100		dB
I_{OS}	Output Short Circuit Current[1]			40	60		40	60	mA
I_{O+}	Output Source Current	V_{ID} = 1.0 V, V+ = 15 V	20	40		20	40		mA
I_{O-}	Output Sink Current	V_{ID} = −1.0 V, V+ = 15 V	10	20		10	20		mA
		V_{ID} = −1.0 V, V_O = 200 mV	12	50		12	50		μA
A_{VS}	Large Signal Voltage Gain	V+ = 15 V, $R_L \geqslant 2.0$ kΩ	50	100		25	100		V/mV
CS	Channel Separation	1.0 kHz ≤ f ≤ 20 kHz, (Input Referenced)		−120			−120		dB

μA124, μA224 and μA324 (Cont.)
Electrical Characteristics $T_A = 25°C$, V + = 5.0 V, V − = GND, unless otherwise specified.

Symbol	Characteristic	Condition	μA124/A224 Min	μA124/A224 Typ	μA124/A224 Max	μA324 Min	μA324 Typ	μA324 Max	Unit
The following specifications apply over the range of $-55°C \leq T_A \leq +125°C$ for the μA124; $-25°C \leq T_A \leq +85°C$ for the μA224; and the $0°C \leq T_A \leq +70°C$ for the μA324.									
V_{IO}	Input Offset Voltage	V + = 5.0 V to 30 V, V_{CM} = 0 V to V − = 2.0 V, $V_O \simeq 1.4$ V, $R_S \leq 50\ \Omega$			7.0			9.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			7.0			7.0		μV/°C
I_{IO}	Input Offset Current				100			150	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			10			10		pA/°C
I_{IB}	Input Bias Current			40	300		50	500	nA
I_{CC}	Supply Current	V_O = 0 V, $R_L = \infty$		0.7	1.2		0.7	1.2	mA
		V + = 30 V, V_O = 0 V, $R_L = \infty$		1.5	3.0		1.5	3.0	
V_{IR}	Input Voltage Range	V + = 30 V	0		28	0		28	V
I_{O+}	Output Source Current	V_{IO} = +1.0 V, V + = 15 V	10	20		10	20		mA
I_{O-}	Output Sink Current	V_{IO} = −1.0 V, V + = 15 V	5.0	8.0		5.0	8.0		mA
A_{VS}	Large Signal Voltage Gain	V + = 15 V, $R_L \geq 2.0$ kΩ	25			15			V/mV
V_{OH}	Output Voltage HIGH	V + = 30 V, R_L = 10 kΩ	27	28		27	28		V
		V + = 30 V, R_L = 2.0 kΩ	26			26			
V_{OL}	Output Voltage LOW	V + = 5.0 V, R_L = 10 kΩ		5.0	20		5.0	20	mV

μA2902
Electrical Characteristics $T_A = 25°C$, V + = 5.0 V, V − = GND, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	V + = 5.0 V to 26 V, V_{CM} = 0 V to (V−) − 1.5 V, $V_O \simeq 1.4$ V, $R_S \leq 50\ \Omega$		2.0	7.0	mV
I_{IO}	Input Offset Current			5.0	50	nA
I_{IB}	Input Bias Current			45	250	nA
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	50	70		dB
V_{IR}	Input Voltage Range	V_{CC} = 26 V	0		24.5	V
PSRR	Power Supply Rejection Ratio		50	100		dB
I_{OS}	Output Short Circuit Current[1]			40	60	mA

μA2902 (Cont.)
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, V− = GND, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{O+}	Output Source Current	$V_{ID} = +1.0$ V, V+ = 15 V	20	40		mA
I_{O-}	Output Sink Current	$V_{ID} = -1.0$ V, V+ = 15 V	10	20		mA
A_{VS}	Large Signal Voltage Gain	V+ = 15 V, $R_L \geq 2.0$ kΩ	15	100		V/mV
CS	Channel Separation	1.0 kHz ≤ f ≤ 20 kHz, Input Referenced		−120		dB

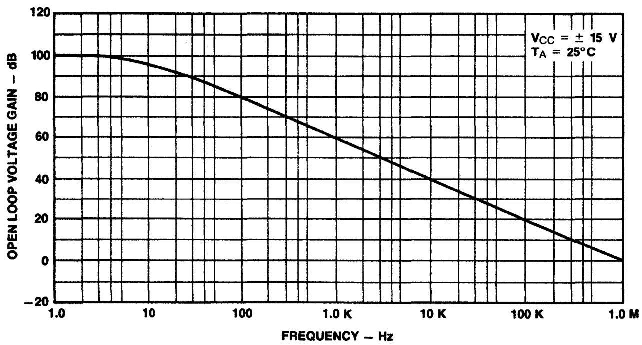
The following specifications apply over the operating temperature range of $-40°C \leq T_A \leq +85°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	V+ = 5.0 V to 26 V, $V_{CM} = 0$ V to V− = 2.0 V, $V_O \simeq 1.4$ V, $R_S \leq 50$ Ω			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			7.0		μV/°C
I_{IO}	Input Offset Current			45	200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			10		pA/°C
I_{IB}	Input Bias Current			50	500	nA
I_{CC}	Supply Current	$V_O = 0$ V, $R_L = \infty$		0.7	1.2	mA
		V+ = 26 V, $V_O = 0$ V, $R_L = \infty$		1.5	3.0	mA
V_{IR}	Input Voltage Range	V+ = 26 V	0		24	V
I_{O+}	Output Source Current	$V_{ID} = +1.0$ V, V+ = 15 V	10	20		mA
I_{O-}	Output Sink Current	$V_{ID} = -1.0$ V, V+ = 15 V	5.0	8.0		mA
A_{VS}	Large Signal Voltage Gain	V+ = 15 V, $R_L \geq 2.0$ kΩ	15	100		V/mV
V_{OH}	Output Voltage HIGH	V+ = 26 V, $R_L = 2.0$ kΩ	22			V
		V+ = 26 V, $R_L = 10$ kΩ	23	24		
V_{OL}	Output Voltage LOW	V+ = 5.0 V, $R_L = 10$ kΩ		5.0	100	mV

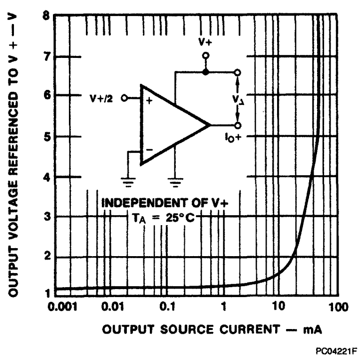
Notes
1. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Typical Performance Curves

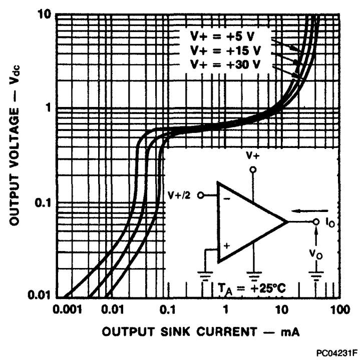
Open Loop Frequency Response



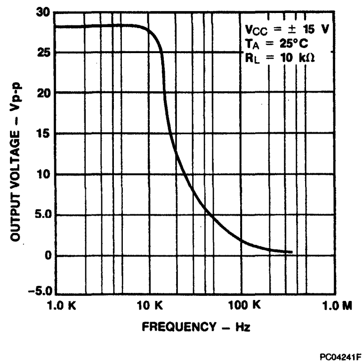
Output Characteristics Current Sourcing



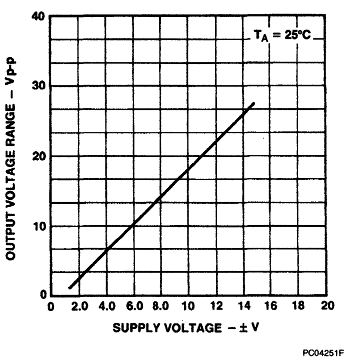
Output Characteristics Current Sinking



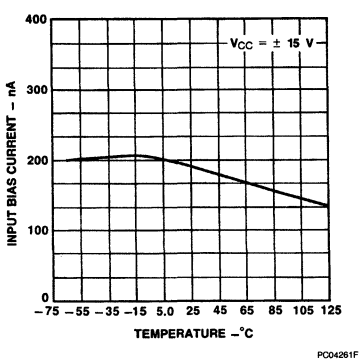
Output Voltage vs Frequency



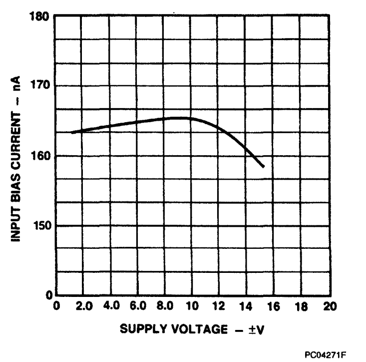
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage



FAIRCHILD
A Schlumberger Company

μA1458 • μA1558 Dual Internally Compensated Operational Amplifiers

Linear Division Operational Amplifiers

Description

The μA1458, μA1558 are a monolithic pair of internally frequency compensated high performance amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch up make the μA1458, μA1558 ideal for use as voltage followers. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.
The μA1458, μA1558 are short circuit protected and require no external components for frequency compensation. The internal 6.0 db/octave roll off ensures stability in closed loop applications. For single amplifier performance, *see the μA741 data sheet.*
The Fairchild μA1458, μA1558 slew rate has been improved to 0.8/μs typical.

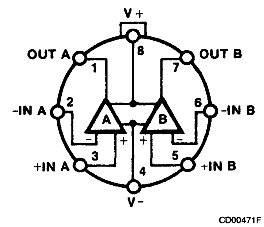
- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**
- **Mini-Dip Package**

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA1558M)	−55°C to +125°C
Commercial (μA1458C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	
μA1558	±22 V
μA1458	±18 V
Differential Input Voltage	±30 V
Common Mode Input Swing[3]	±15 V
Output Short Circuit Duration[4]	Indefinite

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 70°C ambient temperature.

Connection Diagram 8-Lead Metal Package (Top View)

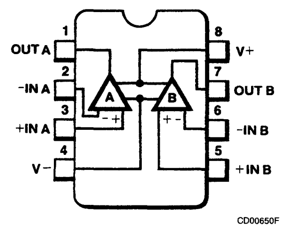


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA1458HC	5W	Metal
μA1458CHC	5W	Metal
μA1558HM	5W	Metal

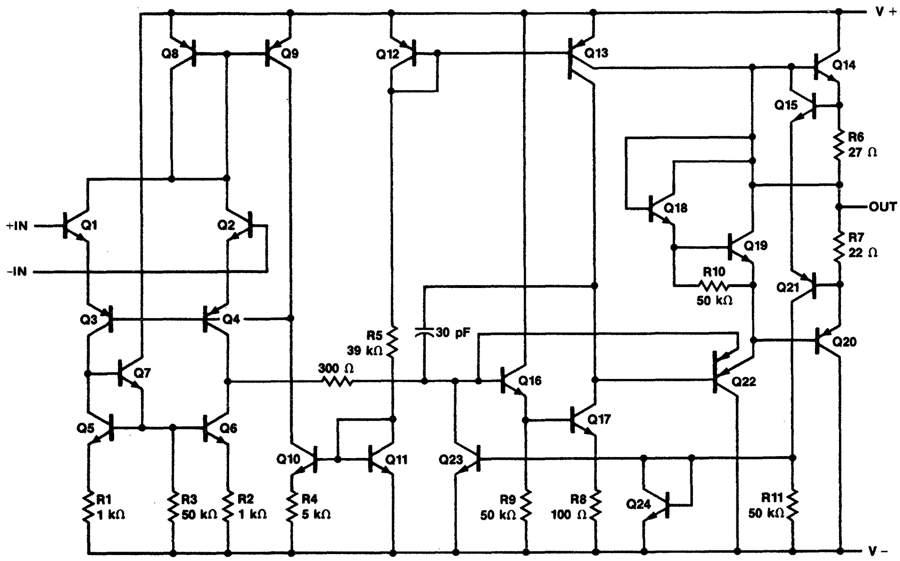
Connection Diagram 8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA1458RC	6T	Ceramic DIP
μA1458SC	KC	Molded Surface Mount
μA1458TC	9T	Molded DIP
μA1458CRC	6T	Ceramic DIP
μA1458CTC	9T	Molded DIP
μA1558RM	6T	Ceramic DIP

Equivalent Circuit (1/2 of Circuit)



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μA1458 and μA1458C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	μA1458 Min	μA1458 Typ	μA1458 Max	μA1458C Min	μA1458C Typ	μA1458C Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		2.0	10	mV
I_{IO}	Input Offset Current			0.03	0.2		0.03	0.3	μA
I_{IB}	Input Bias Current			0.2	0.5		0.2	0.7	μA
Z_I	Input Impedance		0.3	1.0			1.0		MΩ
I_{CC}	Supply Current			2.3	5.6		2.3	8.0	mA
P_c	Power Consumption	$V_O = 0$ V		70	170		70	240	mW
CMR	Common Mode Rejection		70	90		60	90		dB
V_{IR}	Input Voltage Range		±12	±13		±11	±13		V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30		μV/V
I_{OS}	Output Short Circuit Current			20			20		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm10$ V, $R_L \geq 2.0$ kΩ	20	100		20	100		V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±14		±11	±14		V
fc	Unity Gain Crossover Frequency			1.1			1.1		MHz
SR	Slew Rate	$A_V = 1.0$		0.8			0.8		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$									
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			12	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50$ Ω		15			15		μV/°C
I_{IO}	Input Offset Current				0.3			0.4	μA
I_{IB}	Input Bias Current				0.8			1.0	μA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm10$ V, $R_L \geq 2.0$ kΩ	15			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10	±13		±9.0	±13		V

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μA1558

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

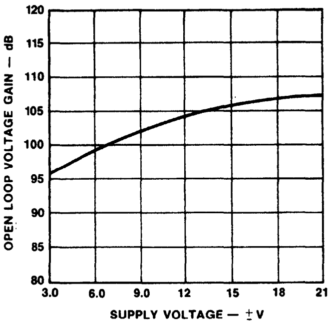
Symbol	Characteristic	Condition	μA1558 Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
I_{IO}	Input Offset Current			0.03	0.2	μA
I_{IB}	Input Bias Current			0.2	0.5	μA
Z_I	Input Impedance		0.3	1.0		MΩ
I_{CC}	Supply Current			2.3	5.0	mA
P_c	Power Consumption	$V_O = 0$ V		70	150	mW
CMR	Common Mode Rejection		70	90		dB
V_{IR}	Input Voltage Range		±12	±13		V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
I_{OS}	Output Short Circuit Current			20		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	50	200		V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±14		V
fc	Unity Gain Crossover Frequency			1.1		MHz
SR	Slew Rate	$A_V = 1.0$		0.8		V/μs

The following specifications apply for $-55°C \leq T_A \leq +125°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50$ Ω		15		μV/°C
I_{IO}	Input Offset Current				0.5	μA
I_{IB}	Input Bias Current				1.5	μA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10	±13		V

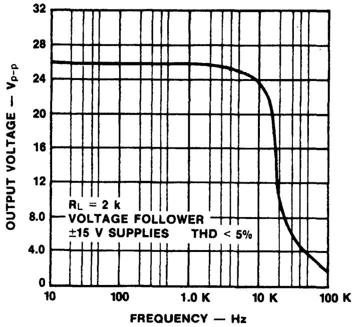
Typical Performance Curves $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified

Voltage Gain vs Supply Voltage



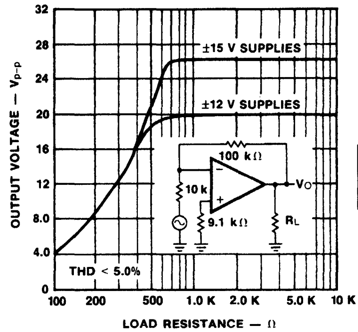
PC02411F

Power Bandwidth (Large Signal Swing vs Frequency)



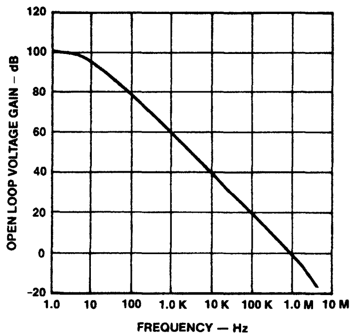
PC02421F

Output Voltage Swing vs Load Resistance



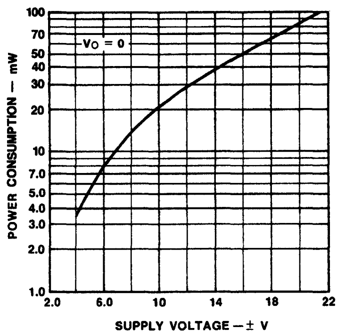
PC02431F

Open Loop Frequency Response



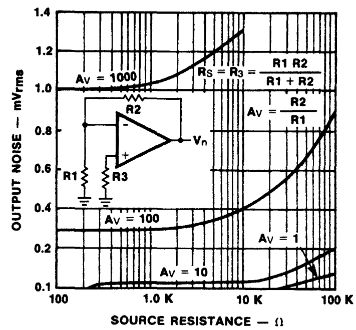
PC02441F

Power Consumption vs Supply Voltage



PC02451F

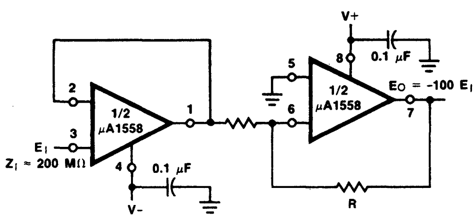
Output Noise vs Source Resistance



PC02461F

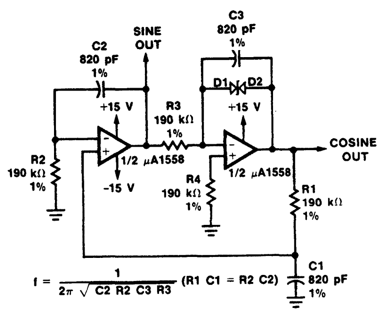
Typical Applications

High Impedance, High Gain Inverting Amplifier



AF00190F

Quadrature Oscillator



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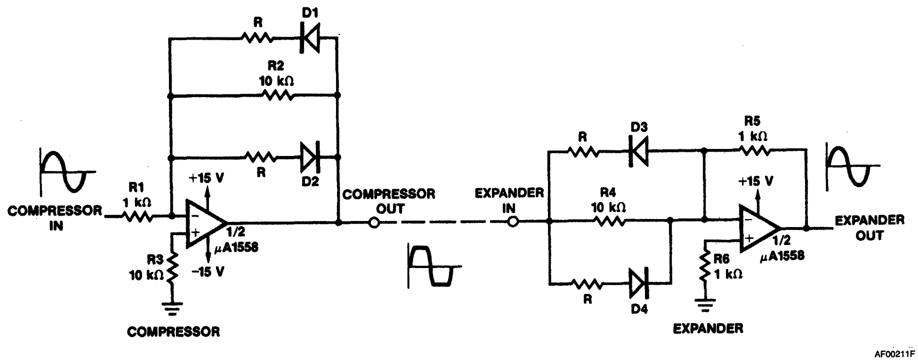
Typical Applications (Cont.)

Compressor/Expander Amplifiers

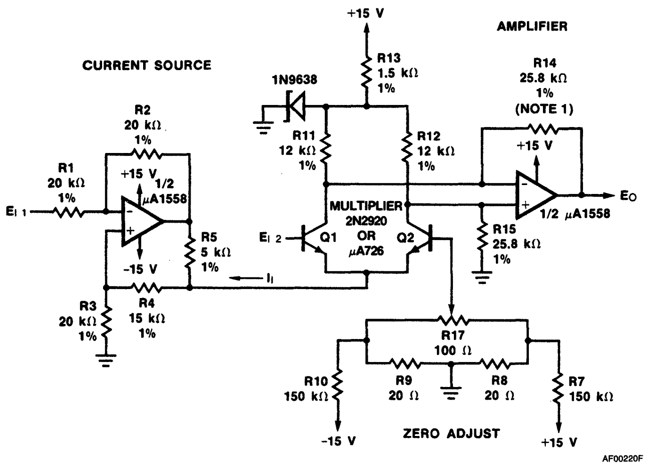


Notes

Maximum compression expansion ratio = R_1/R ($10\ k\Omega > R \geq 0$)

Diodes D1 through D4 are matched FD6666 or equivalent

Analog Multiplier



Note

1. Matched to 0.1%

   $E_O = 100\ E_{I1} \times E_{I2}$

FAIRCHILD

A Schlumberger Company

μA148 • μA248 • μA348 Quad Operational Amplifiers

Linear Division Operational Amplifiers

Description

The μA148 series is a true quad μA741. It consists of four independent, high gain, internally frequency compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar μA741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single μA741 type operational amplifier.

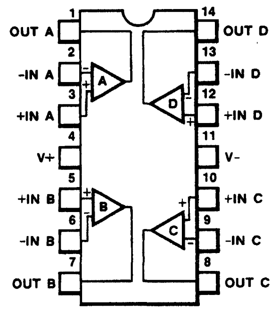
Other features include input offset currents and input bias currents which are much less than those of a standard μA741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

- **μA741 Op Amp Operating Characteristics**
- **Low Supply Current Drain**
- **Class AB Output Stage — No Crossover Distortion**
- **Lead Compatible With The μA324 & μA3403**
- **Low Input Offset Voltage — 1.0 mV Typically**
- **Low Input Offset Current — 4.0 nA Typically**
- **Low Input Bias Current — 30 nA Typically**
- **Gain Bandwidth Product For μA148 (Unity Gain) — 1.0 MHz Typically**
- **High Degree Of Isolation Between Amplifiers — 120 dB Typically**
- **Overload Protection For Inputs And Outputs**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA148M)	-55°C to +125°C
Industrial (μA248V)	-25°C to +85°C
Commercial (μA348C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
14L-Molded DIP	1.04 W
14L-Ceramic DIP	1.36 W
Supply Voltage	
μA148	±22 V
μA248, μA348	±18 V
Differential Input Voltage	
μA148	±44 V
μA248, μA348	±36 V
Input Voltage	
μA148	±22 V
μA248, μA348	±18 V
Output Short Circuit Duration[3]	Indefinite

Connection Diagram
14-Lead DIP
(Top View)



CD00561F

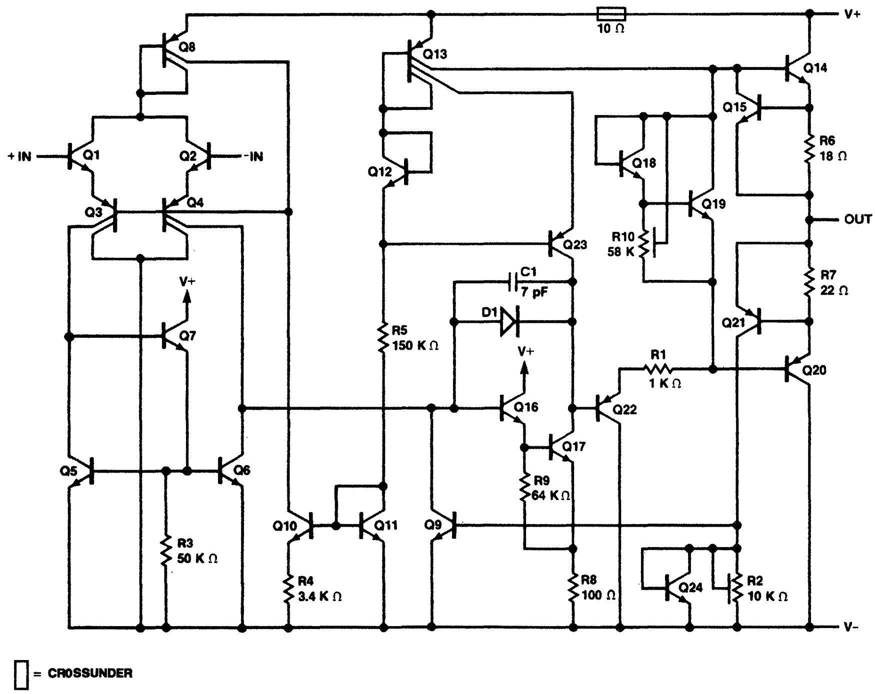
Order Information

Device Code	Package Code	Package Description
μA148DM	6A	Ceramic DIP
μA248DV	6A	Ceramic DIP
μA248PV	9A	Molded DIP
μA348DC	6A	Ceramic DIP
μA348PC	9A	Molded DIP

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14-Lead Molded DIP at 8.3 mW/°C, and the 14-Lead Ceramic DIP at 9.1 mW/°C.
3. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Equivalent Circuit (1/4 of Circuit)



EQ00061F

μA148

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 10$ kΩ		1.0	5.0	mV
I_{IO}	Input Offset Current			4	25	nA
I_{IB}	Input Bias Current			30	100	nA
Z_I	Input Impedance		0.8	2.5		MΩ
I_{CC}	Supply Current (Total)			2.4	3.6	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50	160		V/mV
CS	Channel Separation	1.0 Hz $\leqslant f \leqslant$ 20 kHz (Input Referred)		−120		dB

The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 10$ kΩ			6.0	mV
I_{IO}	Input Offset Current				75	nA
I_{IB}	Input Bias Current				325	nA
CMR	Common Mode Rejection	$R_S \leqslant 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range		±12			V
PSRR	Power Supply Rejection Ratio	$R_S \leqslant 10$ kΩ	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
		$R_L = 2.0$ kΩ	±10	±12		

AC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/μs

μA248
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
I_{IO}	Input Offset Current			4	50	nA
I_{IB}	Input Bias Current			30	200	nA
Z_I	Input Impedance		0.8	2.5		MΩ
I_{CC}	Supply Current (Total)			2.4	4.5	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25	160		V/mV
CS	Channel Separation	1.0 Hz $\leq f \leq$ 20 kHz (Input Referred)		−120		dB
The following specifications apply over the range of $-25°C \leq T_A \leq +85°C$.						
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
I_{IO}	Input Offset Current				125	nA
I_{IB}	Input Bias Current				500	nA
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range		±12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
		$R_L = 2.0$ kΩ	±10	±12		

AC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/μs

μA348
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characterisitcs

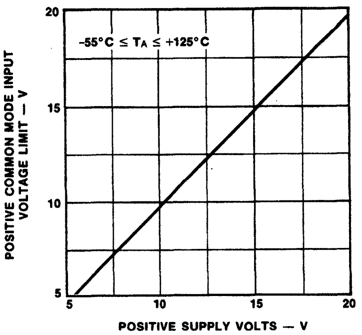
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
I_{IO}	Input Offset Current			4	50	nA
I_{IB}	Input Bias Current			30	200	nA
Z_I	Input Impedance		0.8	2.5		MΩ
I_{CC}	Supply Current (Total)			2.4	4.5	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25	160		V/mV
CS	Channel Separation	1.0 Hz ≤ f ≤ 20 kHz (Input Referred)		−120		dB
The following specifications apply over the range of $0°C \leq T_A \leq +70°C$.						
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
I_{IO}	Input Offset Current				100	nA
I_{IB}	Input Bias Current				400	nA
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range		±12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
		$R_L = 2.0$ kΩ	±10	±12		

AC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/μs

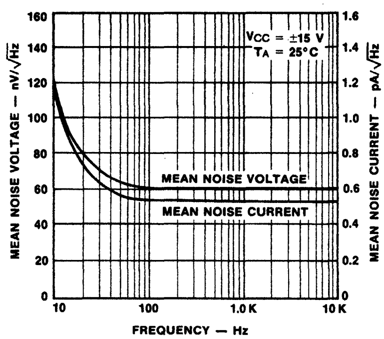
Typical Performance Curves

Positive Common Mode Input Voltage Limit vs Supply Voltage



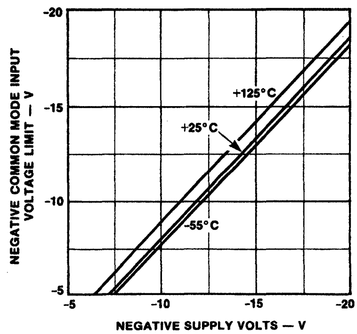
PC02941F

Input Noise Voltage and Noise Current vs Frequency



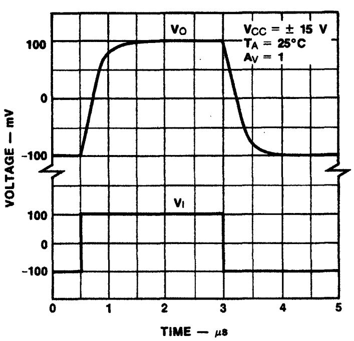
PC02961F

Negative Common Mode Input Voltage Limit vs Supply Voltage



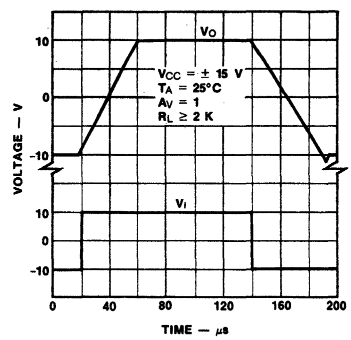
PC02951F

Small Signal Pulse Response



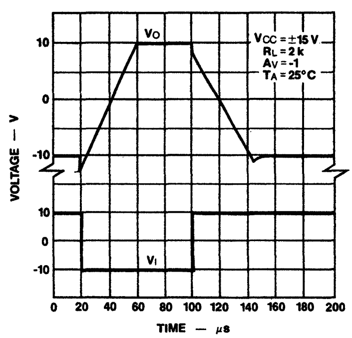
PC02971F

Large Signal Pulse Response



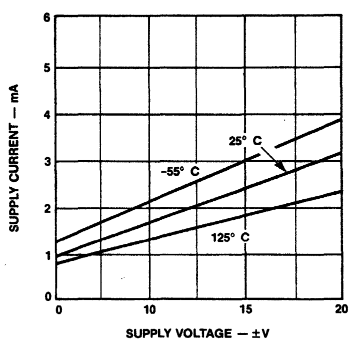
PC02981F

Inverting Large Signal Pulse Response



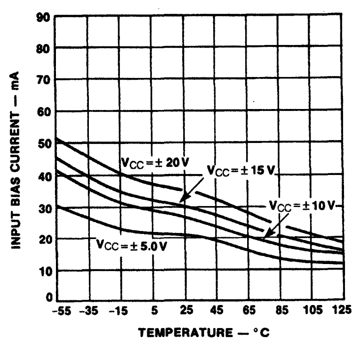
PC02990F

Supply Current vs Power Supply Voltage



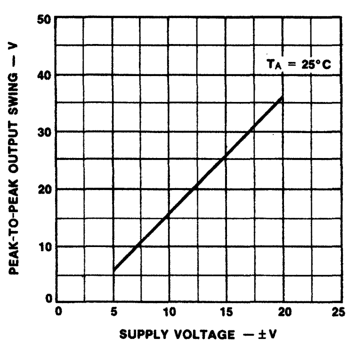
PC03971F

Input Bias Current vs Ambient Temperature



PC03001F

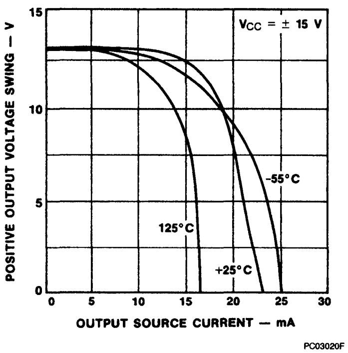
Output Voltage Swing vs Supply Voltage



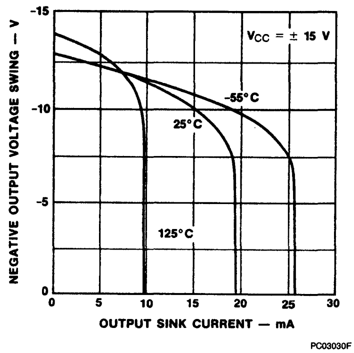
PC03011F

Typical Performance Curves (Cont.)

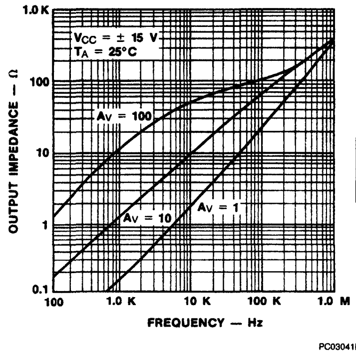
Output Voltage vs Source Current



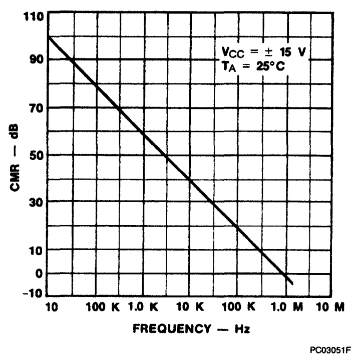
Output Voltage vs Sink Current



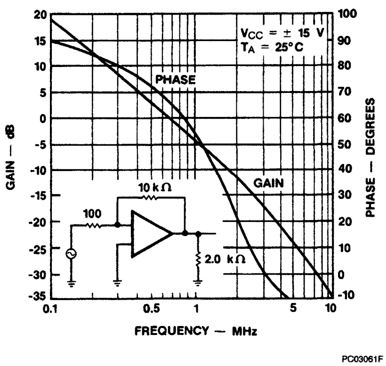
Output Impedance vs Frequency



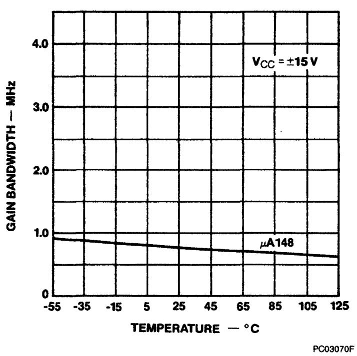
CMR vs Frequency



Gain and Phase vs Frequency



Gain Bandwidth vs Temperature



7

FAIRCHILD

A Schlumberger Company

μA3303 • μA3403 • μA3503 Quad Operational Amplifiers

Description

The μA3303, μA3403, and μA3503 are monolithic quad operational amplifiers consisting of four independent high gain, internally frequency compensated, operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. They are constructed using the Fairchild Planar Epitaxial process.

- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**
- **Output Voltage Can Swing To Ground Or Negative Supply**
- **Four Internally Compensated Operational Amplifiers In A Single Package**
- **Wide Power Supply Range Single Supply Of 3.0 V To 36 V Dual Supply Of ±1.5 To ±18 V**
- **Class AB Output Stage For Minimal Crossover Distortion**
- **Short Circuit Protected Outputs**
- **High Open Loop Gain 200K Typically**
- **μA741 Operational Amplifier Type Performance**

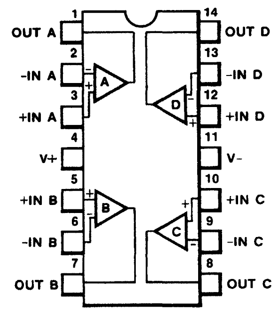
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Extended (μA3503M)	−55°C to +125°C
Industrial (μA3303V)	−40°C to +85°C
Commercial (μA3403C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Disisipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage Between V+ and V−	36 V
Differential Input Voltage[3]	±30 V
Input Voltage (V − 1)[3]	−0.3 V (V−) to V+

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 14-Lead DIP and SO-14 Package (Top View)

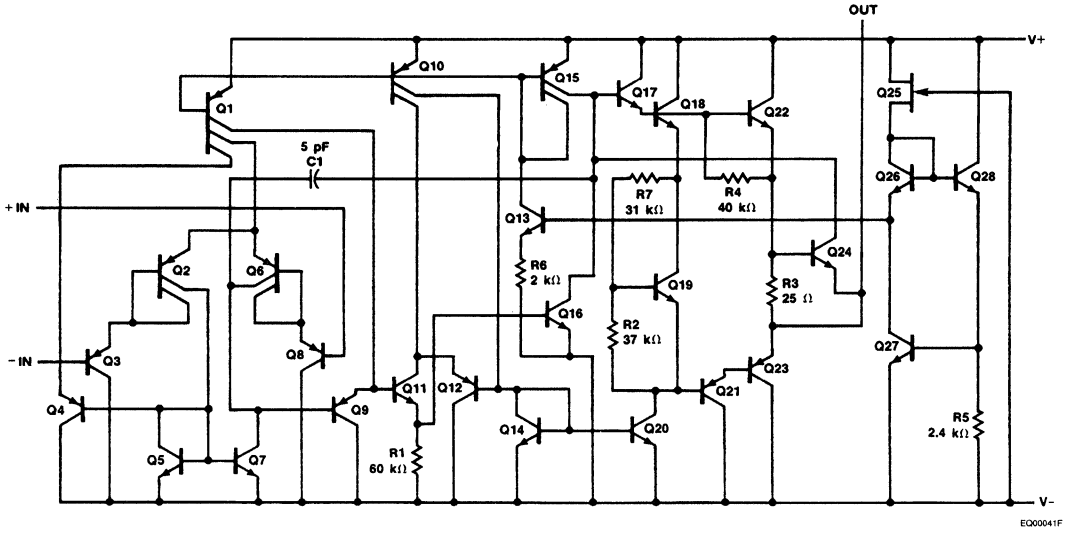


CD00561F

Order Information

Device Code	Package Code	Package Description
μA3303DV	6A	Ceramic DIP
μA3303PV	9A	Molded DIP
μA3403DC	6A	Ceramic DIP
μA3403PC	9A	Molded DIP
μA3403SC	KD	Molded Surface Mount
μA3503DM	6A	Ceramic DIP

Equivalent Circuit (1/4 of Circuit)



μA3303 and μA3403
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	μA3303			μA3403			Unit
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				2.0	8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				30	75		30	50	nA
I_{IB}	Input Bias Current				200	500		200	500	nA
Z_I	Input Impedance			0.3	1.0		0.3	1.0		MΩ
I_{CC}	Supply Current		$V_O = 0$ V, $R_L = \infty$		2.8	7.0		2.8	7.0	mA
CMR	Common Mode Rejection		$R_S \leqslant 10$ kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range			+12 to V−	+12.5 to V−		+13 to V−	+13.5 to V−		V
PSRR	Power Supply Rejection Ratio				30	150		30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier)[1]			±10	±30	±45	±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12	12.5		±12	+13.5		V
			$R_L = 2.0$ kΩ	±10	12		±10	±13		
TR	Transient Response	Rise time/ Fall time	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		0.3			0.3		μs
		Overshoot	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		5.0			5.0		%
BW	Bandwidth		$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		1.0			1.0		MHz
SR	Slew Rate		$V_I = -10$ V to +10 V, $A_V = 1.0$		0.6			0.6		V/μs

The following specifications apply for $-40°C \leqslant T_A \leqslant +85°C$ for the μA3303, and $0°C \leqslant T_A \leqslant +70°C$ for the μA3403.

Symbol	Characteristic	Condition	μA3303 Min	μA3303 Typ	μA3303 Max	μA3403 Min	μA3403 Typ	μA3403 Max	Unit
V_{IO}	Input Offset Voltage				10			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10			10		μV/°C
I_{IO}	Input Offset Current				250			200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50			50		pA/°C
I_{IB}	Input Bias Current				1000			800	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	15			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10			±10			V

μA3303 and μA3403 (Cont.)
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, V− = Gnd, unless otherwise specified.

Symbol	Characteristic	Condition	μA3303 Min	μA3303 Typ	μA3303 Max	μA3403 Min	μA3403 Typ	μA3403 Max	Unit
V_{IO}	Input Offset Voltage				8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				75		30	50	nA
I_{IB}	Input Bias Current				500		200	500	nA
I_{CC}	Supply Current			2.5	7.0		2.5	7.0	mA
PSRR	Power Supply Rejection Ratio				150			150	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing[2]	$R_L = 10$ kΩ	3.3			3.3			V
		5.0 V ⩽ V+ ⩽ 30 V, $R_L = 10$ kΩ	(V+) −2.0			(V+) −2.0			
CS	Channel Separation	1.0 Hz ⩽ f ⩽ 20 kHz (Input Referenced)		−120			−120		dB

μA3503
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage				2.0	5.0	mV
I_{IO}	Input Offset Current				30	50	nA
I_{IB}	Input Bias Current				200	500	nA
Z_I	Input Impedance			0.3	1.0		MΩ
I_{CC}	Supply Current		$V_O = 0$, $R_L = \infty$		2.8	4.0	mA
CMR	Common Mode Rejection		$R_S \leqslant 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range			+13 to V−	+13.5 to V−		V
PSRR	Power Supply Rejection Ratio				30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier)[1]			±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12	±13.5		V
			$R_L = 2.0$ kΩ	±10	±13		
TR	Transient Response	Rise time	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		0.3		μs
		Overshoot	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		5.0		%
BW	Bandwidth		$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		1.0		MHz
SR	Slew Rate		$V_I = -10$ V to +10 V, $A_V = 1.0$		0.6		V/μs

μA3503
Electrical Characteristics $-55°C \leqslant T_A \leqslant +125°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	μA3503 Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage				6.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10		μV/°C
I_{IO}	Input Offset Current				200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50		pA/°C
I_{IB}	Input Bias Current				1200	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10			V

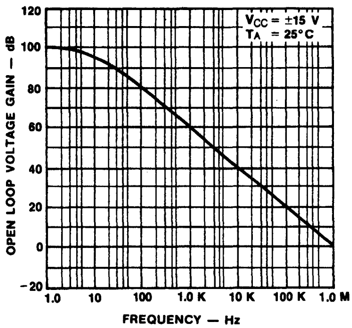
The following specifications apply for $T_A = 25°C$, $V+ = +5.0$ V, $V- =$ GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage			2.0	5.0	mV
I_{IO}	Input Offset Current			30	50	nA
I_{IB}	Input Bias Current			200	500	nA
I_{CC}	Supply Current			2.5	4.0	mA
PSRR	Power Supply Rejection Ratio				150	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ	20	200		V/mV
V_{OP}	Output Voltage Swing[2]	$R_L = 10$ kΩ	3.3			V
		$5.0 \text{ V} \leqslant V+ \leqslant 30$ V, $R_L = 10$ kΩ	(V+) −2.0			
CS	Channel Separation	1.0 Hz ≤ f ≤ 20 kHz (Input Referenced)		−120		dB

Notes
1. Not to exceed maximum package power dissipation.
2. Output will swing to ground.

Typical Performance Curves

Open Loop Frequency Response



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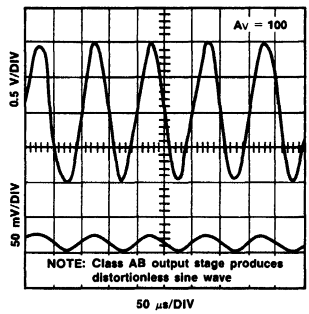
Sine Wave Response



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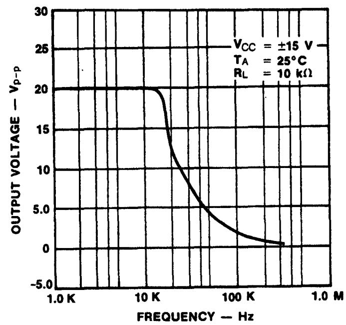
Output Voltage vs Frequency



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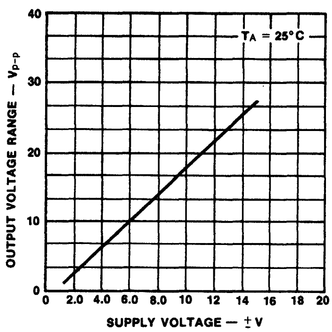
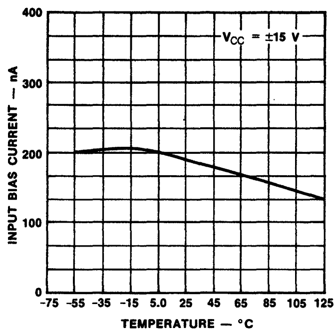
Output Swing vs Supply Voltage



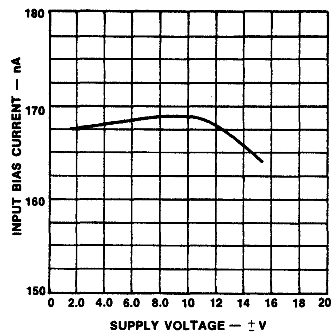
PC02621F

Input Bias Current vs Temperature



PC02630F

Input Bias Current vs Supply Voltage



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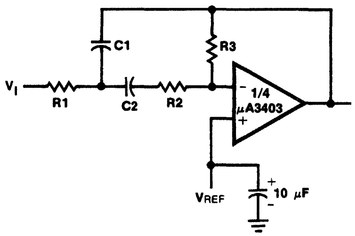
7

Typical Applications

Multiple Feedback Bandpass Filter



f_o = center frequency

BW = Bandwidth
R in kΩ
C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

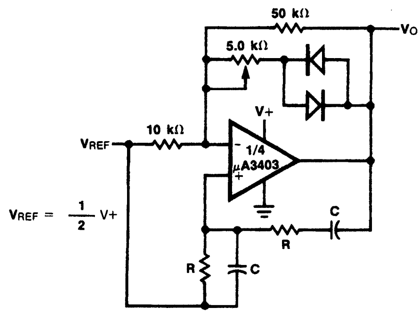
$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:
given: $Q = 5$, $f_o = 1$ kHz
Let R1 = R2 = 10 kΩ
then $R3 = 9(5)^2 - 10$
R3 = 215 kΩ

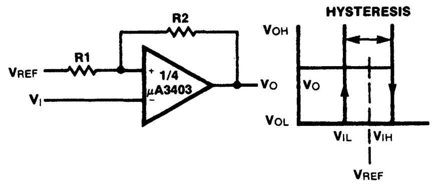
$$C = \frac{5}{3} = 1.6 \text{ nF}$$

Wein Bridge Oscillator



$$f_o = \frac{1}{2\pi RC}$$ for $f_o = 1$ kHz
R = 16 kΩ
C = 0.01 μF

Comparator With Hysteresis



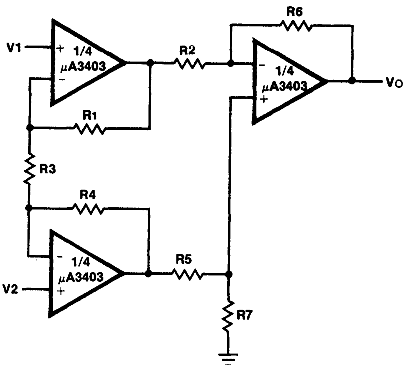
$$V_{IL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Typical Applications (Cont.)

High Impedance Differential Amplifier



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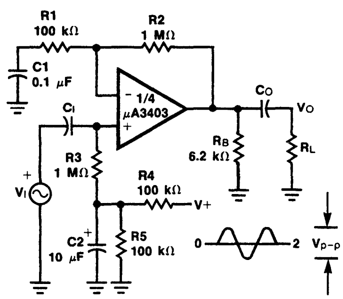
$V_{OUT} = C(1 + a + b)(V2 - V1)$

$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

R1 = R4
R2 = R5

$$\text{Gain} = \frac{R6}{R5}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$$

AC Coupled Non-Inverting Amplifier

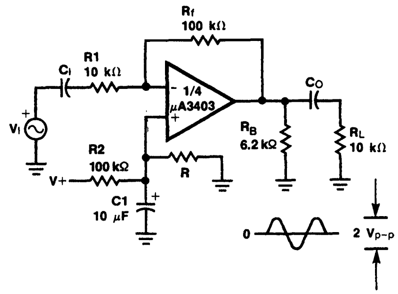


AF00360F

$A_V = 1 + \frac{R2}{R1}$

$A_V = 11$ (as shown)

AC Coupled Inverting Amplifier

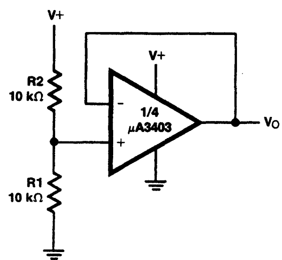


AF00350F

$A_V = \frac{Rf}{R1}$

$A_V = 10$ (as shown)

Voltage Reference

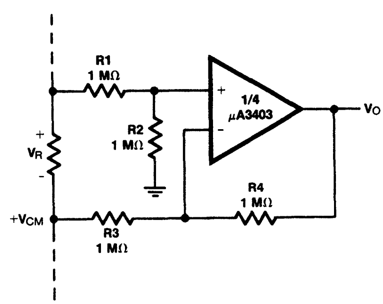


AF00380F

$$V_O = \frac{R1}{R1 + R2}\left(= \frac{V+}{2} \text{ as shown}\right)$$

$V_O = \frac{1}{2} V+$

Ground Referencing A Differential Input Signal



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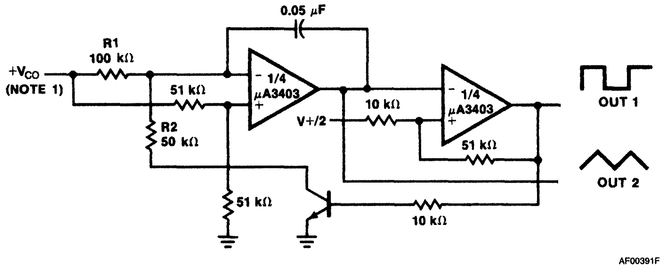
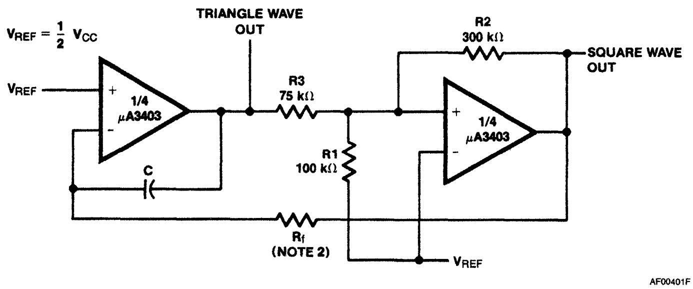
Typical Applications (Cont.)

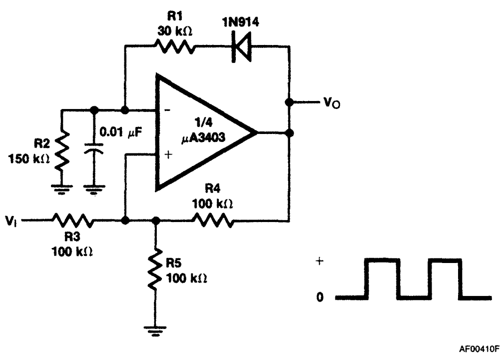
Voltage Controlled Oscillator



Function Generator



Pulse Generator

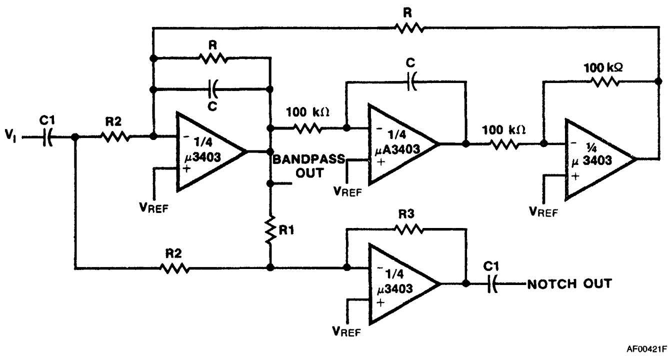


Note

1. Wide Control Voltage Range: $0V \leq V_{CO} \leq 2\ (V+ - 1.5\ V)$
2. $f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

Typical Applications (Cont.)

Bi-Quad Filter



$$Q = \frac{BW}{f_o}$$

where

T_{BP} = Center Frequency Gain

T_N = Bandpass Notch Gain

$$f_o = \frac{1}{2\pi RC},\ V_{REF} = \frac{1}{2} V_{CC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N R2$

$C1 = 10\ C$

Example:

$f_o = 1000$ Hz

$BW = 100$ Hz

$T_{BP} = 1$

$T_N = 1$

$R = 160$ kΩ

$R1 = 1.6$ MΩ

$R2 = 1.6$ MΩ

$R3 = 1.6$ MΩ

$C = 0.001\ \mu F$

FAIRCHILD
A Schlumberger Company

μA4136 Quad Operational Amplifier

Linear Products Operational Amplifiers

Description

The μA4136 Monolithic Quad Operational Amplifier consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the μA4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. It is constructed using the Fairchild Planar Epitaxial process. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

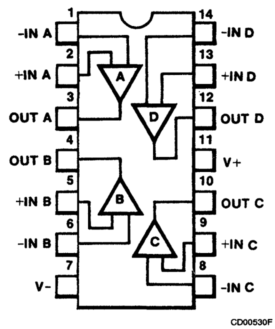
- **Unity Gain Bandwidth — 3.0 MHz Typically**
- **Continuous Short Circuit Protection**
- **No Frequency Compensation Required**
- **No Latch Up**
- **Large Common Mode and Differential Voltage Ranges**
- **μA741 Operational Amplifier Type Performance**
- **Parameter Tracking Over Temperature Range**
- **Gain and Phase Match Between Amplifiers**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Disisipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	±18 V
Differential Input Voltage[3]	±30 V
Input Voltage[1]	±15 V
Output Short Circuit Duration[4]	Indefinite

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Rating apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. For supply voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to ground, one amplifier only.

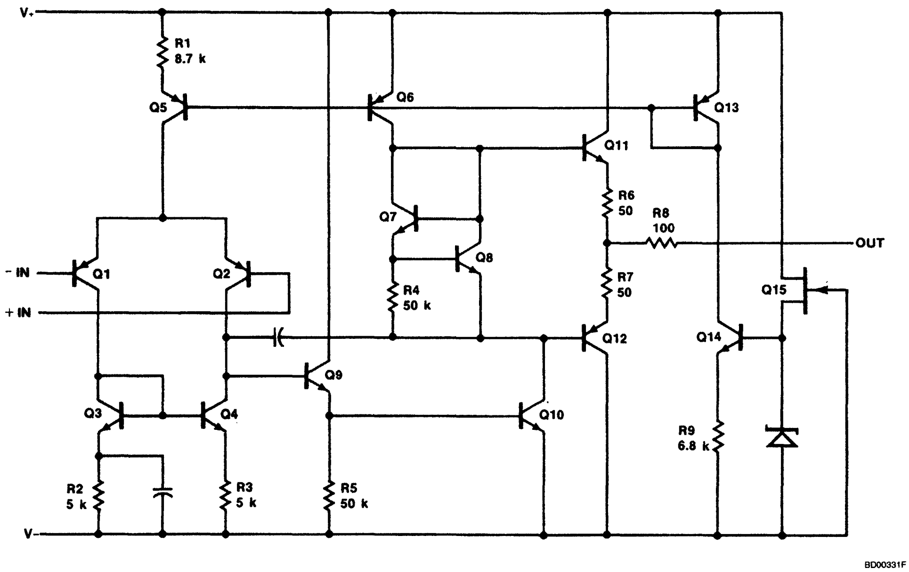
Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA4136DC	6A	Ceramic DIP
μA4136PC	9A	Molded DIP
μA4136SC	KD	Molded Surface Mount

Equivalent Circuit (1/4 of Circuit)



Note

1. All resistor values are in ohms.

μA4136

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

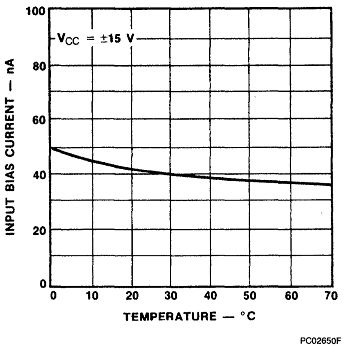
Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		0.5	6.0	mV
I_{IO}	Input Offset Current				5.0	200	nA
I_{IB}	Input Bias Current				40	500	nA
Z_I	Input Impedance			0.3	5.0		MΩ
P_c	Power Consumption				210	340	mW
CMR	Common Mode Rejection		$R_S \leqslant 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range			±12	±14		V
PSRR	Power Supply Rejection Ratio		$R_S \leqslant 10$ kΩ		30	150	μV/V
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	20	300		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12	±14		V
			$R_L = 2.0$ kΩ	±10	±13		
TR	Transient Response	Rise time	$V_I = 20$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.13		μs
		Overshoot			5.0		%
BW	Bandwidth		$A_V = 1.0$		3.0		MHz
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$		1.0		V/μS
CS	Channel Separation		f = 10 kHz, $R_S = 1.0$ kΩ, Open Loop		105		dB
			f = 10 kHz, $R_S = 1.0$ kΩ $A_V = 100$		105		

The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$ for μA4136; $0°C \leqslant T_A \leqslant +70°C$ for μA4136C.

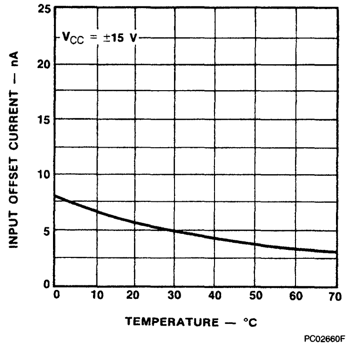
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 10$ kΩ			7.5	mV
I_{IO}	Input Offset Current				300	nA
I_{IB}	Input Bias Current				800	nA
P_c	Power Consumption	$T_A = T_{A\ Max}$		180	300	mW
		$T_A = T_{A\ Min}$		240	400	
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ $V_{CC} = \pm 15$ V	±10			V

Typical Performance Curves

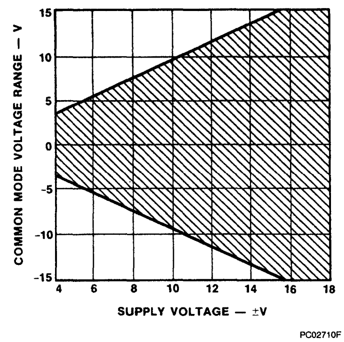
Input Bias Current vs Temperature



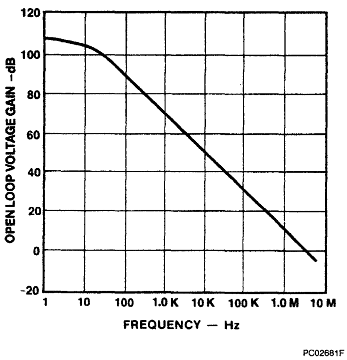
Input Offset Current vs Temperature



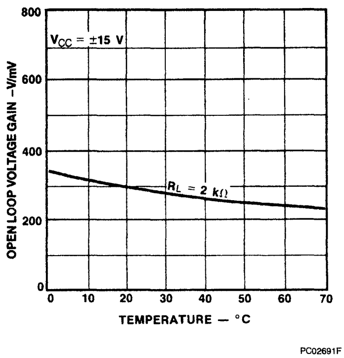
Common Mode Range vs Supply Voltage



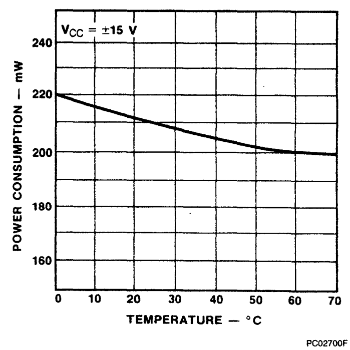
Open Loop Voltage Gain vs Frequency



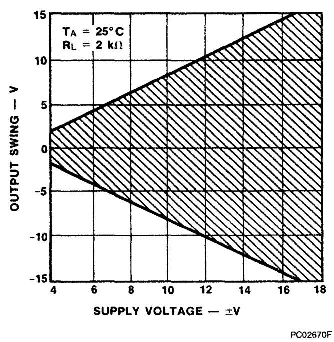
Open Loop Voltage Gain vs Temperature



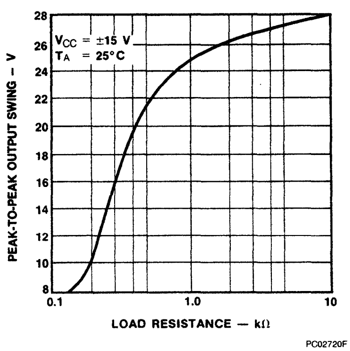
Power Consumption vs Temperature



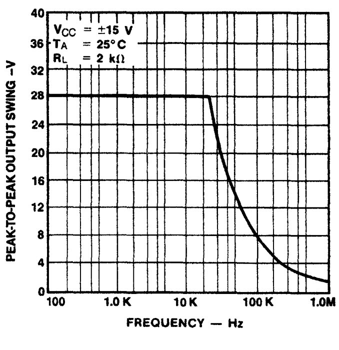
Typical Output Voltage vs Supply Voltage



Output Voltage Swing vs Load Resistance

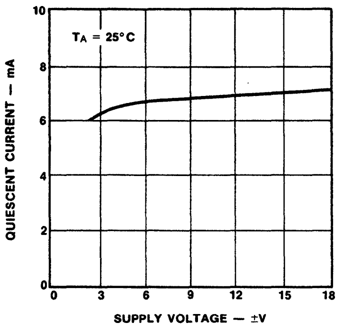


Output Voltage Swing vs Frequency



Typical Performance Curves (Cont.)

Quiescent Current vs Supply Voltage



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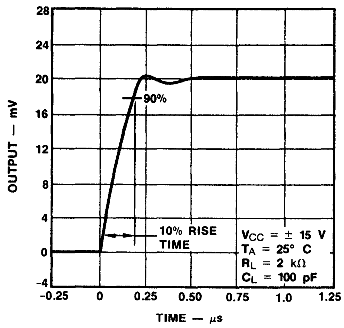
Transient Response



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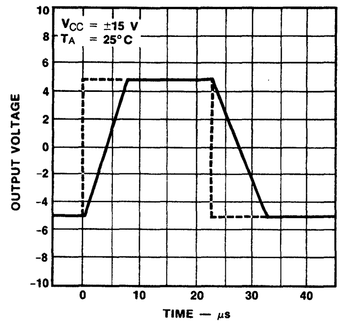
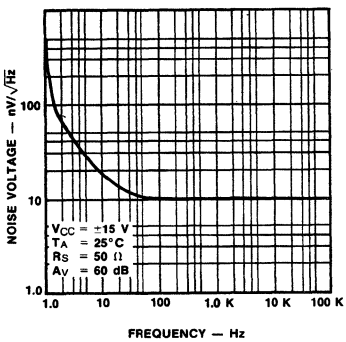
Voltage Follower Large Signal Pulse Response



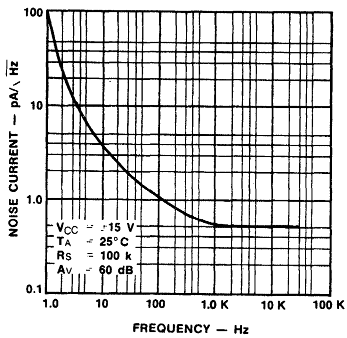
PC02760F

Input Noise Voltage vs Frequency



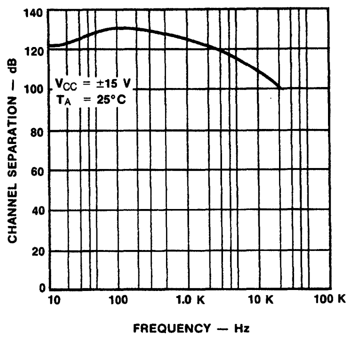
PC02771F

Input Noise Current vs Frequency



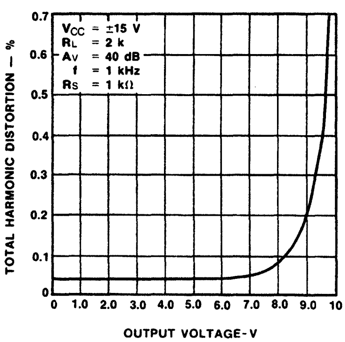
PC02781F

Channel Separation



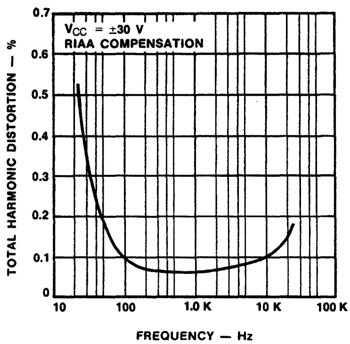
PC02791F

Distortion vs Output Voltage (f = 1 kHz)



PC02801F

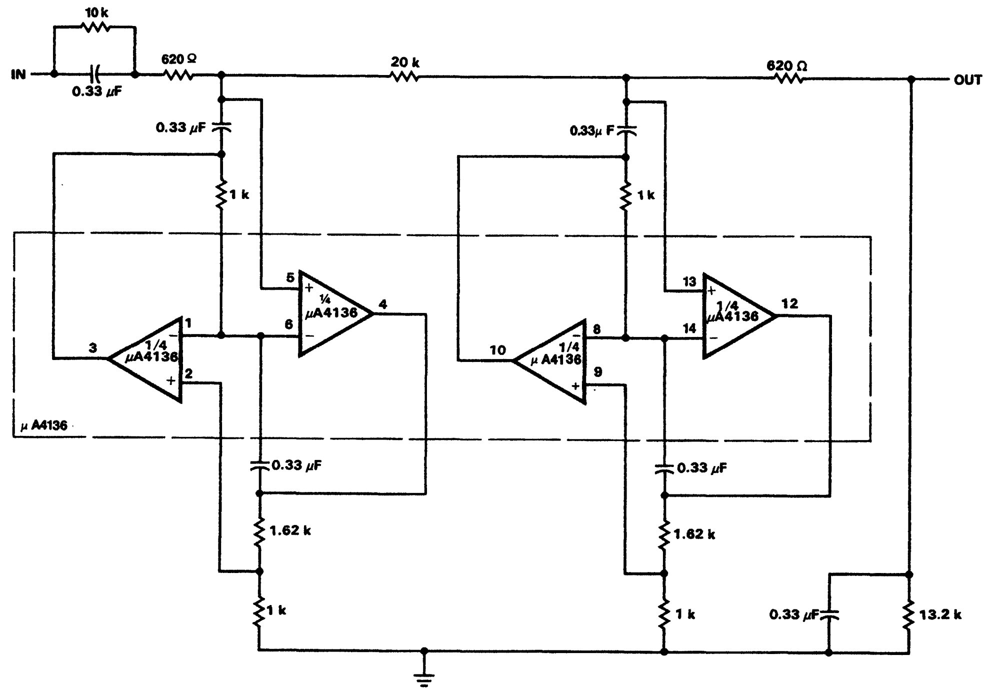
Distortion vs Frequency ($V_O = 1\ V_{rms}$)



PC02811F

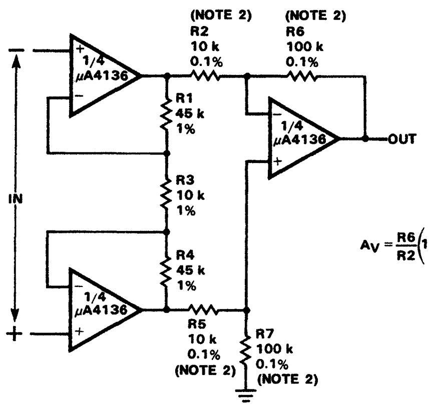
Typical Applications (Note 1)

400 Hz Lowpass Butterworth Active Filter



AF00431F

Differential Input Instrumentation Amplifier With High Common Mode Rejection



$$A_V = \frac{R6}{R2}\left(1 + \frac{2\,R1}{R3}\right)$$

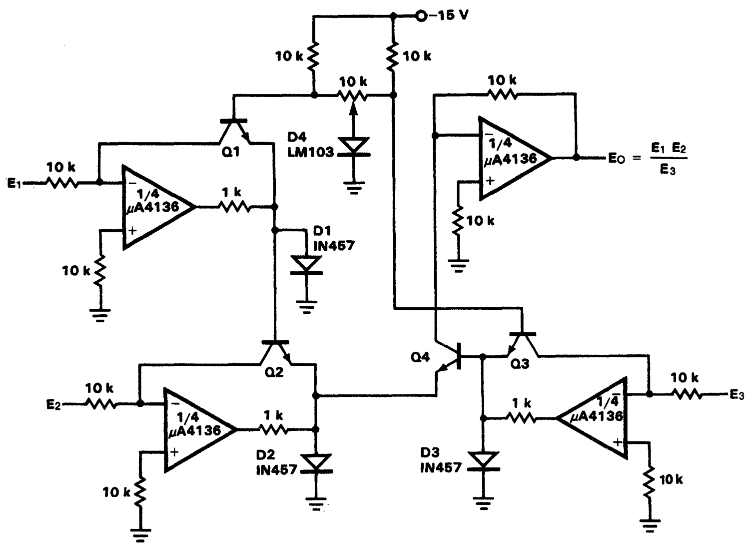
Notes

1. All resistor values are in ohms
2. Matching determines CMRR
   R1 = R4
   R2 = R5
   R6 = R7

AF00441F

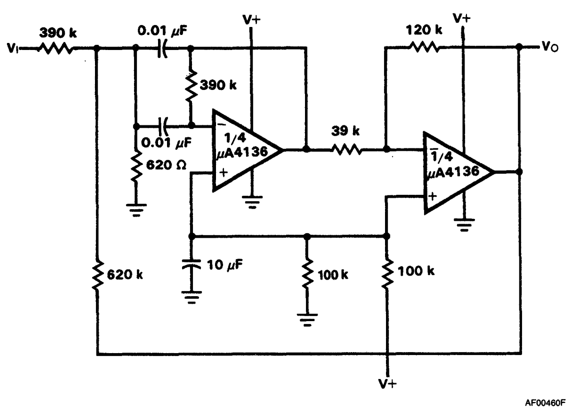
Typical Applications (Cont.) (Note 1)

Analog Multiplier/Divider



AF00451F

1 kHz Bandpass Active Filter

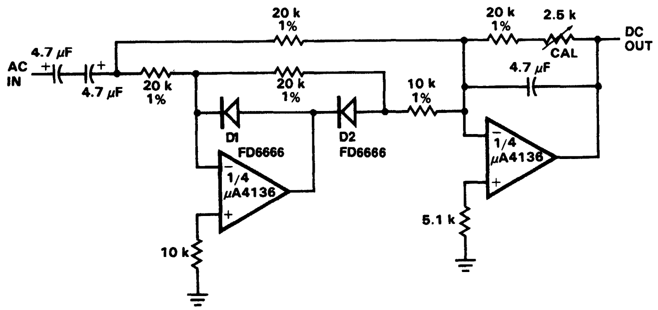


AF00460F

Note
1. All resistor values are in ohms

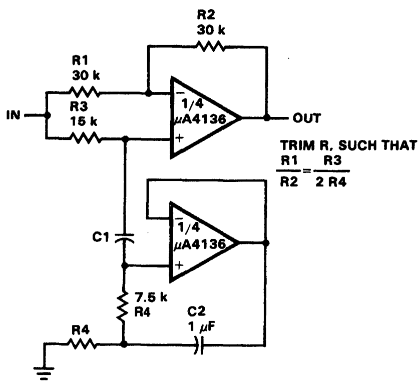
Typical Applications (Cont.) (Note 1)

Full-Wave Rectifier And Averaging Filter



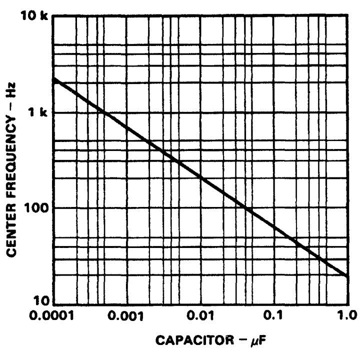
AF00471F

Notch Filter Using The μA4136 As A Gyrator



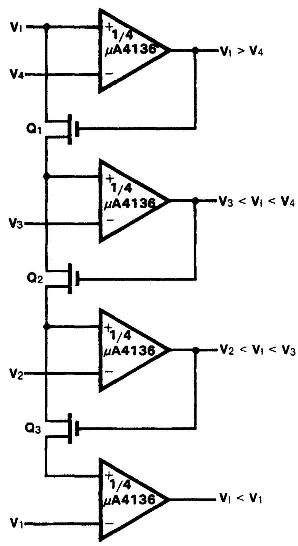
AF00481F

Notch Frequency vs Capacitor



PC02821F

Multiple Aperture Window Discriminator



AF00491F

Note

1. All resistor values are in ohms

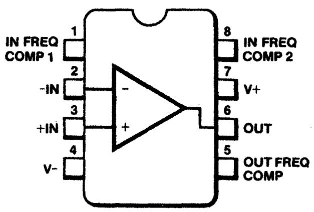
FAIRCHILD
A Schlumberger Company

μA709 High Performance Operational Amplifier

Description

The μA709 is a monolithic high gain operational amplifier constructed using the Fairchild Planar Epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in DC servo systems, high impedance analog computers, low level instrumentation applications, and for the generation of special linear and nonlinear transfer functions.

Connection Diagram 8-Lead DIP and SO-8 Package (Top View)

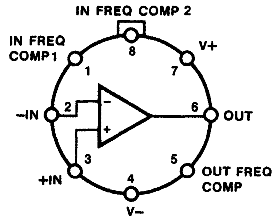


CD00731F

Order Information

Device Code	Package Code	Package Description
μA709TC	9T	Molded DIP
μA709SC	KC	Molded Surface Mount

Connection Diagram 8-Lead Metal Package (Top View)



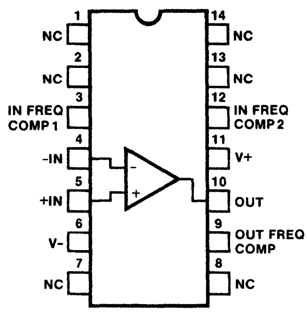
CD00721F

Lead 4 connected to case

Order Information

Device Code	Package Code	Package Description
μA709AHM	5W	Metal
μA709HM	5W	Metal
μA709HC	5W	Metal

Connection Diagram 14-Lead DIP (Top View)



CD00741F

Order Information

Device Code	Package Code	Package Description
μA709PC	9A	Molded DIP

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA709AM, μA709M)	−55°C to +125°C
Commercial (μA709C)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
14L-Molded DIP	1.04 W
Supply Voltage	±18 V
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short Circuit Duration	5.0 s

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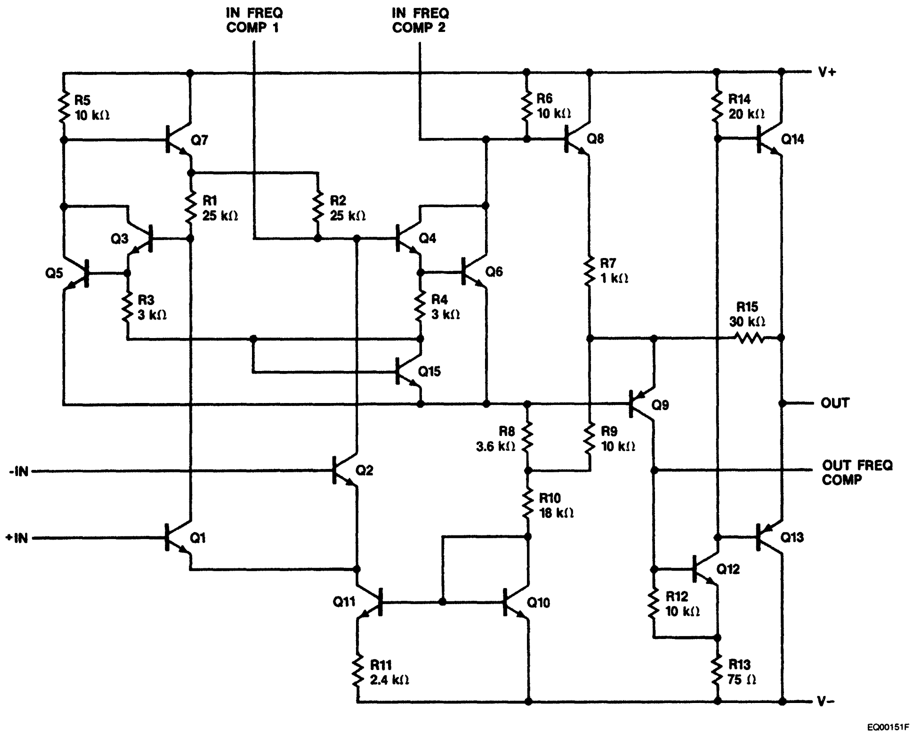
Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, the SO-8 at 6.5 mW/°C, and the 14L-Molded DIP at 8.3 mW/°C.

Equivalent Circuit



μA709A and μA709
Electrical Characteristics $T_A = 25°C$, $\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$, unless otherwise specified.

Symbol	Characteristic		Condition	μA709A Min	μA709A Typ	μA709A Max	μA709 Min	μA709 Typ	μA709 Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10\ k\Omega$		0.6	2.0		1.0	5.0	mV
I_{IO}	Input Offset Current				10	50		50	200	nA
I_{IB}	Input Bias Current				100	200		200	500	nA
Z_I	Input Impedance			350	700		150	400		kΩ
I_{CC}	Supply Current		$V_{CC} = \pm 15\ V$		2.5	3.6		2.7	5.5	mA
P_c	Power Consumption		$V_{CC} = \pm 15\ V$		75	108		80	165	mW
TR	Transient Response	Rise time	$V_{CC} = \pm 15\ V$ $V_I = 20\ mV$ $R_L = 2.0\ k\Omega$ $C1 = 5.0\ nF$ $A_V = 1.0$		0.3	1.5		0.3	1.0	μs
		Overshoot	$R2 = 50\ \Omega$ $C_L \leqslant 100\ pF$ $R1 = 1.5\ k\Omega$ $C2 = 200\ pF$ $A_V = 1.0$		10	30		10	30	%
The following specifications apply over the range of −55°C to +125°C for the μA709A and μA709.										
V_{IO}	Input Offset Voltage		$R_S \leqslant 10\ k\Omega$			3.0			6.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$R_S = 50\ \Omega$		1.8	10		3.0		μV/°C
			$R_S \leqslant 10\ k\Omega$		4.8	25		6.0		
I_{IO}	Input Offset Current		$T_A = +125°C$		3.5	50		20	200	nA
			$T_A = -55°C$		40	250		100	500	
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$T_A = +25°C$ to $+125°C$		0.08	0.5				nA/°C
			$T_A = +25°C$ to $-55°C$		0.45	2.8				
I_{IB}	Input Bias Current		$T_A = -55°C$		300	600		500	1500	nA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Sensitivity		$T_A = +125°C$		2.1	3.0				nA/°C
			$T_A = -55°C$		2.7	4.5				
Z_I	Input Impedance		$T_A = -55°C$	85	170		40	100		kΩ
CMR	Common Mode Rejection		$R_S \leqslant 10\ k\Omega$	80	110		70	90		db
V_{IR}	Input Voltage Range		$V_{CC} = \pm 15\ V$	±8.0	±10		±8.0	±10		V
PSRR	Power Supply Rejection Ratio		$R_S \leqslant 10\ k\Omega$		40	100		50	150	μV/V
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$ $R_L \geqslant 2.0\ k\Omega$ $V_O = \pm 10\ V$	25		70	25	45	70	V/mV
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$ $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
			$V_{CC} = \pm 15\ V$ $R_L = 2.0\ k\Omega$	±10	±13		±10	±13		

μA709A and μA709 (Cont.)
Electrical Characteristics $T_A = 25°C$, $\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$, unless otherwise specified.

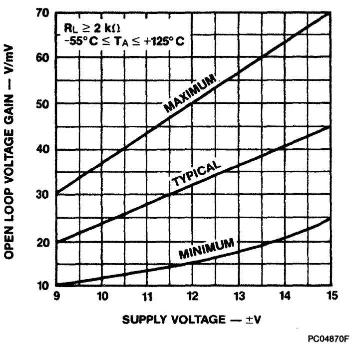
Symbol	Characteristic	Condition	μA709A Min	μA709A Typ	μA709A Max	μA709 Min	μA709 Typ	μA709 Max	Unit
I_{CC}	Supply Current	$T_A = \pm 125°C$		2.1	3.0				mA
		$T_A = -55°C$		2.7	4.5				

μA709C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15\ V$, unless otherwise specified.

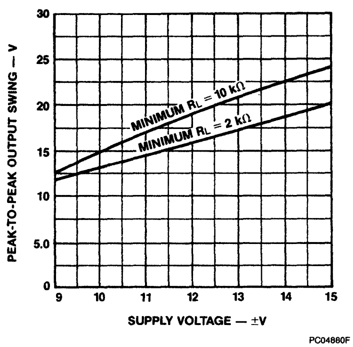
Symbol	Characteristic		Condition	μA709C Min	μA709C Typ	μA709C Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10\ k\Omega$		2.0	7.5	mV
I_{IO}	Input Offset Current				100	500	nA
I_{IB}	Input Bias Current				300	1500	nA
Z_I	Input Impedance			50	250		kΩ
I_{CC}	Supply Current		$V_{CC} = \pm 15\ V$		2.7	6.66	mA
P_c	Power Consumption		$V_{CC} = \pm 15\ V$		80	200	mW
CMR	Common Mode Rejection		$R_S \leqslant 10\ k\Omega$	65	90		dB
V_{IR}	Input Voltage Range		$V_{CC} = \pm 15\ V$	±8.0	±10		V
PSRR	Power Supply Rejection Ratio		$R_S \leqslant 10\ k\Omega$		50	200	μV/V
TR	Transient Response	Rise time	$V_{CC} = \pm 15\ V$ $V_I = 20\ mV$ $R_L = 2.0\ k\Omega$ $C1 = 5.0\ nF$ $A_V = 1.0$		0.3		μs
		Overshoot	$R2 = 50\ \Omega$ $C_L = 100\ pF$ $R1 = 1.5\ k\Omega$ $C2 = 200\ pF$ $A_V = 1.0$		10		%
The following specifications apply over the range of 0°C to +70°C.							
V_{IO}	Input Offset Voltage		$R_S \leqslant 10\ k\Omega$			10.0	mV
I_{IO}	Input Offset Current		$T_A = 0°C$			750	nA
I_{IB}	Input Bias Current		$T_A = 0°C$			2000	nA
Z_I	Input Impedance		$T_A = 0°C$	35	80		kΩ
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$ $R_L \geqslant 2.0\ k\Omega$ $V_O = \pm 10\ V$	15	45		V/mV
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$ $R_L = 10\ k\Omega$	±12	±14		V
			$V_{CC} = \pm 15\ V$ $R_L = 2.0\ k\Omega$	±10	±13		V

Typical Performance Curves for μA709A

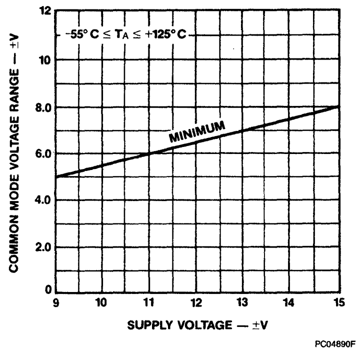
Voltage Gain vs Supply Voltage



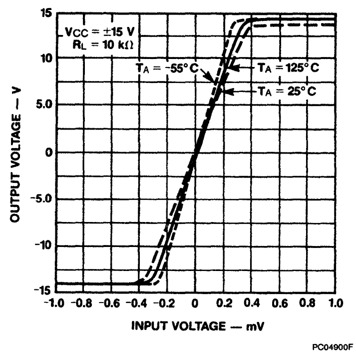
Output Voltage Swing vs Supply Voltage



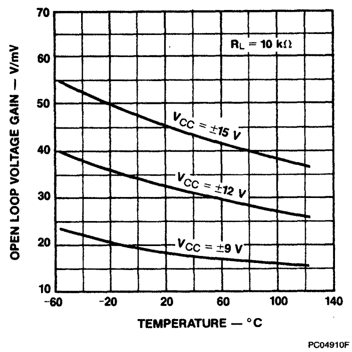
Input Common Mode Voltage Range vs Supply Voltage



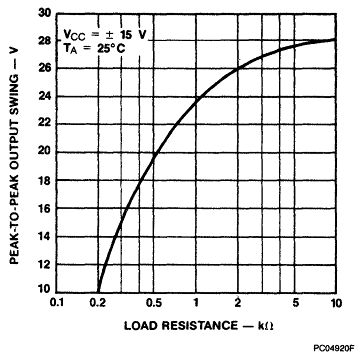
Voltage Transfer Characteristics



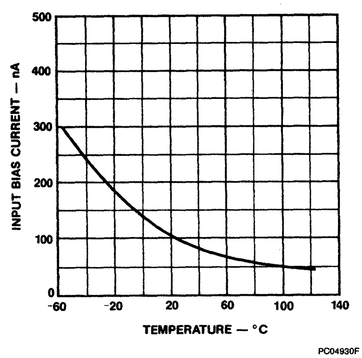
Voltage Gain vs Temperature



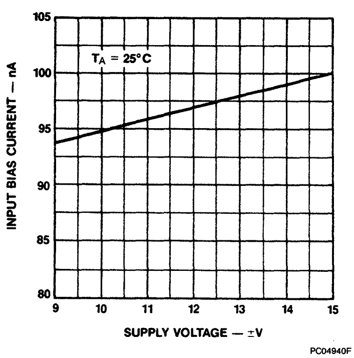
Output Voltage Swing vs Load Resistance



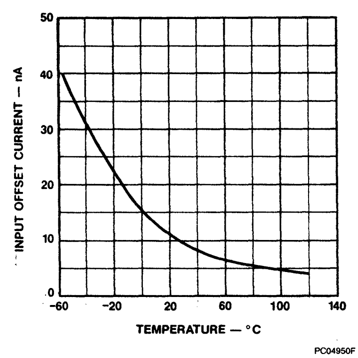
Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage

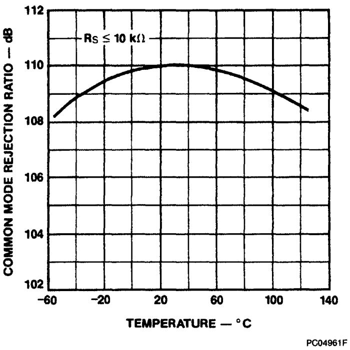


Input Offset Current vs Temperature

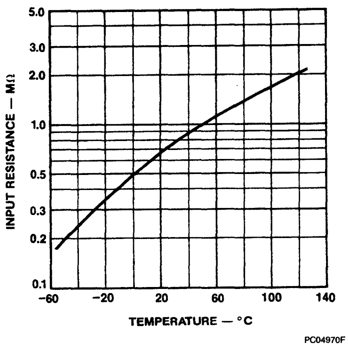


Typical Performance Curves for μA709A (Cont.)

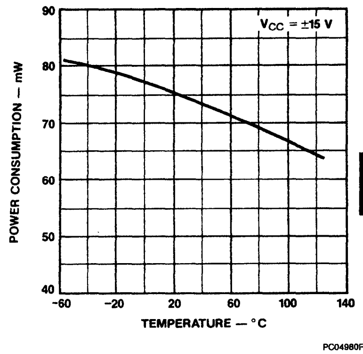
Common Mode Rejection Ratio vs Temperature



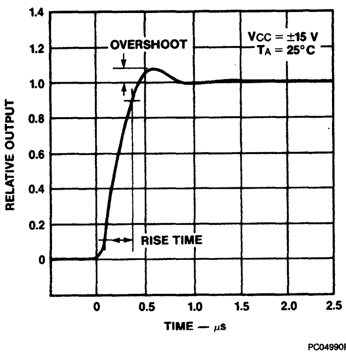
Input Resistance vs Temperature



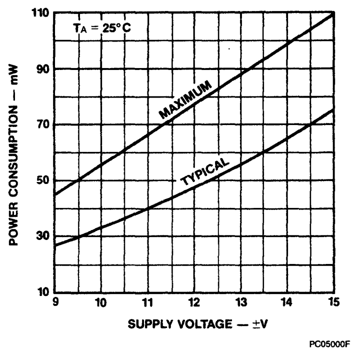
Power Consumption vs Temperature



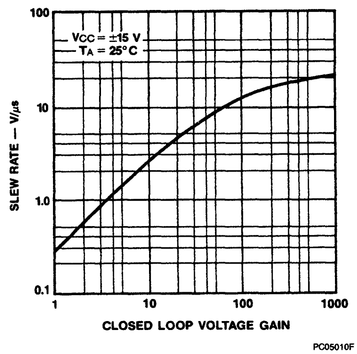
Transient Response



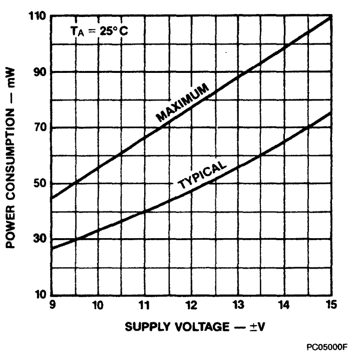
Power Consumption vs Supply Voltage



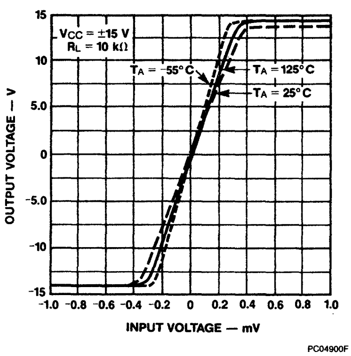
Slew Rate vs Closed Loop Gain Using Recommended Compensation Networks



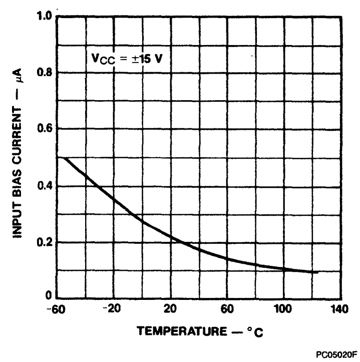
Power Consumption vs Supply Voltage (μA709 and μA709C)



Voltage Transfer Characteristics (μA709 and μA709C)



Input Bias Current vs Temperature (μA709 and μA709C)



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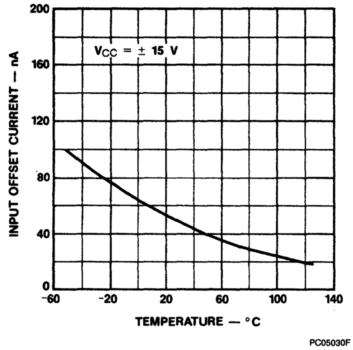
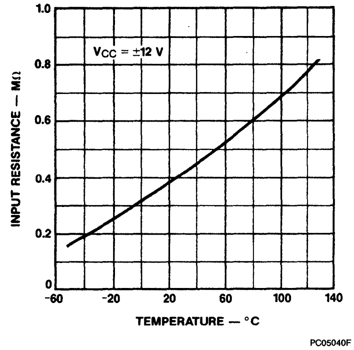
Typical Performance Curves for μA709 and μA709C (Cont.)

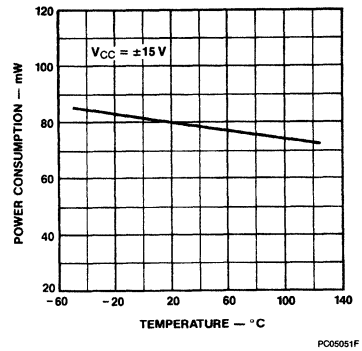
Input Offset Current vs Temperature



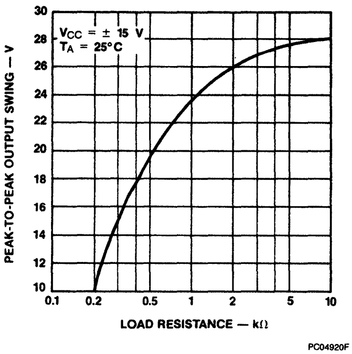
Input Resistance vs Temperature



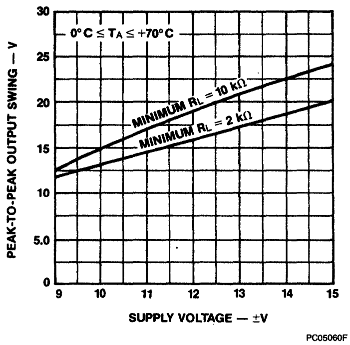
Power Consumption vs Temperature



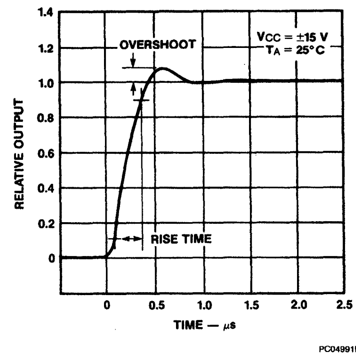
Output Voltage Swing vs Load Resistance



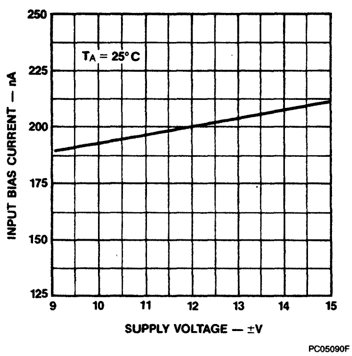
Output Voltage Swing vs Supply Voltage



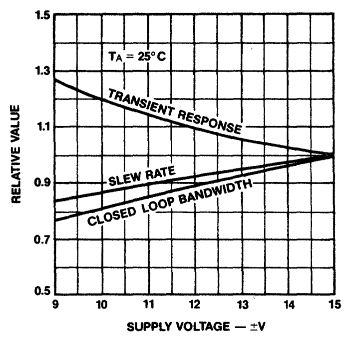
Transient Response



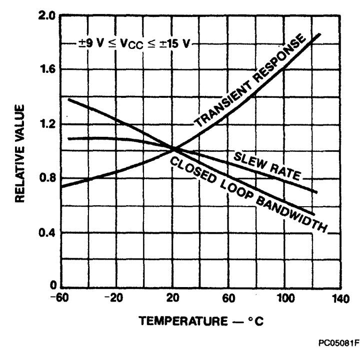
Input Bias Current vs Supply Voltage



Frequency Characteristics vs Supply Voltage

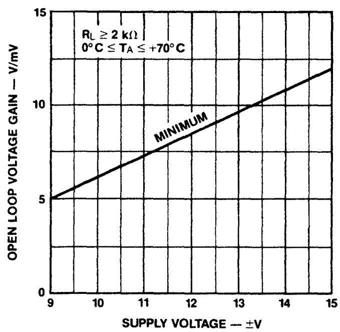


Frequency Characteristics vs Temperature



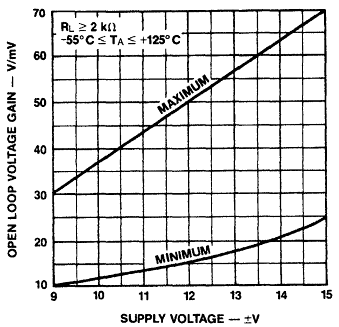
Typical Performance Curves for μA709 and μA709C (Cont.)

Voltage Gain vs Supply Voltage (μA709C)



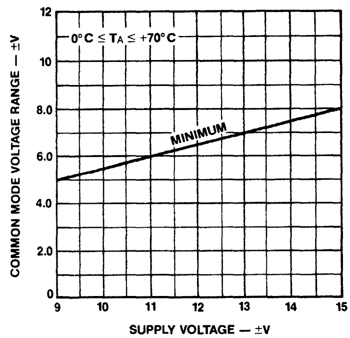
PC05100F

Voltage Gain vs Supply Voltage (μA709)



PC05110F

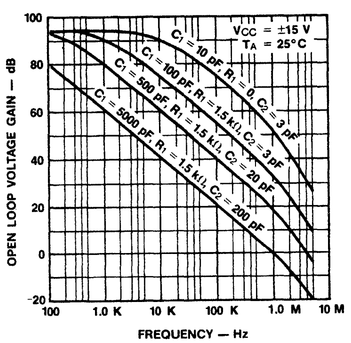
Input Common Mode Voltage Range vs Supply Voltage



PC05121F

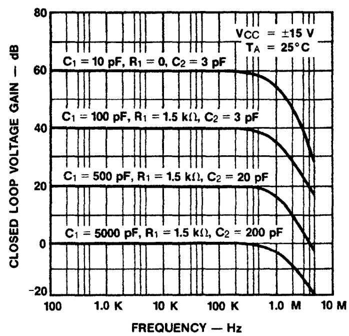
Frequency Compensation Curves For All Types

Open Loop Frequency Response For Various Values Of Compensation



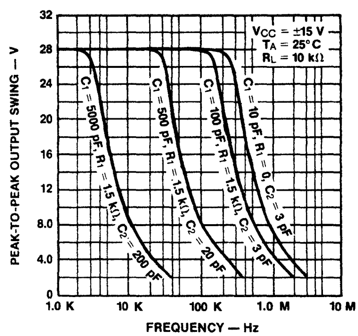
PC05131F

Frequency Response For Various Closed Loop Gains



PC05141F

Output Voltage Swing vs Frequency For Various Values Of Compensation



PC05151F

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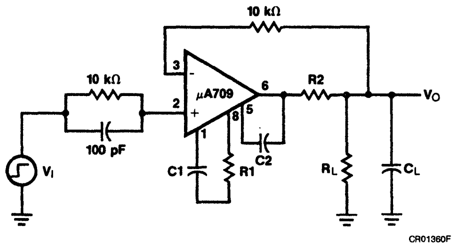
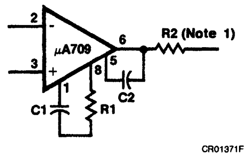
Test Circuits

Transient Response Circuit

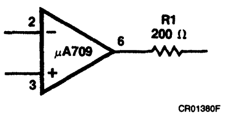


Frequency Compensation Circuit

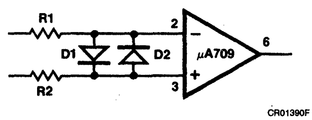


Protection Circuits

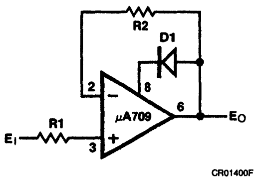
Output Short Circuit Protection



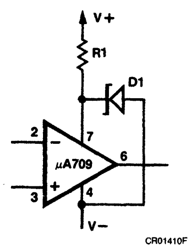
Input Breakdown Protection



Latch Up Protection



Supply Over Voltage Protection



Note

1. Use R2 = 50 Ω when the amplifier is operated with capacitive loading.

FAIRCHILD

A Schlumberger Company

µA714 Precision Operational Amplifier

Description

The µA714 is a monolithic instrumentation operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications.

- **Low Offset Voltage — 75 µV**
- **Low Offset Voltage Drift — 1.0 µV/°C Typically**
- **Low Bias Current — ± 2.6 nA**
- **Low Input Noise Current — 0.12 pA/ √Hz at 1.0 kHz Typically**
- **High Open Loop Gain — 500 K Typically**
- **Low Input Offset Current — 2.8 nA**
- **High Common Mode Rejection — 110 dB**
- **Wide Power Supply Range — ± 3.0 To ± 22 V**
- **Plug-In Replacement For Op-07**

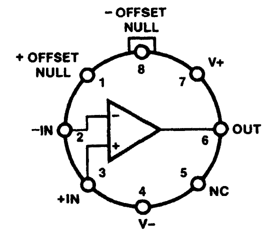
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (µA714M)	-55°C to +125°C
Commercial (µA714C, µA714EC, µA714LC)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissapation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	
µA714, µA714C, µA714E	±22 V
µA714L	±18 V
Differential Input Voltage	±30 V
Input Voltage[3]	
µA714, µA714C, µA714E	±22 V
µA714L	±18 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. For supply voltage less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 8-Lead Metal Package (Top View)

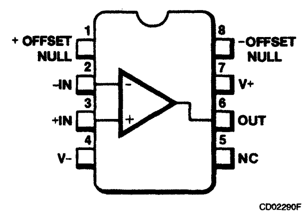


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
µA714HM	5W	Metal
µA714HC	5W	Metal
µA714EHC	5W	Metal
µA714LHC	5W	Metal

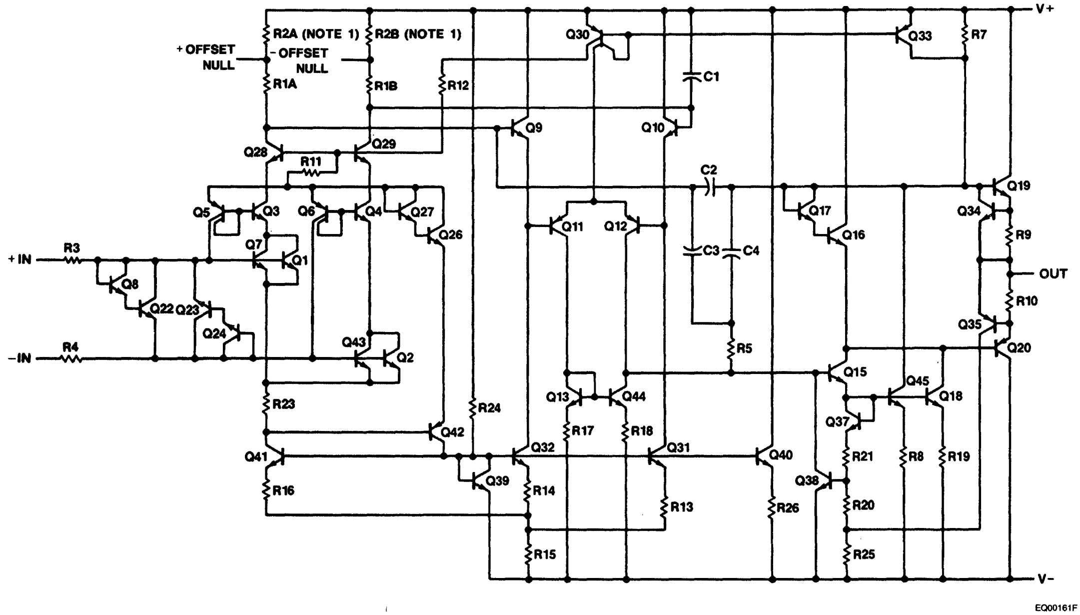
Connection Diagram 8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
µA714SC	KC	Molded Surface Mount
µA714TC	9T	Molded DIP
µA714LSC	KC	Molded Surface Mount
µA714LTC	9T	Molded DIP

Equivalent Circuit



Note

1. R2A and R2B are electronically adjusted on chip at the factory for minimum offset voltage

μA714
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		30	75	μV
S	Long Term Input Offset Voltage Stability	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.2		μV/mo
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_O = 20$ kΩ		± 4.0		mV
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		0.4	2.8	nA
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		1.0	3.0	nA
Z_I	Input Impedance		20	60		MΩ
P_c	Power Consumption	$V_O = 0$ V		75	120	mW
		$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		4.0	6.0	
CMR	Common Mode Rejection	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	110	126		dB
V_{IR}	Input Voltage Range		± 13.0	± 14.0		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 3.0$ V to ± 18 V, $R_S = 50\ \Omega$	100	110		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	200	500		V/mV
		$R_L \geqslant 500\ \Omega$, $V_O = \pm 0.5$ V, $V_{CC} = \pm 3.0$ V	150	500		
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	± 12.5	± 13.0		V
		$R_L = 2.0$ kΩ	± 12.0	± 12.8		
		$R_L = 1.0$ kΩ	± 10.5	± 12.0		
BW	Bandwidth	$A_V = 1.0$		0.6		MHz
SR	Slew Rate	$R_L = 2.0$ kΩ, $A_V = 1.0$		0.17		V/μs
e_n	Input Noise Voltage	0.1 Hz to 1.0 kHz		0.35	0.6	μVp — p
	Input Noise Voltage Density	$f_o = 10$ Hz		10.3	18.0	nV/$\sqrt{Hz}$
		$f_o = 100$ Hz		10.0	13.0	
		$f_o = 1000$ Hz		9.6	11.0	
i_n	Input Noise Current	0.1 Hz to 1.0 kHz		14		pA p — p
	Input Noise Current Density	$f_o = 10$ Hz		0.32	0.80	pA/$\sqrt{Hz}$
		$f_o = 100$ Hz		0.14	0.23	
		$f_o = 1000$ Hz		0.12	0.17	

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μA714 (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
The following specifications apply for $V_{CC} = \pm 15$ V, $-55°C \leqslant T_A \leqslant +125°C$							
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		60	200	μV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity[1]	Without External Trim	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.3	1.3	μV/°C
		With External Trim	$R_O = 20$ kΩ, $R_S = 50\ \Omega$		0.3	1.3	
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		1.2	5.6	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		8.0	50	pA/°C
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		2.0	6.0	nA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		13	50	pA/°C
CMR	Common Mode Rejection		$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	106	123		dB
V_{IR}	Input Voltage Range			±13.0	±13.5		V
PSRR	Power Supply Rejection Ratio		$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	94	106		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	150	400		V/mV
V_{OP}	Output Voltage Swing		$R_L = 2.0$ kΩ	±12.0	±12.6		V

μA714E
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		30	75	μV
S	Long Term Input Offset Voltage Stability	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.3		μV/mo
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_O = 20$ kΩ		±4.0		mV
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		0.5	3.8	nA
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		1.2	4.0	nA
Z_I	Input Impedance		15	50		MΩ
P_c	Power Consumption	$V_O = 0$ V		75	120	mW
		$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		4.0	6.0	
CMR	Common Mode Rejection	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	106	123		dB

μ**A714E** (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IR}	Input Voltage Range		±13.0	±14.0		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	94	107		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	200	500		V/mV
		$R_L \geq 500\ \Omega$, $V_O = \pm 0.5$ V $V_{CC} = \pm 3.0$ V	150	500		
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.5	±13.0		V
		$R_L = 2.0$ kΩ	±12.0	±12.8		
		$R_L = 1.0$ kΩ	±10.5	±12.0		
BW	Bandwidth	$A_V = 1.0$		0.6		MHz
SR	Slew Rate	$R_L = 2.0$ kΩ, $A_V = 1.0$		0.17		V/μs
e_n	Input Noise Voltage[1]	0.1 Hz to 1.0 kHz		0.35	0.6	μV p—p
	Input Noise Voltage Density[1]	$f_o = 10$ Hz		10.3	18.0	nV/√Hz
		$f_o = 100$ Hz		10.0	13.0	
		$f_o = 1000$ Hz		9.6	11.0	
i_n	Input Noise Current[1]	0.1 Hz to 1.0 kHz		14	30	pA p—p
	Input Noise Current Density[1]	$f_o = 10$ Hz		0.32	0.80	pA/√Hz
		$f_o = 100$ Hz		0.14	0.23	
		$f_o = 1000$ Hz		0.12	0.17	

The following specifications apply for $V_{CC} = \pm 15$ V, $0°C \leq T_A \leq 70°C$

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		45	130	μV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity[1]	Without External Trim	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.3	1.3	μV/°C
		With External Trim	$R_O = 20$ kΩ, $R_S = 50\ \Omega$		0.3	1.3	
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		0.9	5.3	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		8.0	35	pA/°C
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		1.5	5.5	nA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		13	35	pA/°C
CMR	Common Mode Rejection		$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	103	123		dB

μA714E (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IR}	Input Voltage Range		±13.0	±13.5		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	90	104		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	180	450		V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±12.0	±12.6		V

μA714C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		60	150	μV
S	Long Term Input Offset Voltage Stability	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.4	2.0	μV/mo
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_O = 20$ kΩ		±4.0		mV
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		0.8	6.0	nA
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		1.8	7.0	nA
Z_I	Input Impedance		8.0	33		MΩ
P_c	Power Consumption	$V_O = 0$ V		80	150	mW
		$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		4.0	8.0	
CMR	Common Mode Rejection	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	100	120		dB
V_{IR}	Input Voltage Range		±13.0	±14.0		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	90	104		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	120	400		V/mV
		$R_L \geqslant 500\ \Omega$, $V_O = \pm 0.5$ V, $V_{CC} = \pm 3.0$ V	100	400		
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.0	±13.0		V
		$R_L = 2.0$ kΩ	±11.5	±12.8		
		$R_L = 1.0$ kΩ		±12.0		
BW	Bandwidth	$A_V = 1.0$		0.6		MHz
SR	Slew Rate	$R_L = 2.0$ kΩ, $A_V = 1.0$		0.17		V/μs

μA714C (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 15$ V

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
e_n	Input Noise Voltage[1]		0.1 Hz to 1.0 kHz		0.38	0.65	μVp — p
	Input Noise Voltage Density[1]		$f_o = 10$ Hz		10.5	20.0	nV/√Hz
			$f_o = 100$ Hz		10.2	13.5	
			$f_o = 1000$ Hz		9.8	11.5	
i_n	Input Noise Current[1]		0.1 Hz to 1.0 kHz		0.15	35	μVp — p
	Input Noise Current Density[1]		$f_o = 10$ Hz		0.35	0.90	pA/√Hz
			$f_o = 100$ Hz		0.15	0.27	
			$f_o = 1000$ Hz		0.13	0.18	

The following specifications apply for $V_{CC} = \pm 15$ V, $0°C \leq T_A \leq 70°C$

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		85	250	μV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity[1]	Without External Trim	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.5	1.8	μV/°C
		With External Trim	$R_O = 20$ kΩ, $R_S = 50\ \Omega$		0.4	1.6	
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		1.6	8.0	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		12	50	pA/°C
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		2.2	9.0	nA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		18	50	pA/°C
CMR	Common Mode Rejection		$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	97	120		dB
V_{IR}	Input Voltage Range			±13.0	±13.5		V
PSRR	Power Supply Rejection Ratio		$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	86	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	100	400		V/mV
V_{OP}	Output Voltage Swing		$R_L = 2.0$ kΩ	±11.0	±12.6		V

μA714L
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		100	250	μV
S	Long Term Input Offset Voltage Stability	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.5	3.0	μV/mo
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_O = 20$ kΩ		±4.0		mV
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		5.0	20	nA
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		6.0	30	nA
Z_I	Input Impedance		8.0	33		MΩ
P_c	Power Consumption	$V_O = 0$ V		100	180	mW
		$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		5.0	12	
CMR	Common Mode Rejection	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	100	120		dB
V_{IR}	Input Voltage Range		±13.0	±14.0		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	90	104		dB
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	100	300		V/mV
		$R_L \geqslant 500\ \Omega$, $V_O = \pm 0.5$ V, $V_{CC} = \pm 3.0$ V	50	150		
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.0	±13.0		V
		$R_L = 2.0$ kΩ	±11.0	±12.8		
		$R_L = 1.0$ kΩ		±12.0		
BW	Bandwidth	$A_V = 1.0$		0.6		MHz
SR	Slew Rate	$R_L = 2.0$ kΩ, $A_V = 1.0$		0.17		V/μs
e_n	Input Noise Voltage[1]	0.1 Hz to 1.0 kHz		0.5		μV p—p
	Input Noise Voltage Density[1]	$f_o = 10$ Hz		10.5		$nV/\sqrt{Hz}$
		$f_o = 100$ Hz		10.2		
		$f_o = 1000$ Hz		9.8		
i_n	Input Noise Current[1]	0.1 Hz to 1.0 kHz		0.15		pA p—p
	Input Noise Current Density[1]	$f_o = 10$ Hz		0.35		$pA/\sqrt{Hz}$
		$f_o = 100$ Hz		0.15		
		$f_o = 1000$ Hz		0.13		

μA714L (Cont.)

Electrical Characteristics $0°C \leqslant T_A \leqslant +70°C$, $V_{CC} = \pm 15$ V

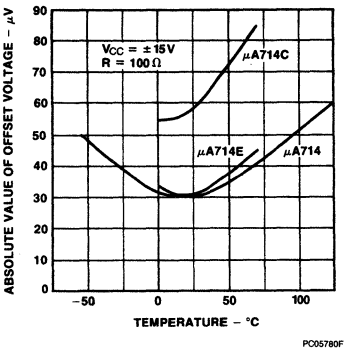
Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S = \Omega$, $V_{CM} = 0$ V			400	μV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity[1]	Without External Trim	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		1.0	3.0	μV/°C
		With External Trim	$R_O = 20$ kΩ, $R_S = 50\ \Omega$		1.3		
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		8.0	40	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		20	100	pA/°C
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		15	60	nA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Sensitivity[1]		$V_{CM} = 0$ V		35	150	pA/°C
CMR	Common Mode Rejection		$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	94	120		dB
V_{IR}	Input Voltage Range			±13.0	±13.5		V
PSRR	Power Supply Rejection Ratio		$V_{CC} = \pm 3.0$ V to ±18 V, $R_S = 50\ \Omega$	83	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	80	400		V/mV
V_{OP}	Output Voltage Swing		$R_L = 2.0$ kΩ	±10.0	±12.6		V

Note

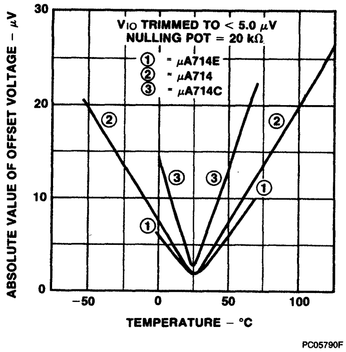
1. Parameter is not 100% tested; 90% of the units meet this specification.

Typical Performance Curves

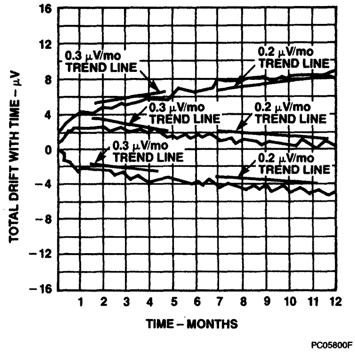
Untrimmed Offset Voltage vs Temperature



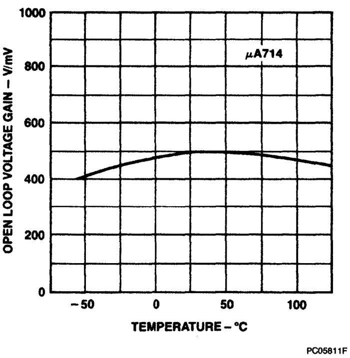
Trimmed Offset Voltage vs Temperature



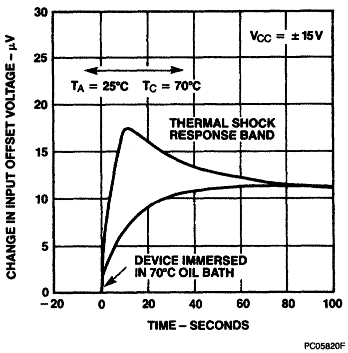
Offset Voltage Stability vs Time



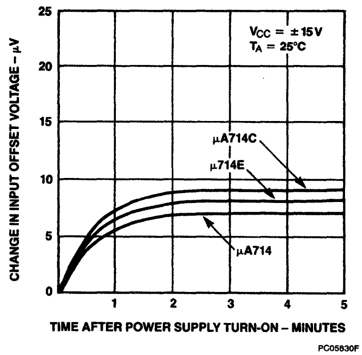
Voltage Gain vs Temperature



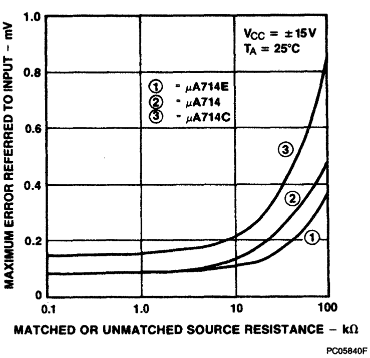
Offset Voltage Change Due to Thermal Shock



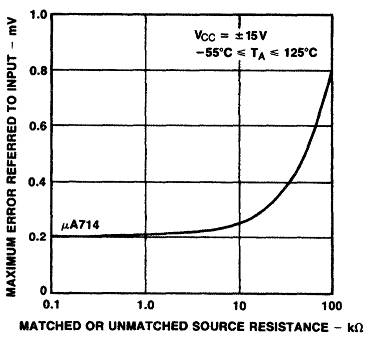
Warm-Up Drift



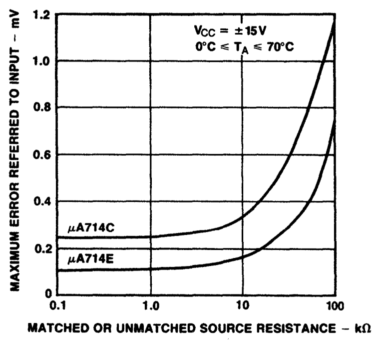
Maximum Error vs Source Resistance



Maximum Error vs Source Resistance

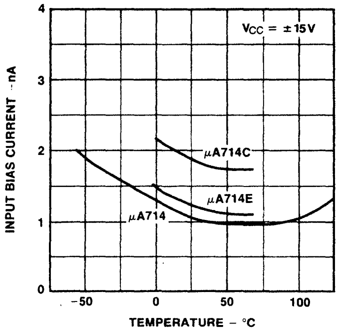


Maximum Error vs Source Resistance



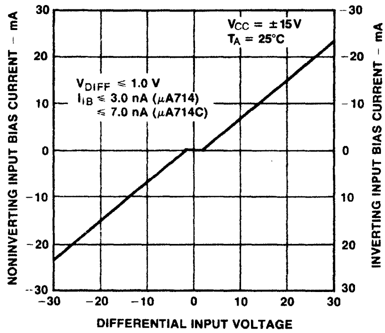
Typical Performance Curves (Cont.)

Input Bias Current vs Temperature



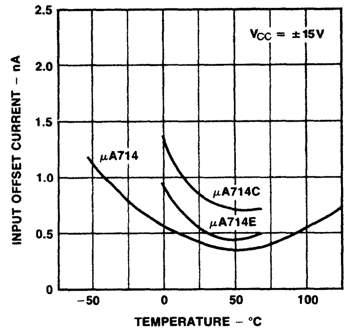
PC05870F

Input Bias Current vs Differential Input Voltage



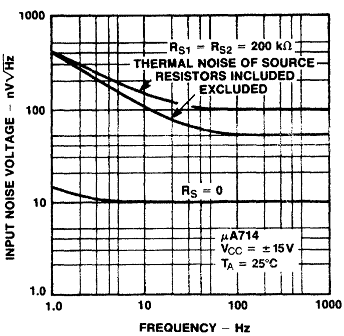
PC05891F

Input Offset Current vs Temperature



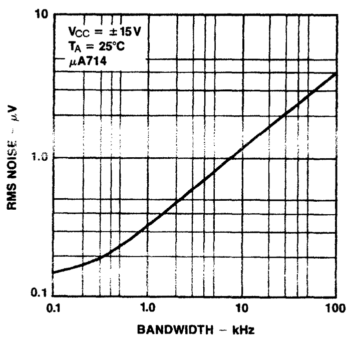
PC05880F

Input Noise Voltage vs Frequency



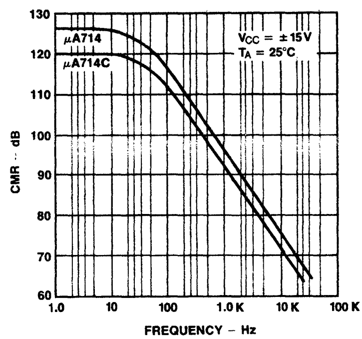
PC05901F

Input Wideband Noise vs Bandwidth (0.1 Hz to Frequency Indicated)



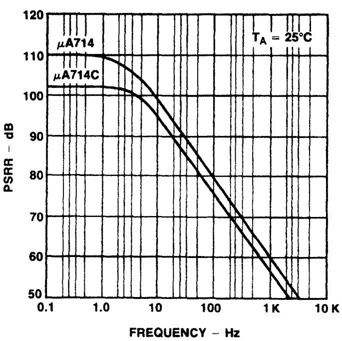
PC05911F

CMR vs Frequency



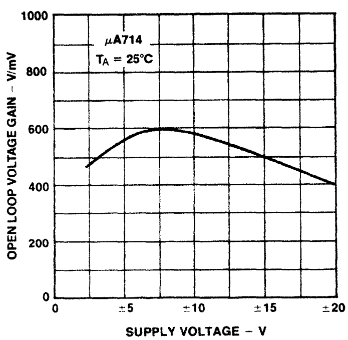
PC05921F

PSRR vs Frequency



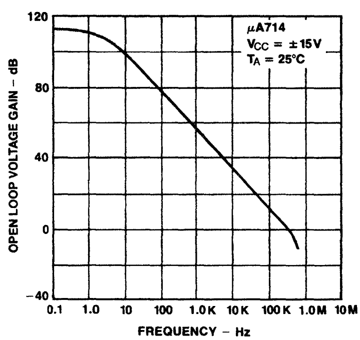
PC05931F

Voltage Gain vs Supply Voltage



PC05941F

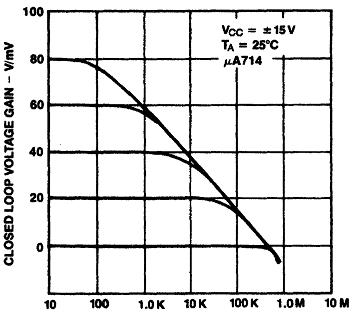
Open Loop Frequency Response



PC05951F

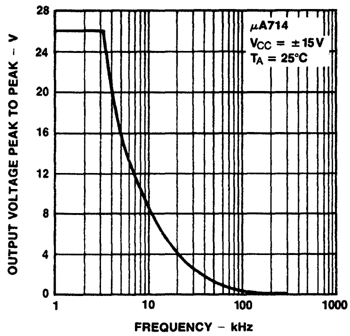
Typical Performance Curves (Cont.)

Frequency Response For Various Closed Loop Gains



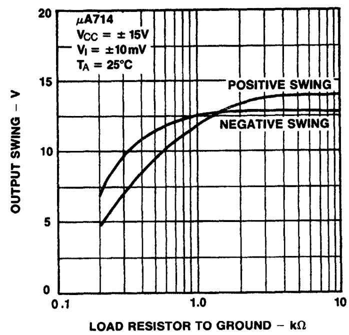
PC05961F

Maximum Undistorted Output vs Frequency



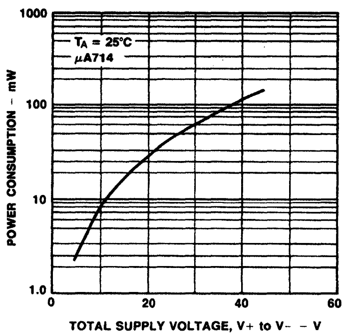
PC05971F

Output Voltage vs Load Resistance



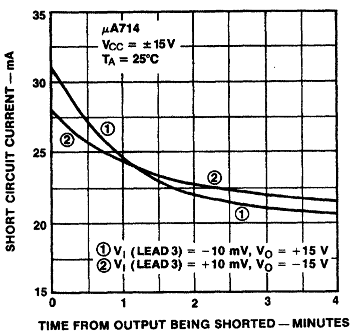
PC05981F

Power Consumption vs Supply Voltage



PC05991F

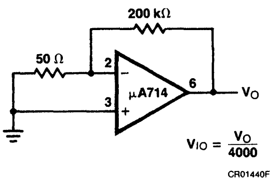
Short Circuit Current vs Time



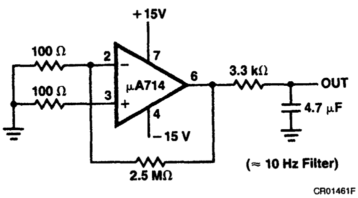
PC06001F

Test Circuits

Offset Voltage Test Circuit

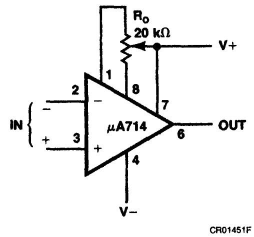


Low Frequency Noise Test Circuit



Input Referred Noise = $\frac{V_O}{25{,}000}$

Optional Offset Nulling Circuit



FAIRCHILD

A Schlumberger Company

μA715 High Speed Operational Amplifier

Linear Division Operational Amplifiers

Description

The μA715 is a high speed, high gain, monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A/D and D/A converters, active filters, deflection amplifiers, video amplifiers, phase-locked loops, multiplexed analog gates, precision comparators, sample-and-holds, and general feedback applications requiring DC wide bandwidth operation.

- **High Slew Rate — 100 V/μs (Inverting, $A_V = 1$) Typically**
- **Fast Settling Time — 800 ns Typically**
- **Wide Bandwidth — 65 MHz Typically**
- **Wide Operating Supply Range**
- **Wide Input Voltage Ranges**

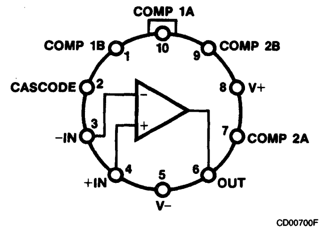
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	
Extended (μA715M)	-55°C to +125°C
Commercial (μA715C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
14L-Ceramic DIP	1.36 W
Supply Voltage	±18 V
Differential Input Voltage	±15 V
Input Voltage[3]	±15 V

Notes

1. $T_{J\ Max}$ = 175°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, and the 14L-Ceramic DIP at 9.1 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 10-Lead Metal Package (Top View)

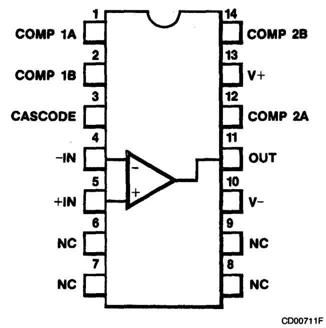


Lead 5 connected to case.

Order Information

Device Code	Package Code	Package Description
μA715HM	5X	Metal
μA715HC	5X	Metal

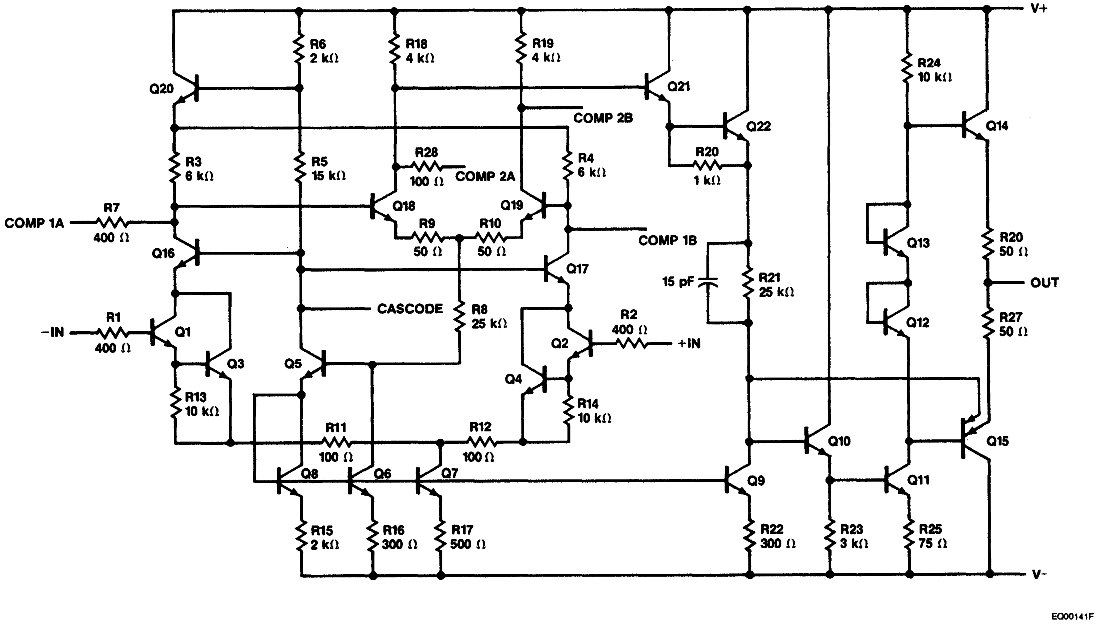
Connection Diagram 14-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA715DM	6A	Ceramic DIP
μA715DC	6A	Ceramic DIP

Equivalent Circuit



7

μA715 and μA715C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	μA715 Min	μA715 Typ	μA715 Max	μA715C Min	μA715C Typ	μA715C Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		2.0	5.0		2.0	7.5	mV
I_{IO}	Input Offset Current				70	250		70	250	nA
I_{IB}	Input Bias Current				400	750		400	1500	nA
Z_I	Input Impedance				1.0			1.0		MΩ
R_O	Output Resistance				75			75		Ω
I_{CC}	Supply Current				5.5	7.0		5.5	10	mA
P_c	Power Consumption				165	210		165	300	mW
V_{IR}	Input Voltage Range			± 10	± 12		± 10	± 12		V
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	15	30		10	30		V/mV
V	Settling Time		$V_O = \pm 5.0$ V, $A_V = 1.0$		800			800		ns
TR	Transient Response	Rise time	$V_I = 400$ mV, $A_V = 1.0$		30	60		30	75	ns
		Overshoot			25	40		25	50	%
SR	Slew Rate		$A_V = 100$		70			70		V/μs
			$A_V = 10$		38			38		
			$A_V = 1.0$ (non-inverting)	15	18		10	18		
			$A_V = 1.0$ (inverting)		100			100		

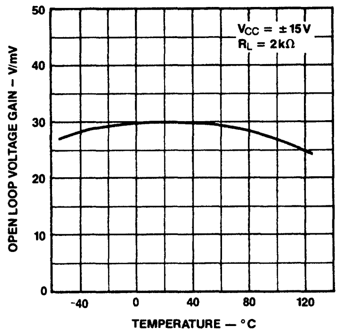
The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$ for the μA715, and $0°C \leqslant T_A \leqslant +70°C$ for the μA715C.

Symbol	Characteristic	Condition	μA715 Min	μA715 Typ	μA715 Max	μA715C Min	μA715C Typ	μA715C Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 10$ kΩ			7.5			10	mV
I_{IO}	Input Offset Current	$T_A = T_{A\ Max}$			250			250	nA
		$T_A = T_{A\ Min}$			800			750	
I_{IB}	Input Bias Current	$T_A = T_{A\ Max}$			750			1500	nA
		$T_A = T_{A\ Min}$			4.0			7.5	
CMR	Common Mode Rejection	$R_S \leqslant 10$ kΩ	74	92		74[1]	92[1]		db
PSRR	Power Supply Rejection Ratio	$R_S \leqslant 10$ kΩ		45	300		45[1]	400[1]	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	10			8			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	± 10	± 13		± 10	± 13		V

Note
1. $T_A = 25°C$ only.

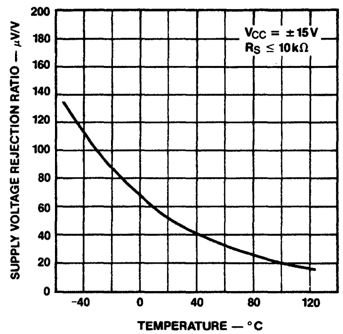
Typical Performance Curves for μA715 and μA715C

Voltage Gain vs Temperature (μA715)



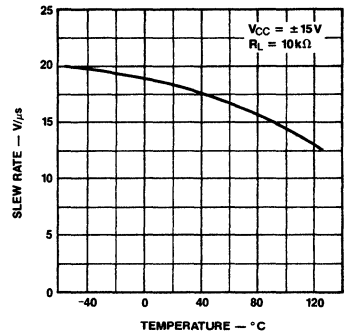
PC04600F

Supply Voltage Rejection Ratio vs Temperature (μA715)



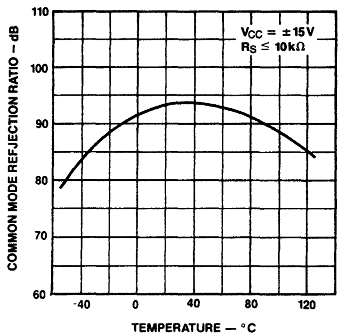
PC04610F

Slew Rate vs Temperature (μA715)



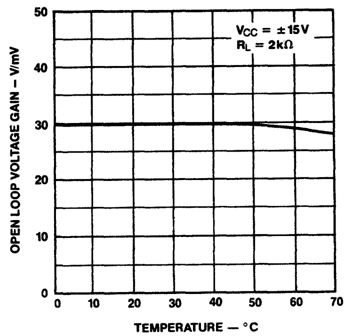
PC04620F

Common Mode Rejection Ratio vs Temperature (μA715)



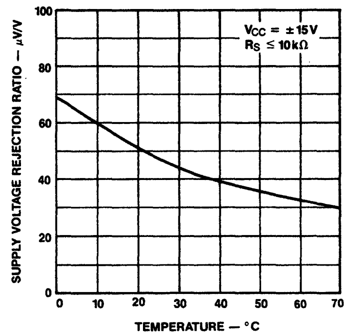
PC04630F

Voltage Gain vs Temperature (μA715C)



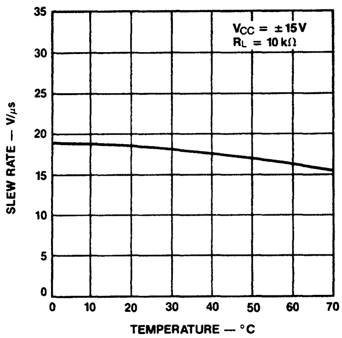
PC04640F

Supply Voltage Rejection Ratio vs Temperature (μA715C)



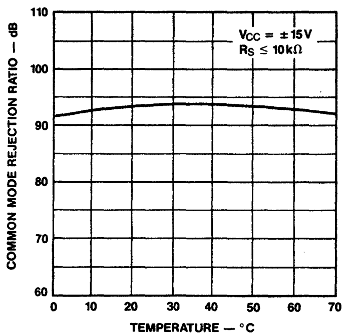
PC04650F

Slew Rate vs Temperature (μA715C)



PC04660F

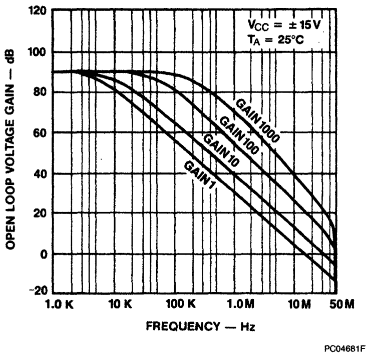
Common Mode Rejection Ratio vs Temperature (μA715C)



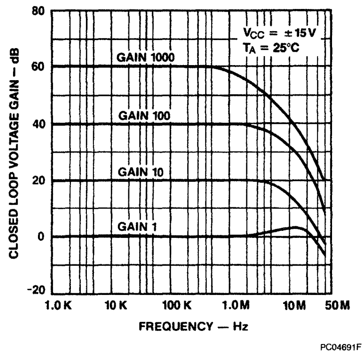
PC04670F

Typical Performance Curves for μA715 and μA715C

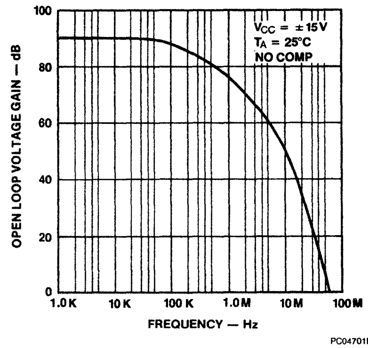
Frequency Response For Open Loop Gains (Note 1)



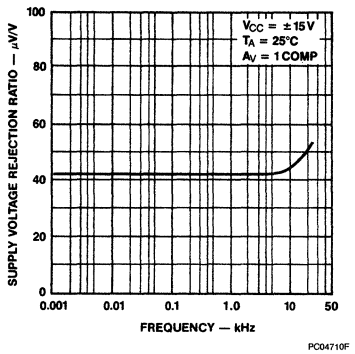
Frequency Response for Closed Loop Gains



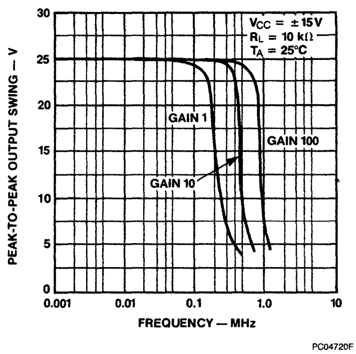
Voltage Gain vs Frequency



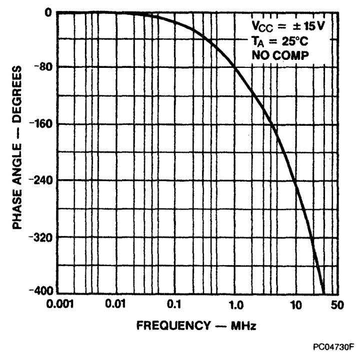
Supply Voltage Rejection Ratio vs Frequency



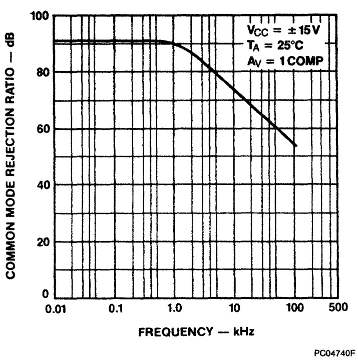
Output Swing vs Frequency for Closed Loop Gains



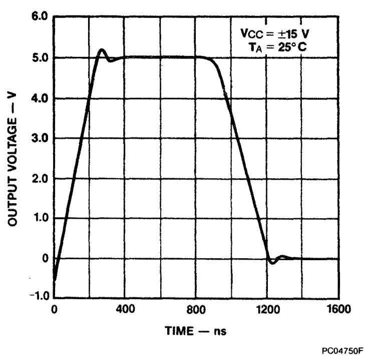
Open Loop Phase vs Frequency



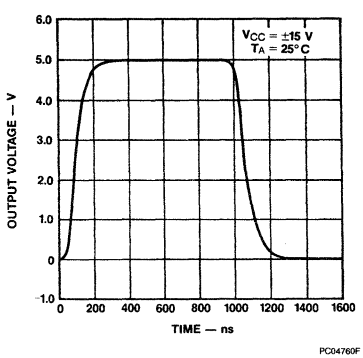
Common Mode Rejection Ratio vs Frequency



Unity Gain Large Signal Pulse Response



Large Signal Pulse Response for Gain 10

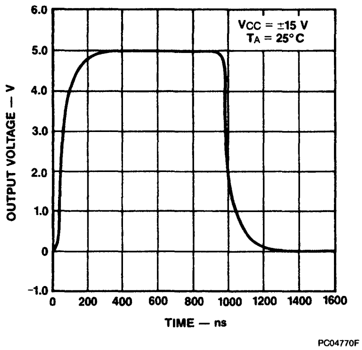


Note

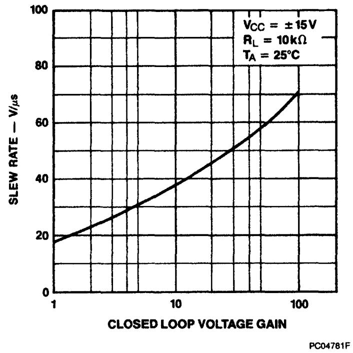
1. See "Non-Inverting Compensation Components Value Table" for Closed Loop Gain values.

Typical Performance Curves for μA715 and μA715C (Cont.)

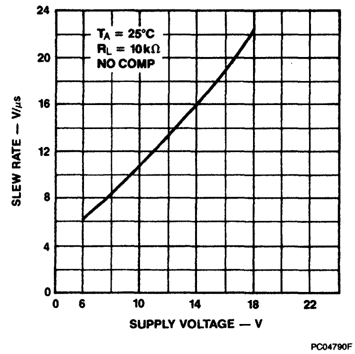
Large Signal Pulse Response for Gain 100



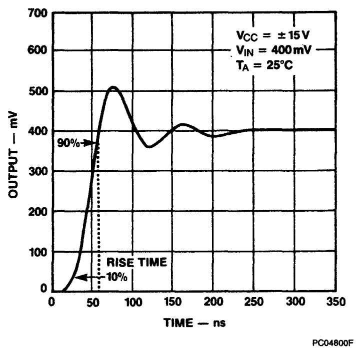
Slew Rate vs Closed Loop Voltage Gain



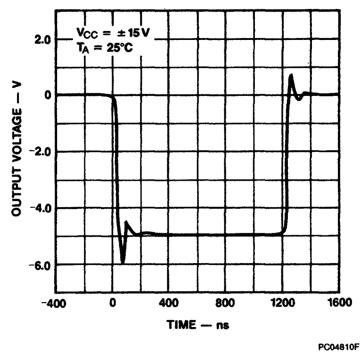
Slew Rate vs Supply Voltage



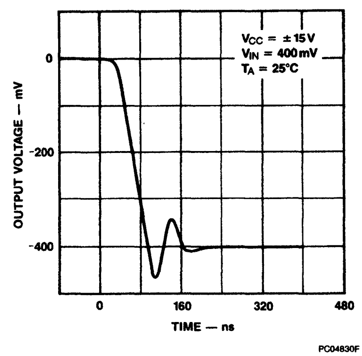
Voltage Follower Transient Response



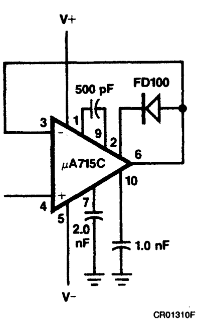
Inverting Unity Gain Large Signal Pulse Response



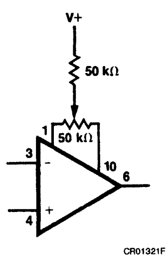
Small Signal Pulse Response Inverting Unity Gain



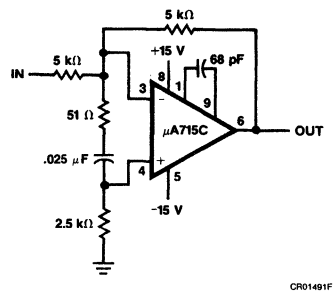
Voltage Follower (Note 1)



Voltage Offset Null Circuit (Note 1)



High Slew Rate Circuit (Note 1)



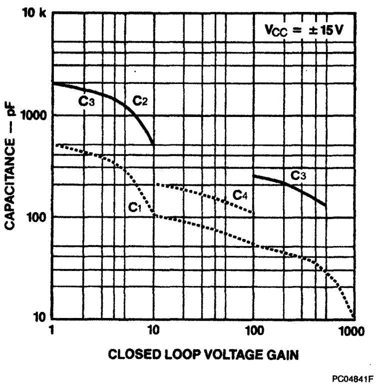
Note
1. Lead numbers apply to metal package.

Non-Inverting Compensation Components Values

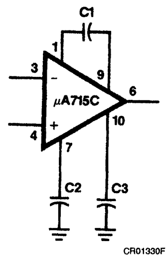
Closed Loop Gain	C1	C2	C3
1000	10 pF		
100	50 pF		250 pF
10 (Note)	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

Note
For gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Lead 7 and 10.

Suggested Values of Compensation Capacitors vs Closed Loop Voltage Gain



Frequency Compensation Circuit



Note
Lead numbers apply to metal package.

Layout Instructions

Layout — The layout should be such that stray capacitance is minimal.

Supplies — The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

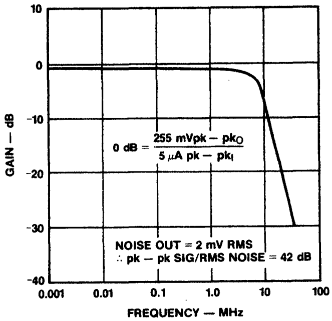
Ringing — Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω.

Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

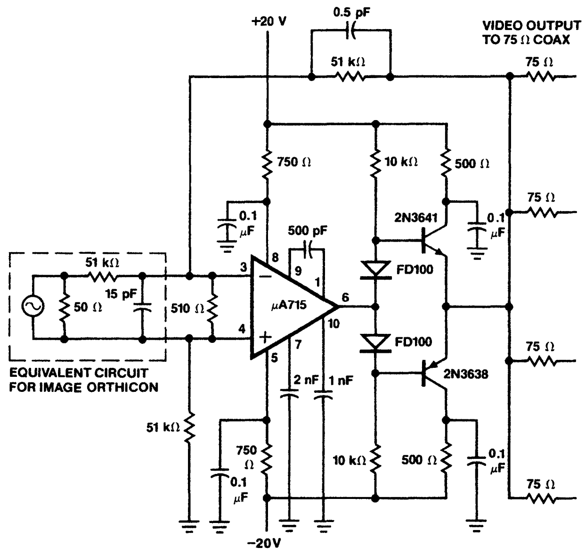
Latch Up — This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between leads 6 and 2 with the cathode toward lead 2 is the recommended preventive measure.

Typical Applications

Wide Bank Video Amplifier Drive Capability With 75 Ω Coax Cable

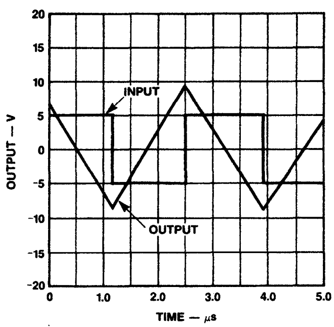


PC04850F

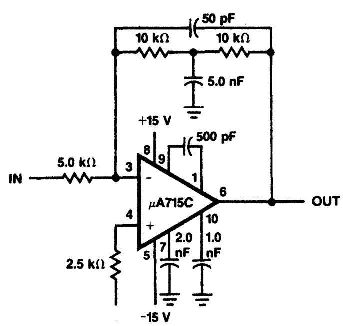


CR05740F

High Speed Integrator



PC04860F



CR01351F

Note
All lead numbers shown refer to metal package.

FAIRCHILD

A Schlumberger Company

μA725 Instrumentation Operational Amplifier

Description

The μA725 is a monolithic instrumentation operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift, and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is lead compatible with the popular μA741 operational amplifier.

- **Low Input Noise Current — 0.15 pA/√Hz At 1.0 kHz Typically**
- **High Open Loop Gain — 3,000,000 Typically**
- **Low Input Offset Current — 2.0 nA Typically**
- **Low Input Voltage Drift — 0.6 μV/°C Typically**
- **High Common Mode Rejection — 120 dB**
- **High Input Voltage Range — ± 14 V Typically**
- **Wide Power Supply Range — ± 3.0 V To ± 22 V**
- **Offset Null Capability**

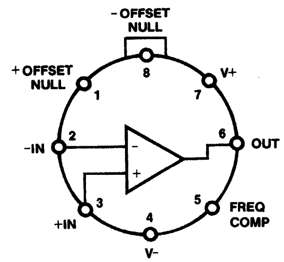
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA725AM, μA725M)	-55°C to +125°C
Commercial (μA725EC, μA725C)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
Supply Voltage	± 22 V
Differential Input Voltage	± 5.0 V
Input Voltage[3]	± 22 V
Voltage Between Offset Null and V+	± 0.5 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
3. For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 8-Lead Metal Package (Top View)

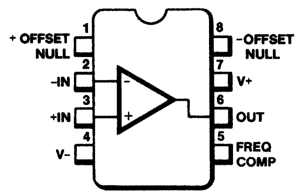


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA725HM	5W	Metal
μA725HC	5W	Metal
μA725AHM	5W	Metal
μA725EHC	5W	Metal

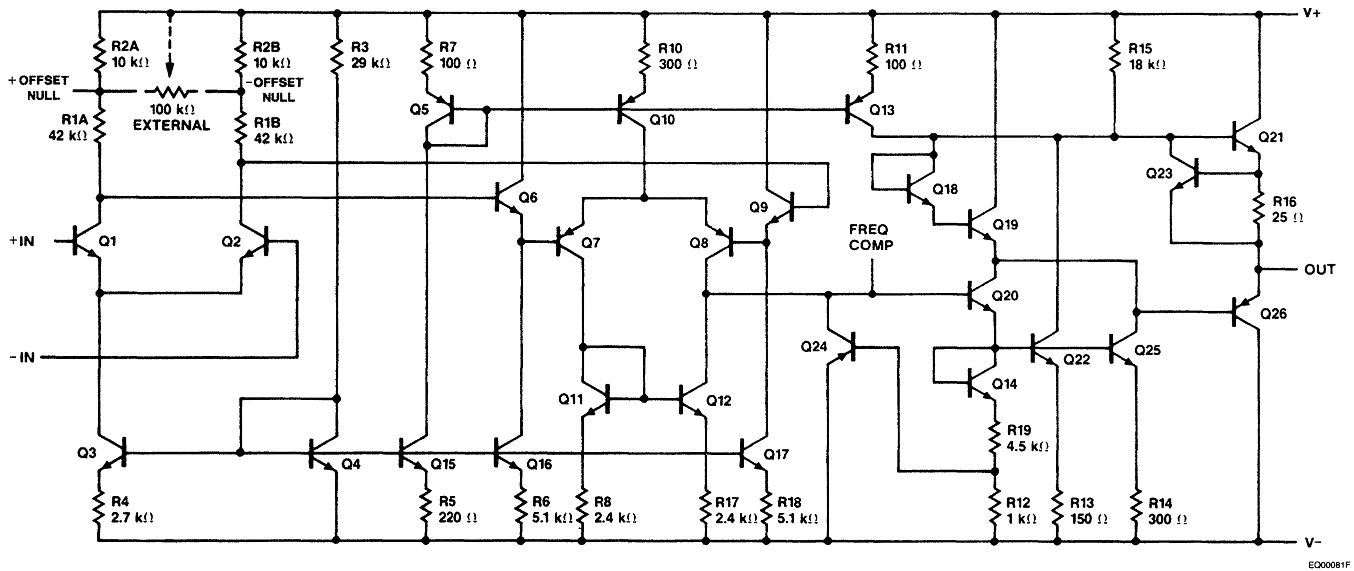
Connection Diagram 8-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA725TC	9T	Molded DIP

Equivalent Circuit



µA725A/E and µA725
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

			µA725A/E			µA725			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IO}	Input Offset Voltage (Without external trim)	$R_S \leqslant 10$ kΩ			0.5		0.5	1.0	mV
I_{IO}	Input Offset Current				5.0		2.0	20	nA
I_{IB}	Input Bias Current				75		42	100	nA
Z_I	Input Impedance			1.5			1.5		MΩ
P_c	Power Consumption	µA725A/µA725		80	120		80	120	mW
		µA725E			150				
		$V_{CC} = \pm 3.0$ V			6.0				
CMR	Common Mode Rejection	$R_S \leqslant 10$ kΩ	120	130		110	120		dB
V_{IR}	Input Voltage Range		±13.5	±14		±13.5	±14		V
PSRR	Power Supply Rejection Ratio	$R_S \leqslant 10$ kΩ		2.0	5.0		2.0	10	µV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	1000	3000		1000	3000		V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.5			±12	±13.5		V
		$R_L = 2.0$ kΩ	±10			±10	±13.5		V
e_n	Input Noise Voltage	$f_o = 10$ Hz		15	15		15		nV/√Hz
		$f_o = 100$ Hz		9.0	12		9.0		
		$f_o = 1.0$ kHz		8.0	12		8.0		
i_n	Input Noise Current	$f_o = 10$ Hz		1.0	1.2		1.0		pA/√Hz
		$f_o = 100$ Hz		0.3	0.6		0.3		
		$f_o = 1.0$ kHz		0.15	0.25		0.15		

The following specifications apply over the range of $0°C \leqslant T_A \leqslant +70°C$ for µA725E, $-55°C \leqslant T_A \leqslant +125°C$ for µA725A and µA725.

V_{IO}	Input Offset Voltage (Without external trim)	$R_S \leqslant 10$ kΩ			0.75			1.5	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (Without external trim)	$R_S = 50$ Ω		2.0	2.0		2.0	5.0	µV/°C
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (With external trim)	$R_S = 50$ Ω		0.6			0.6		µV/°C
I_{IO}	Input Offset Current	$T_A = T_{A\ Max}$			4.0		1.2	20	nA
		$T_A = T_{A\ Min}$		5.0	18		7.5	40	

μA725A/E and μA725 (Cont.)
Electrical Characteristics $V_{CC} = \pm 15$ V, 0°C ≤ T_A ≤ +70°C for μA725E, −55°C ≤ T_A ≤ +125°C for μA725A and μA725.

Symbol	Characteristic	Condition	μA725A/E			μA725			Unit
			Min	Typ	Max	Min	Typ	Max	
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			35	90		35		pA/°C
I_{IB}	Input Bias Current	$T_A = T_{A\ Max}$			70		20	100	nA
		$T_A = T_{A\ Min}$			180		80	200	nA
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	110			100			dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			8.0			20	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $T_A = T_{A\ Max}$	1000			1000			V/mV
		$R_L \geq 2.0$ kΩ, $T_A = T_{A\ Min}$	500			250			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10			±10			V

μA725C
Electrical Characteristics $T_A = 25$°C, $V_{CC} = \pm 15$ V, unless otherwise specified.

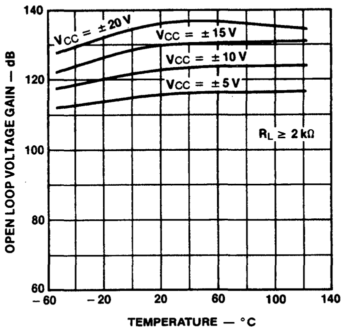
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
I_{IO}	Input Offset Current			2.0	35	nA
I_{IB}	Input Bias Current			42	125	nA
e_n	Input Noise Voltage	$f_o = 10$ Hz		15		$nV/\sqrt{Hz}$
		$f_o = 100$ Hz		9.0		
		$f_o = 1.0$ kHz		8.0		
i_n	Input Noise Current	$f_o = 10$ Hz		1.0		$pA/\sqrt{Hz}$
		$f_o = 100$ Hz		0.3		
		$f_o = 1.0$ kHz		0.15		
Z_I	Input Impedance			1.5		MΩ
V_{IR}	Input Voltage Range		±13.5	±14		V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	250	3000		V/mV
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	94	120		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±13.5		V
		$R_L = 2.0$ kΩ	±10	±13.5		
P_c	Power Consumption			80	150	mW

μA725C (Cont.)
Electrical Characteristics $0°C \leq T_A \leq +70°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (Without external trim)	$R_S = 50$ Ω		2.0		μV/°C
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (With external trim)	$R_S = 50$ Ω		0.6		μV/°C
I_{IO}	Input Offset Current	$T_A = T_{A\ Max}$		1.2	35	nA
		$T_A = T_{A\ Min}$		4.0	50	
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			10		pA/°C
I_{IB}	Input Bias Current	$T_A = T_{A\ Max}$			125	nA
		$T_A = T_{A\ Min}$			250	
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ	125			V/mV
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ		115		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10			V

Typical Performance Curves

Voltage Gain vs Temperature For Supply Voltages For μA725/A



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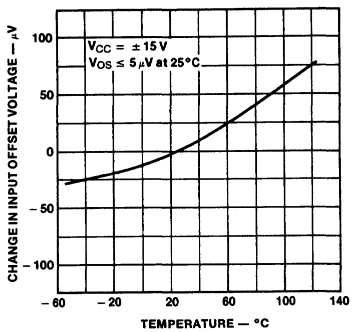
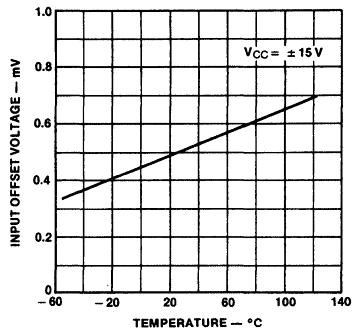
Change In Trimmed Input Offset Voltage vs Temperature For μA725/A



PC03430F

Untrimmed Input Offset Voltage vs Temperature For μA725/A



PC03440F

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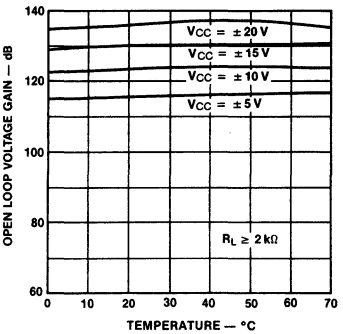
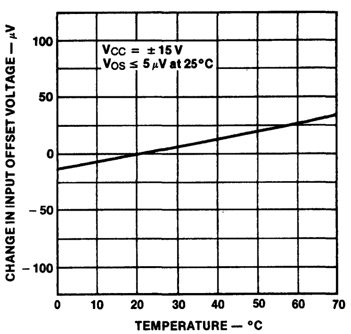
Voltage Gain vs Temperature for Supply Voltages For μA725C/E



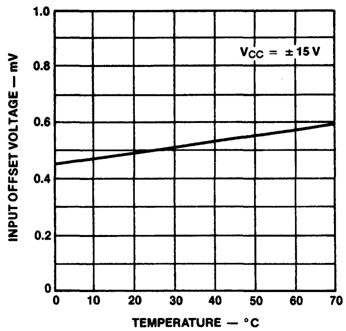
PC03420F

Trimmed Input Offset Voltage vs Temperature For μA725C/E



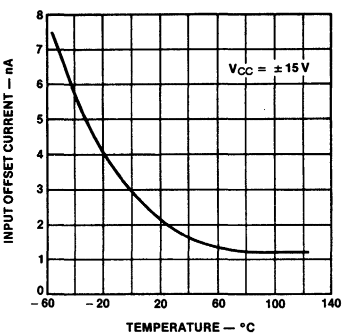
PC03460F

Untrimmed Input Offset Voltage vs Temperature For μA725C/E



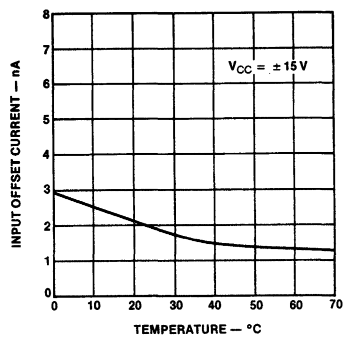
PC03470F

Input Offset Current vs Temperature For μA725/A



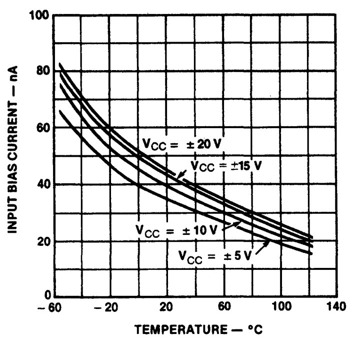
PC03480F

Input Offset Current vs Temperature For μA725C/E



PC03490F

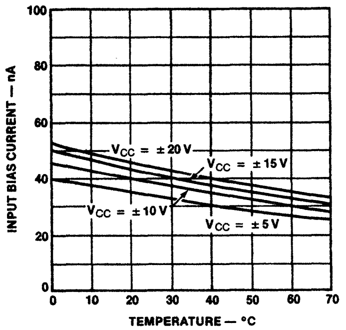
Input Bias Current vs Temperature For μA725/A



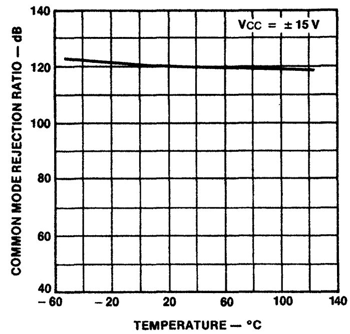
PC03500F

Typical Performance Curves for all Types (Cont.)

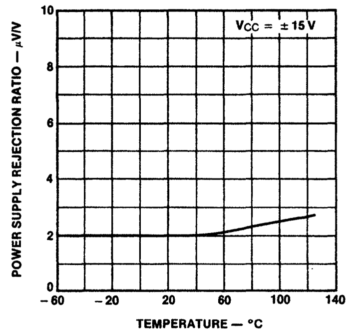
Input Bias Current vs Temperature μA725C/E



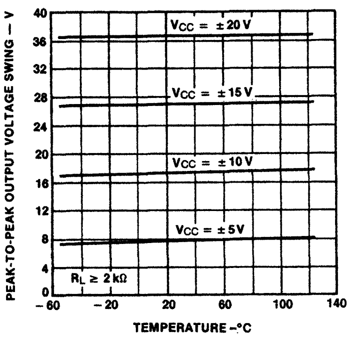
Common Mode Rejection Ratio vs Temperature



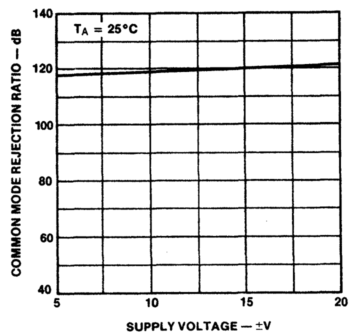
Power Supply Rejection Ratio vs Temperature



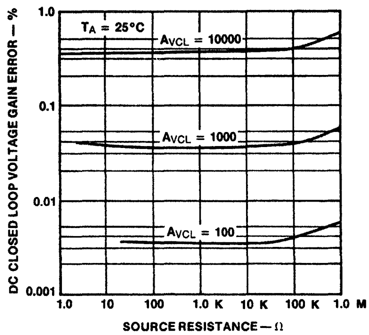
Output Voltage Swing vs Temperature



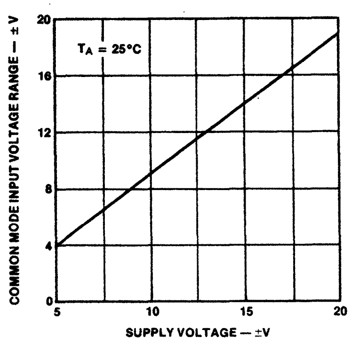
Common Mode Rejection Ratio vs Supply Voltage



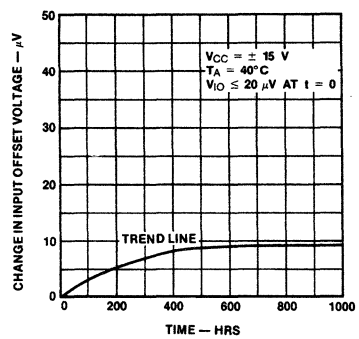
DC Closed Loop Voltage Gain Error vs Source Resistance



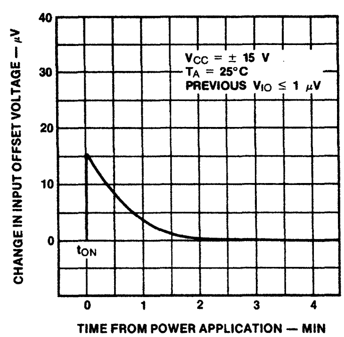
Common Mode Input Voltage Range vs Supply Voltage



Input Offset Voltage Drift vs Time

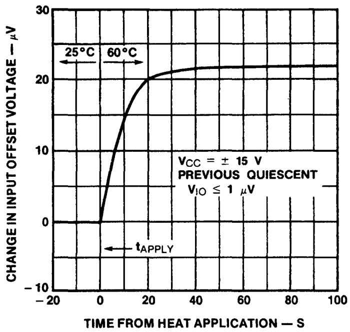


Stabilization Time of Input Offset Voltage From Power Turn-On



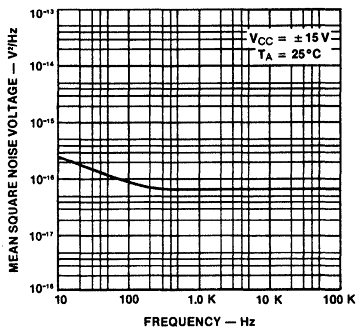
Typical Performance Curves for all Types (Cont.)

Change In Input Offset Voltage Due to Thermal Shock vs Time



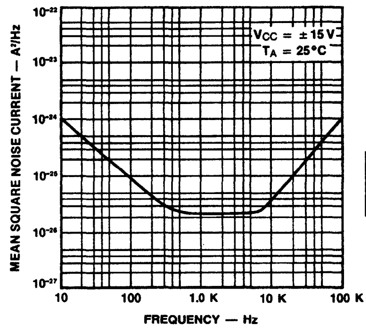
PC03600F

Input Noise Voltage vs Frequency



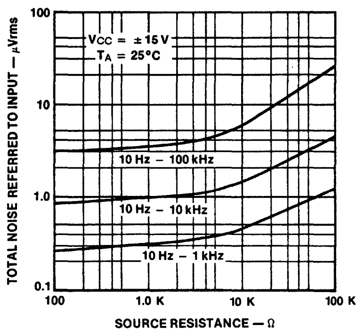
PC03611F

Input Noise Current vs Frequency



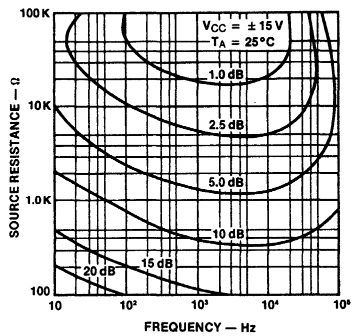
PC03621F

Broadband Noise for Various Bandwidths



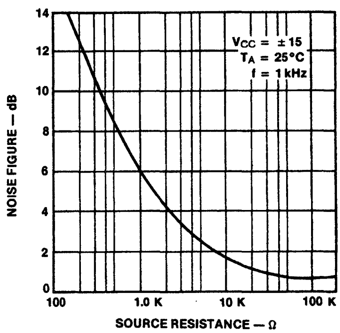
PC03631F

Narrow Band Spot Noise Figure Contours



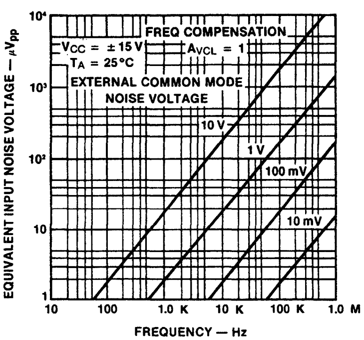
PC03641F

Noise Figure vs Source Resistance



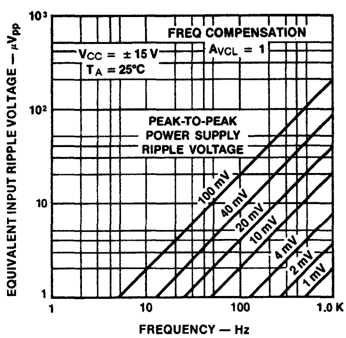
PC03651F

Equivalent Input Noise Voltage Due to External Common Mode Noise vs Frequency



PC03661F

Equivalent Input Ripple Voltage Due to Power Supply Ripple vs Frequency

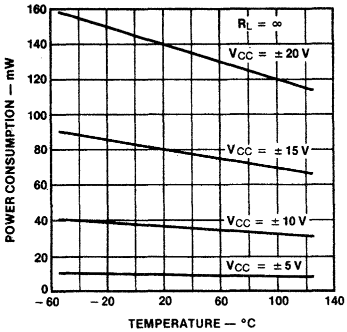


PC03671F

7

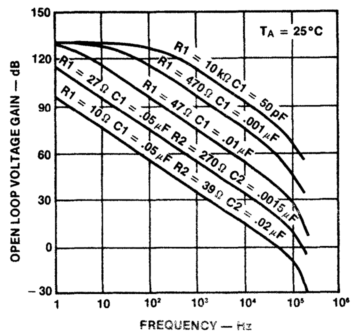
Typical Performance Curves for all Types (Cont.)

Power Consumption vs Temperature



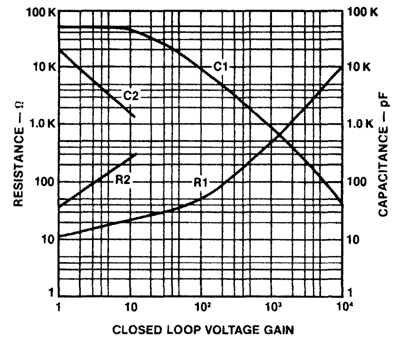
PC03690F

Open Loop Frequency Response For Values of Compensation



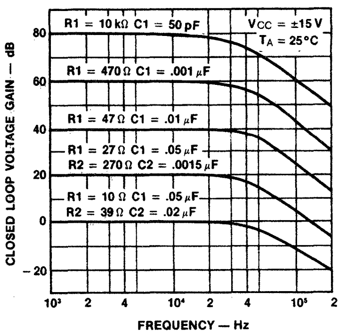
PC03700F

Values for Suggested Compensation Networks vs Various Closed Loop Voltage Gains



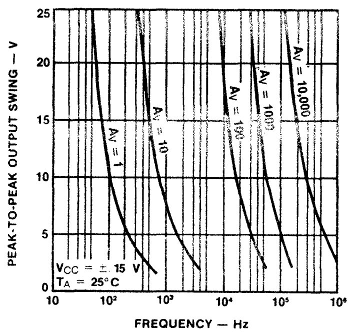
PC03711F

Frequency Response for Various Closed Loop Gains



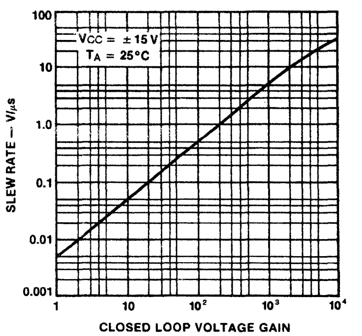
PC03720F

Output Voltage Swing vs Frequency



PC03730F

Slew Rate vs Closed Loop Gain

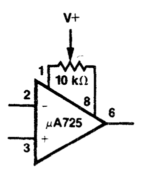


PC03741F

Compensation Component Values

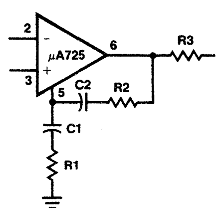
A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

Voltage Offset Null Circuit



CR01140F

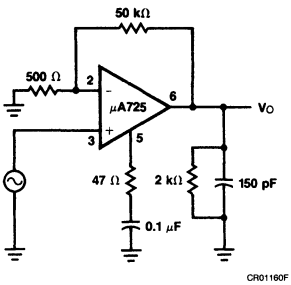
Frequency Compensation Circuit



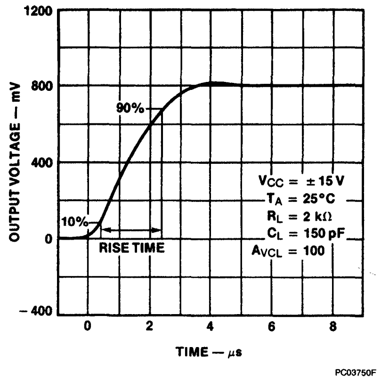
CR01150F

Use $R_3 = 51\Omega$ when the amplifier is operated with capacitive load.

Transient Response Test Circuit

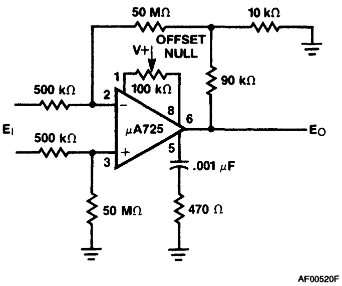


Transient Response



Typical Applications

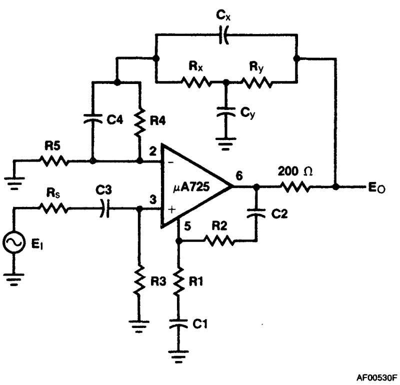
Precision Amplifier $A_{VCL} = 1000$



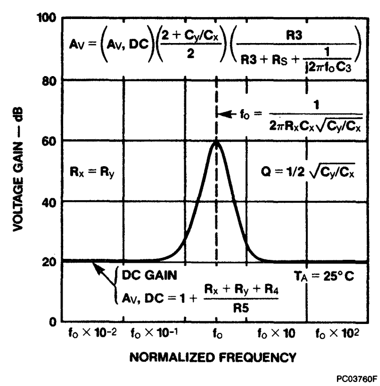
Characteristics

$A_V = 1000 = 60$ dB
DC Gain Error = 0.05%
Bandwidth = 1 kHz for −0.05% error
Diff. Input Res. = 1 MΩ
Typical amplifying capability
$e_n = 10$ μV on $V_{CM} = 1.0$ V
Caution: Minimize Stray Capacitance

Active Filter — Band Pass With 60 dB Gain



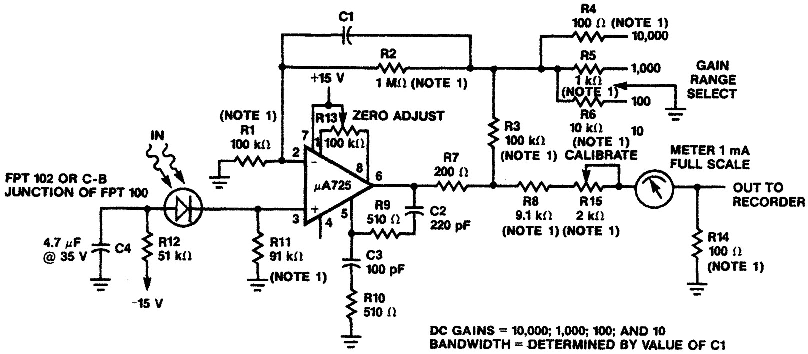
Active Filter Frequency Response



Lead numbers are shown for metal package only.

Typical Applications (Cont.)

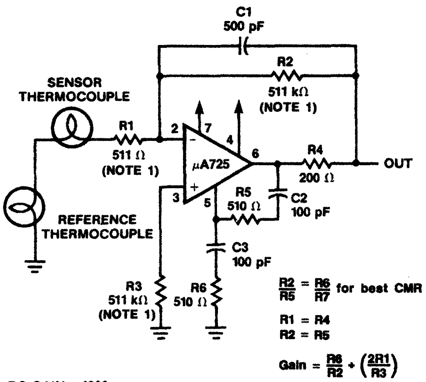
Photodiode Amplifier (Note 2)



DC GAINS = 10,000; 1,000; 100; AND 10
BANDWIDTH = DETERMINED BY VALUE OF C1

AF00541F

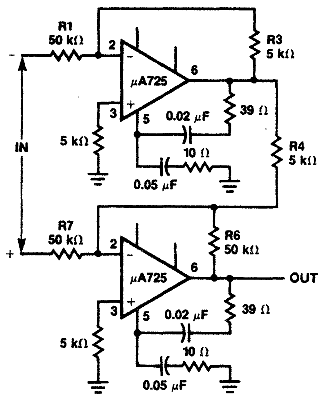
Thermocouple Amplifier (Note 2)



DC GAIN = 1000
BANDWIDTH = DC TO 540 Hz
EQUIVALENT INPUT NOISE = 0.24 μVrms

AF00551F

± 100 V Common Mode Range Differential Amplifier (Note 2)



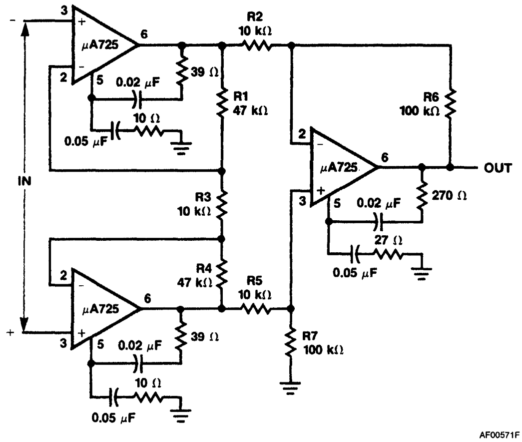
AF00561F

Notes

1. Indicates ± 1% metal film resistors recommended for temperature stability.
2. Lead numbers are shown for metal package only.

Typical Applications (Cont.)

Instrumentation Amplifier With High Common Mode Rejection (Note 1)



$\frac{R1}{R6} = \frac{R3}{R4}$ for best CMRR

$R3 = R4$

$R1 = R6 = 10\ R3$

$\text{Gain} = \frac{R6}{R7}$

Note

1. Lead numbers are shown for metal package only.

7

μA741
Operational Amplifier

FAIRCHILD
A Schlumberger Company

Description
The μA741 is a high performance monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch up tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.

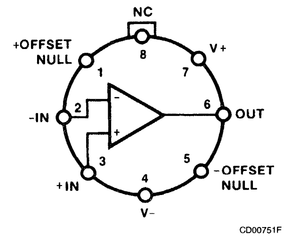
- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA741AM, μA741M)	−55°C to +125°C
Commercial (μA741EC, μA741C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
8L-Ceramic DIP	1.30 W
SO-8	0.81 W
Supply Voltage	
μA741A, μA741, μA741E	±22 V
μA741C	±18 V
Differential Input Voltage	±30 V
Input Voltage[3]	±15 V
Output Short Circuit Duration[4]	Indefinite

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, the 8L-Ceramic DIP at 8.7 mW/°C, and the SO-8 at 6.5 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

Connection Diagram
8-Lead Metal Package
(Top View)

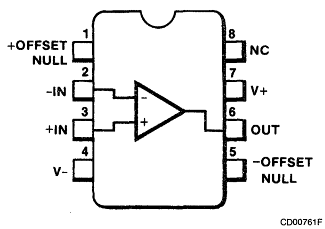


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA741HM	5W	Metal
μA741HC	5W	Metal
μA741AHM	5W	Metal
μA741EHC	5W	Metal

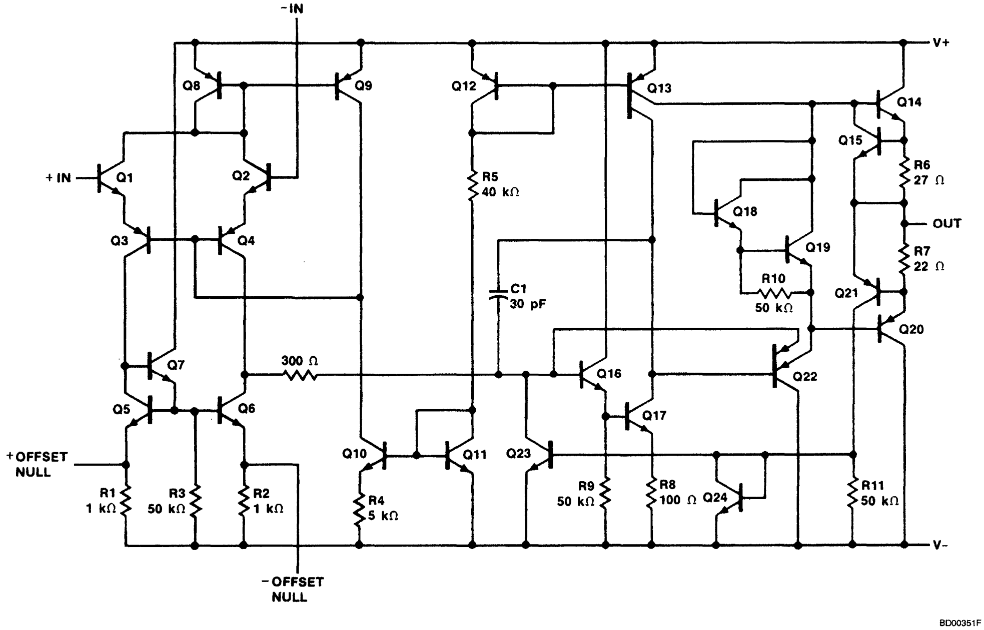
Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA741RM	6T	Ceramic DIP
μA741RC	6T	Ceramic DIP
μA741SC	KC	Molded Surface Mount
μA741TC	9T	Molded DIP
μA741ARM	6T	Ceramic DIP
μA741ERC	6T	Ceramic DIP
μA741ETC	9T	Molded DIP

Equivalent Circuit



μA741 and μA741C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	μA741 Min	μA741 Typ	μA741 Max	μA741C Min	μA741C Typ	μA741C Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		1.0	5.0		2.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				±15			±15		mV
I_{IO}	Input Offset Current				20	200		20	200	nA
I_{IB}	Input Bias Current				80	500		80	500	nA
Z_I	Input Impedance			0.3	2.0		0.3	2.0		MΩ
I_{CC}	Supply Current				1.7	2.8		1.7	2.8	mA
P_c	Power Consumption				50	85		50	85	mW
CMR	Common Mode Rejection			70			70	90		dB
V_{IR}	Input Voltage Range			±12	±13		±12	±13		V
PSRR	Power Supply Rejection Ratio				30	150				μV/V
			$V_{CC} = \pm 5.0$ V to ± 18 V					30	150	
I_{OS}	Output Short Circuit Current				25			25		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	50	200		20	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12			±12	±14		V
			$R_L = 2.0$ kΩ	±10			±10	±13		
TR	Transient Response	Rise time	$V_I = 20$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.3			0.3		μs
		Overshoot			5.0			5.0		%
BW	Bandwidth				1.0			1.0		MHz
SR	Slew Rate		$R_L \geqslant 2.0$ kΩ, $A_V = 1.0$		0.5			0.5		V/μs

μA741 and μA741C (Cont.)
Electrical Characteristics Over the range of $-55°C \leqslant T_A \leqslant +125°C$ for μA741, $0°C \leqslant T_A \leqslant +70°C$ for μA741C, unless otherwise specified.

Symbol	Characteristic	Condition	μA741 Min	μA741 Typ	μA741 Max	μA741C Min	μA741C Typ	μA741C Max	Unit
V_{IO}	Input Offset Voltage							7.5	mV
		$R_S \leqslant 10$ kΩ		1.0	6.0				
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range			±15			±15		mV
I_{IO}	Input Offset Current							300	nA
		$T_A = +125°C$		7.0	200				
		$T_A = -55°C$		85	500				
I_{IB}	Input Bias Current							800	nA
		$T_A = +125°C$		0.03	0.5				μA
		$T_A = -55°C$		0.3	1.5				
I_{CC}	Supply Current	$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				
P_c	Power Consumption	$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		60	100				
CMR	Common Mode Rejection	$R_S \leqslant 10$ kΩ	70	90					dB
V_{IR}	Input Voltage Range		±12	±13					V
PSRR	Power Supply Rejection Ratio			30	150				μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	25			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±14					V
		$R_L = 2.0$ kΩ	±10	±13		±10	±13		

μA741A and μA741E
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 50\ \Omega$		0.8	3.0	mV
I_{IO}	Input Offset Current				3.0	30	nA
I_{IB}	Input Bias Current				30	80	nA
Z_I	Input Impedance		$V_{CC} = \pm 20$ V	1.0	6.0		MΩ
P_c	Power Consumption		$V_{CC} = \pm 20$ V		80	150	mW
PSRR	Power Supply Rejection Ratio		$V_{CC} = +10$ V, -20 V to $V_{CC} = +20$ V, -10 V, $R_S = 50\ \Omega$		15	50	μV/V
I_{OS}	Output Short Circuit Current			10	25	40	mA
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 20$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 15$ V	50	200		V/mV
TR	Transient Response	Rise time	$A_V = 1.0$, $V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF		0.25	0.8	μs
		Overshoot			6.0	20	%
BW	Bandwidth			0.437	1.5		MHz
SR	Slew Rate		$V_I = \pm 10$ V, $A_V = 1.0$	0.3	0.7		V/μs

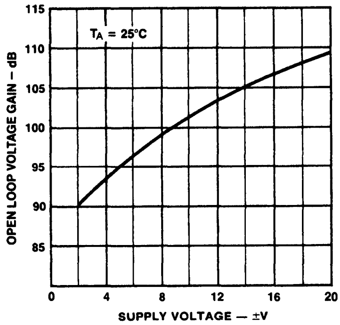
The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$ for the μA741A, and $0°C \leqslant T_A \leqslant +70°C$ for the μA741E.

Symbol	Characteristic	Condition			Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage						4.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity						15	μV/°C
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$V_{CC} = \pm 20$ V			10			mV
I_{IO}	Input Offset Current						70	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity						0.5	nA/°C
I_{IB}	Input Bias Current						210	nA
Z_I	Input Impedance				0.5			MΩ
P_c	Power Consumption	$V_{CC} = \pm 20$ V	μA741A	−55°C			165	mW
				+125°C			135	
			μA741E				150	
CMR	Common Mode Rejection	$V_{CC} = \pm 20$ V, $V_I = \pm 15$ V, $R_S = 50\ \Omega$			80	95		dB
I_{OS}	Output Short Circuit Current				10		40	mA
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 20$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 15$ V			32			V/mV
		$V_{CC} = \pm 5.0$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 2.0$ V			10			
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 20$ V	$R_L = 10$ kΩ		±16			V
			$R_L = 2.0$ kΩ		±15			

7

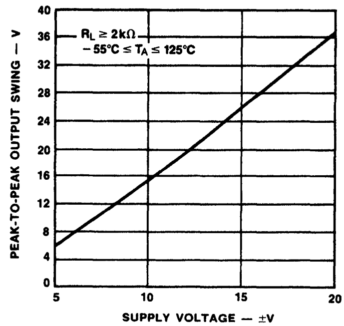
Typical Performance Curves

Voltage Gain vs Supply Voltage for µA741/A



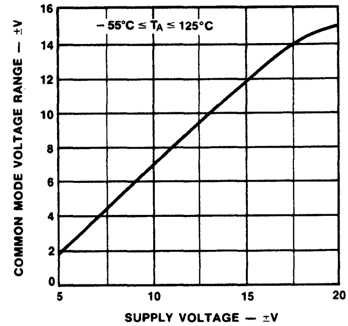
PC05160F

Output Voltage Swing vs Supply Voltage for µA741/A



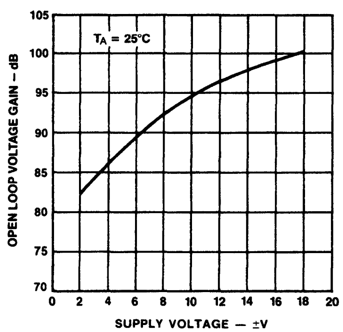
PC05170F

Input Common Mode Voltage vs Supply Voltage for µA741/A



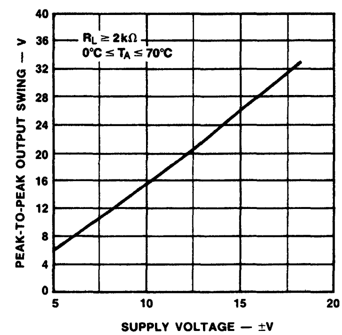
PC05180F

Voltage Gain vs Supply Voltage for µA741C/E



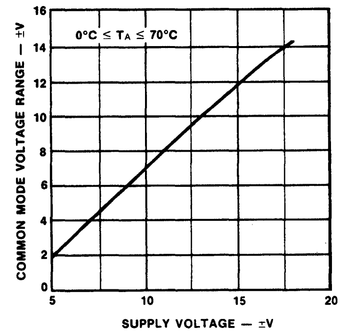
PC05190F

Output Voltage Swing vs Supply Voltage for µA741C/E



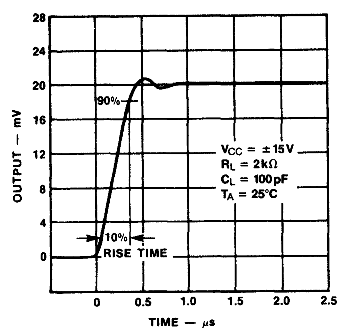
PC05200F

Input Common Mode Voltage Range vs Supply Voltage for µA741C/E



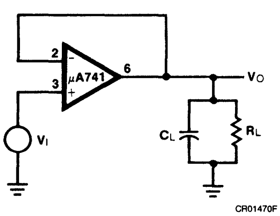
PC05210F

Transient Response for µA741C/E



PC05220F

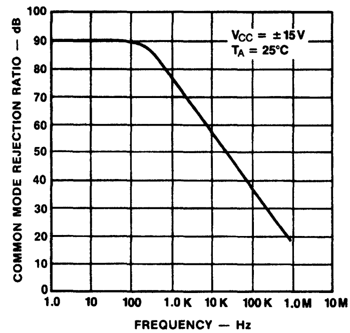
Transient Response Test Circuit for µA741C/E



CR01470F

Lead numbers are shown for metal package only

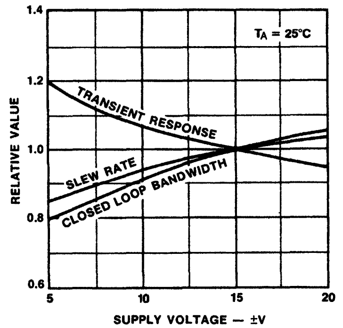
Common Mode Rejection Ratio vs Frequency for µA741C/E



PC05241F

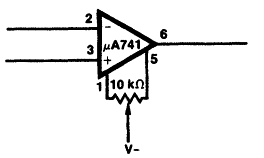
Typical Performance Curves (Cont.)

Frequency Characteristics vs Supply Voltage for μA741C/E



PC05251F

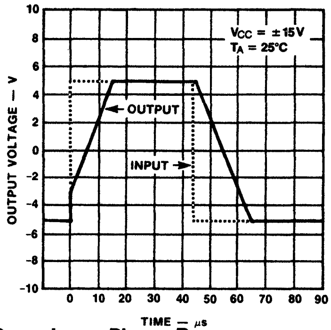
Voltage Offset Null Circuit for μA741C/E



CR01480F

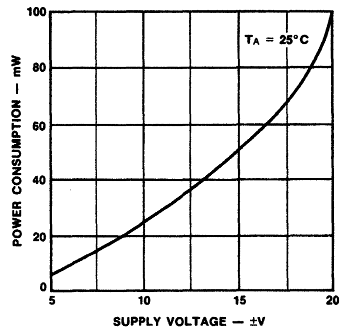
Lead numbers are shown for metal package only

Voltage Follower Large Signal Pulse Response for μA741C/E



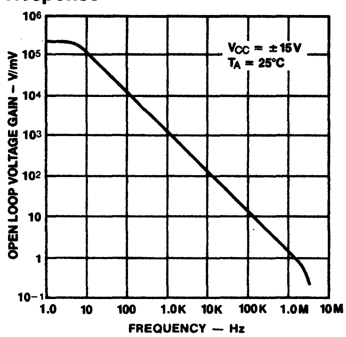
PC05260F

Power Consumption vs Supply Voltage



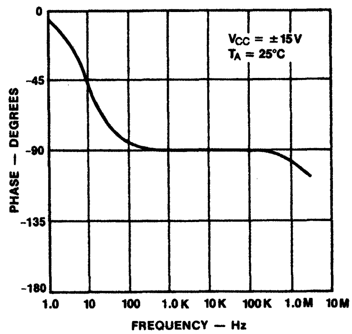
PC05271F

Open Loop Frequency Response



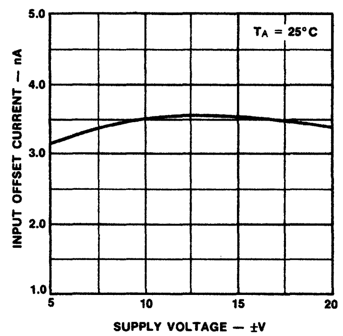
PC05281F

Open Loop Phase Response vs Frequency



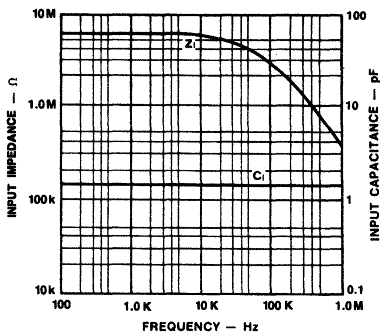
PC05291F

Input Offset Current vs Supply Voltage



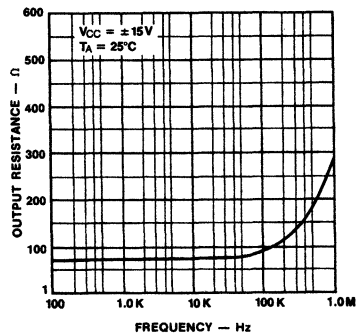
PC05301F

Input Impedance and Input Capacitance vs Frequency



PC05311F

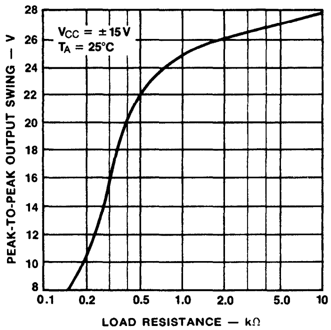
Output Resistance vs Frequency



PC05321F

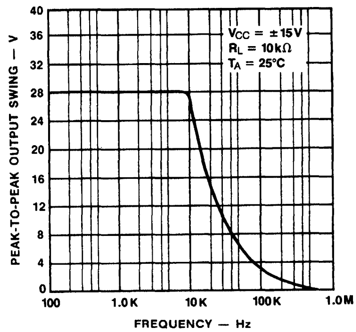
Typical Performance Curves (Cont.)

Output Voltage Swing vs Load Resistance



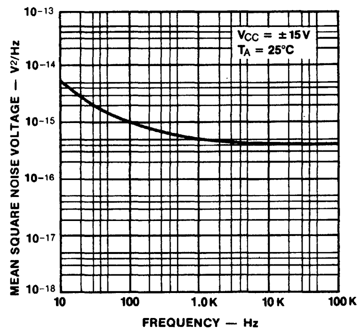
PC05330F

Output Voltage Swing vs Frequency



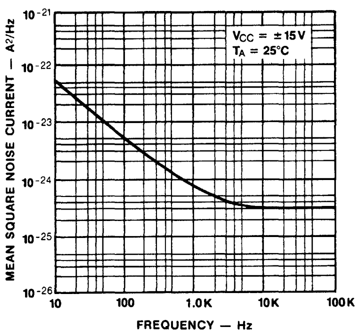
PC05341F

Input Noise Voltage vs Frequency



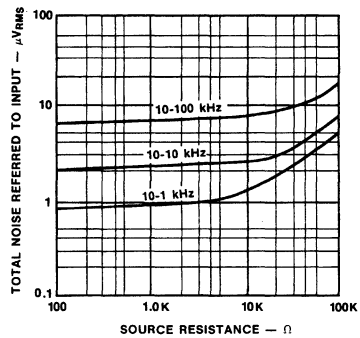
PC05361F

Input Noise Current vs Frequency



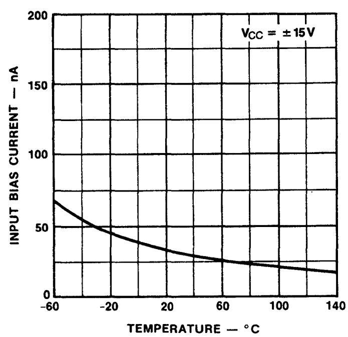
PC05371F

Broadband Noise for Various Bandwidths



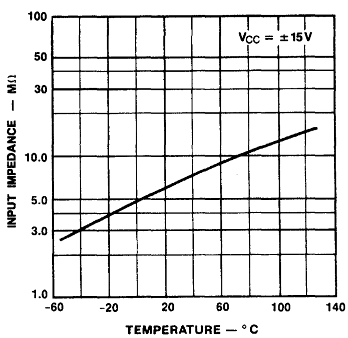
PC05381F

Input Bias Current vs Temperature for μA741/A



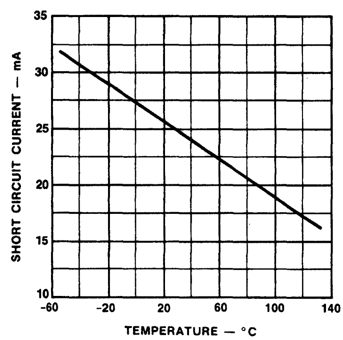
PC05390F

Input Impedance vs Temperature for μA741/A



PC05401F

Short Circuit Current vs Temperature for μA741/A



PC05411F

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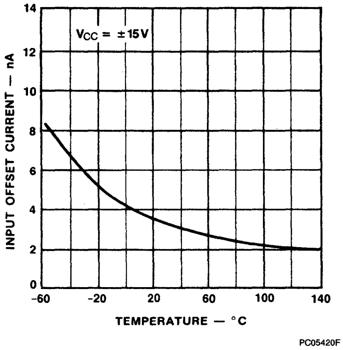
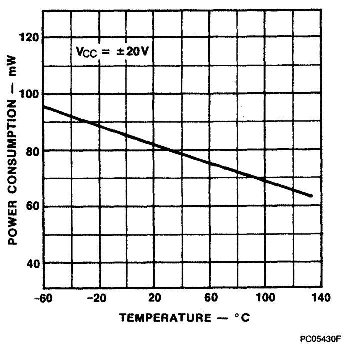
Typical Performance Curves (Cont.)

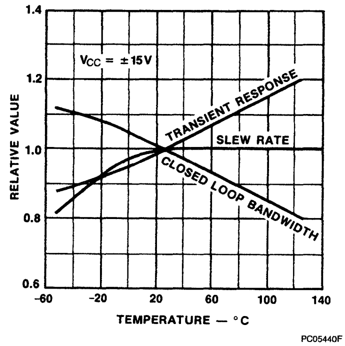
Input Offset Current vs Temperature for μA741/A



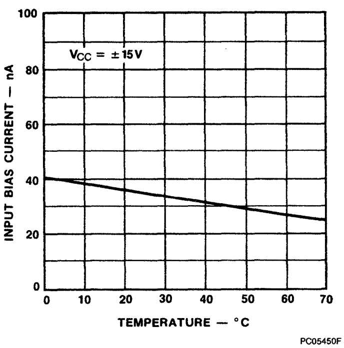
Power Consumption vs Temperature for μA741/A



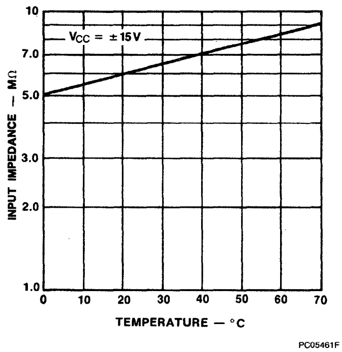
Frequency Characteristics vs Temperature for μA741/A



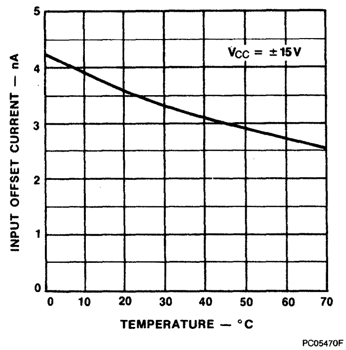
Input Bias Current vs Temperature for μA741C/E



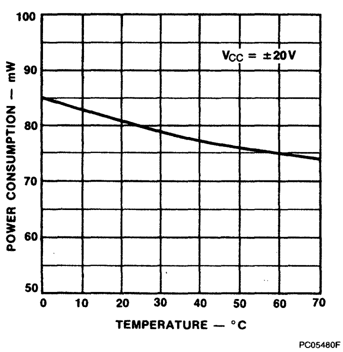
Input Impedance vs Temperature for μA741C/E



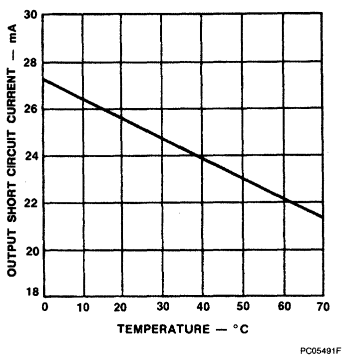
Input Offset Current vs Temperature for μA741C/E



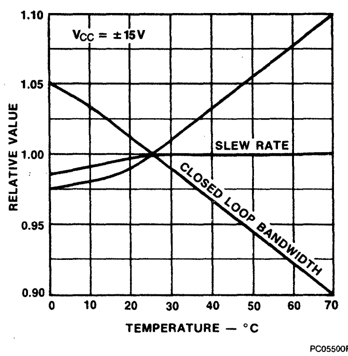
Power Consumption vs Temperature for μA741C/E



Short Circuit Current vs Temperature for μA741C/E



Frequency Characteristics vs Temperature for μA741C/E



FAIRCHILD

A Schlumberger Company

μA747 Dual Operational Amplifier

Linear Division Operational Amplifiers

Description

The μA747 contains a pair of high performance monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch up make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, *see μA741 data sheet.*

- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

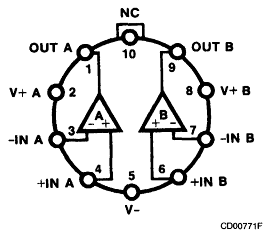
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Extended (μA747AM, μA747M)	−55°C to +125°C
Commercial (μA747EC, μA747C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	
μA747A, μA747	±22 V
μA747E, μA747C	±18 V
Differential Input Voltage	±30 V
Input Voltage[3]	±15 V
Voltage Between Offset Null and V−	±0.5 V
Output Short Circuit Duration[4]	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Metal Can Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram 10-Lead Metal Package (Top View)

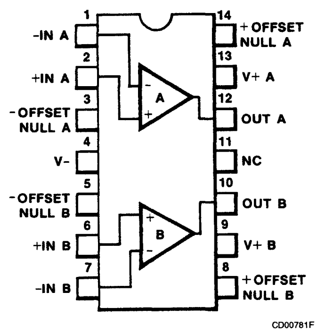


Lead 5 connected to case.

Order Information

Device Code	Package Code	Package Description
μA747HM	5X	Metal
μA747HC	5X	Metal
μA747AHM	5X	Metal
μA747EHC	5X	Metal

Connection Diagram 14-Lead DIP and SO-14 Package (Top View)

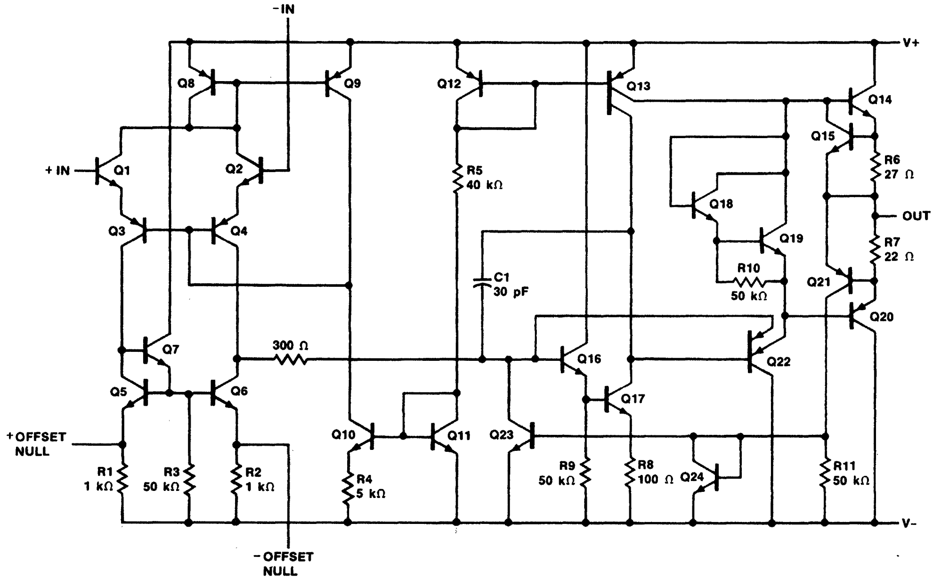


Order Information

Device Code	Package Code	Package Description
μA747DM	6A	Ceramic DIP
μA747DC	6A	Ceramic DIP
μA747PC	9A	Molded DIP
μA747SC	KD	Molded Surface Mount
μA747ADM	6A	Ceramic DIP
μA747EDC	6A	Ceramic DIP

4. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

Equivalent Circuit (1/2 of circuit)



V+A is internally connected to V+B.

μA747 and μA747C
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	μA747 Min	μA747 Typ	μA747 Max	μA747C Min	μA747C Typ	μA747C Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0		1.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				±15			±15		mV
I_{IO}	Input Offset Current				20	200		20	200	nA
I_{IB}	Input Bias Current				80	500		80	500	nA
Z_I	Input Impedance			0.3	2.0		0.3	2.0		MΩ
I_{CC}	Supply Current				3.4	5.6		3.9	5.6	mA
P_c	Power Consumption				100	170		100	170	mW
PSRR	Power Supply Rejection Ratio				30	150				μV/V
			$V_{CC} = \pm 5.0$ V to ±18 V					30	150	
I_{OS}	Output Short Circuit Current				25			25		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	50	200		25	200		V/mV
TR	Transient Response	Rise time	$V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.3			0.3		μs
		Overshoot			5.0			5.0		%
BW	Bandwidth				1.0			1.0		MHz
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$		0.5			0.5		V/μs
CS	Channel Separation				120			120		dB

The following specifications apply over the range of $-55°C \leq T_A \leq +125°C$ for μA747, $0°C \leq T_A \leq 70°C$ for μA747C

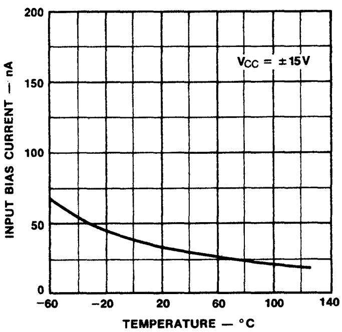
Symbol	Characteristic	Condition	μA747 Min	μA747 Typ	μA747 Max	μA747C Min	μA747C Typ	μA747C Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0		1.0	7.5	mV
I_{IO}	Input Offset Current	$0°C \leq T_A \leq 70°C$					7.0	300	nA
		$T_A = +125°C$		7.0	200				
		$T_A = -55°C$		85	500				
I_{IB}	Input Bias Current	$0°C \leq T_A \leq 70°C$					30	800	nA
		$T_A = +125°C$		0.03	0.5				μA
		$T_A = -55°C$		0.3	1.5				
I_{CC}	Supply Current	$0°C \leq T_A \leq 70°C$					4.0	6.6	mA
		$T_A = +125°C$		3.0	5.0				
		$T_A = -55°C$		4.0	6.6				
P_c	Power Consumption	$0°C \leq T_A \leq 70°C$					120	200	mW
		$T_A = +125°C$		90	150				
		$T_A = -55°C$		120	200				
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range		±12	±13		±12	±13		V
PSRR	Power Supply Rejection Ratio			30	150				μV/V
		$V_{CC} = \pm 5.0$ V to ±18 V					30	150	
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	25			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12	±14		±12	±14		V
		$R_L = 2.0$ kΩ	±10	±13		±10	±13		

μA747A and μA747E
Electrical Characteristics $T_A = 25°C$, $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 50\ \Omega$		0.8	3.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$V_{CC} = \pm 20$ V	10			mV
I_{IO}	Input Offset Current			3.0	30	nA
I_{IB}	Input Bias Current			30	80	nA
Z_I	Input Impedance	$V_{CC} = \pm 20$ V	1.0	6.0		MΩ
P_c	Power Consumption	$V_{CC} = \pm 20$ V		160	300	mW
CMR	Common Mode Rejection	$V_{CC} = \pm 20$ V, $V_I = \pm 15$ V, $R_S = 50\ \Omega$	80	95		dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = +10$ V, −20 V to $V_{CC} = +20$ V, −10 V, $R_S = 50\ \Omega$		15	50	μV/V
I_{OS}	Output Short Circuit Current	μA747A	10	25	40	mA
		μA747E	10	25	35	
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 20$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 15$ V	50			V/mV
TR	Transient Response — Rise time	$V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.25	0.8	μs
	Transient Response — Overshoot			6.0	20	%
BW	Bandwidth		0.437	1.5		MHz
SR	Slew Rate	$V_I = \pm 10$ V, $A_V = 1$	0.3	0.7		V/μs
The following specifications apply over the range of $-55°C \leqslant T_A \leqslant +125°C$ for μA747A, $0°C \leqslant T_A \leqslant +70°C$ for μA747E.						
V_{IO}	Input Offset Voltage				4.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity				15	μV/°C
I_{IO}	Input Offset Current				70	nA
I_{IB}	Input Bias Current				210	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	μA747E, $T_A = 25°C$ to 70°C			0.2	nA/°C
		μA747E, $T_A = 0°C$ to 25°C			0.5	
		μA747A, $T_A = 25°C$ to 125°C			0.2	
		μA747A, $T_A = -55°C$ to +25°C			0.5	
Z_I	Input Impedance	$V_{CC} = \pm 20$ V	0.5			MΩ
P_c	Power Consumption	$V_{CC} = \pm 20$ V, μA747A, −55°C			330	mW
		$V_{CC} = \pm 20$ V, μA747A, +125°C			270	
		$V_{CC} = \pm 20$ V, μA747E			330	
I_{OS}	Output Short Circuit Current		10		40	mA
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 20$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 15$ V	32			V/mV
		$V_{CC} = \pm 5$ V, $R_L \geqslant 2.0$ kΩ, $V_O = \pm 2.0$ V	10			
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 20$ V, $R_L = 10$ kΩ	±16			V
		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ	±15			
CS	Channel Separation	$V_{CC} = \pm 20$ V	100			dB

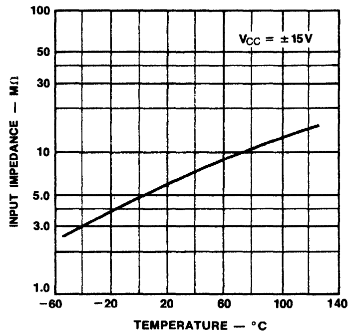
Typical Performance Curves for μA747A and μA747

Input Bias Current vs Temperature



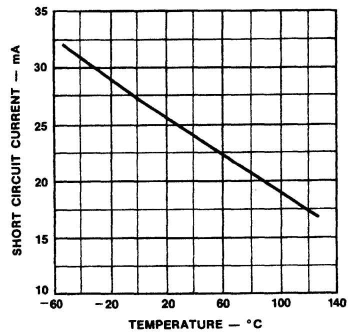
PC05510F

Input Impedance vs Temperature



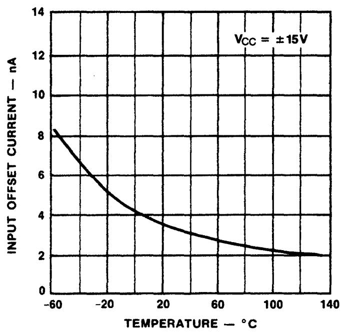
PC05521F

Short Circuit Current vs Temperature



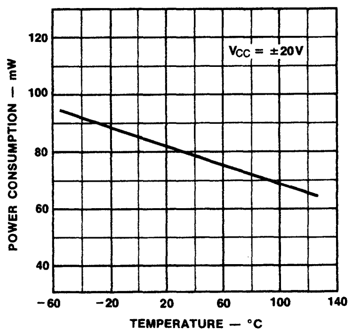
PC05531F

Input Offset Current vs Temperature



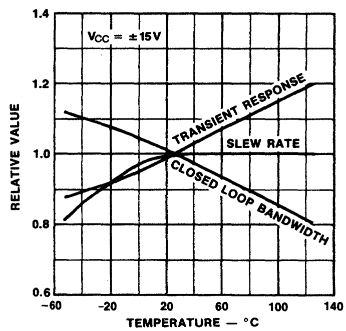
PC05540F

Power Consumption vs Temperature



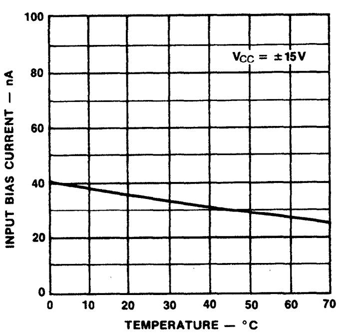
PC05550F

Frequency Characteristics vs Temperature



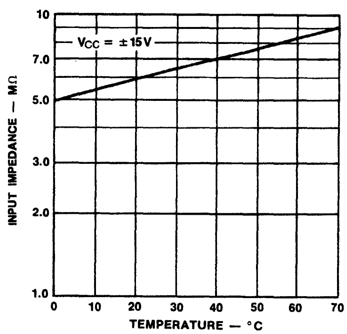
PC05560F

Input Bias Current vs Temperature For μA747C/E



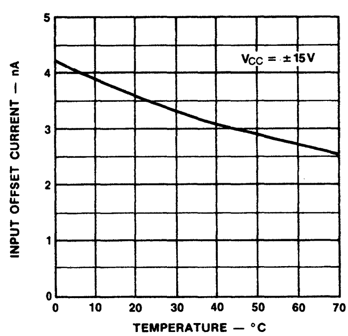
PC05570F

Input Impedance vs Temperature For μA747C/E



PC05581F

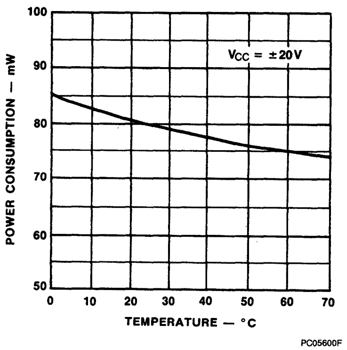
Input Offset Current vs Temperature For μA747C/E



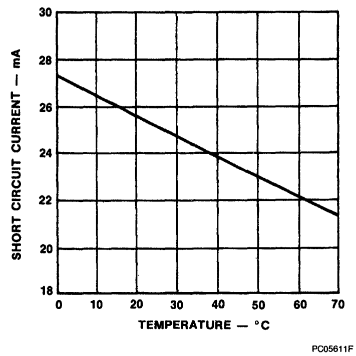
PC05590F

Typical Performance Curves (Cont.)

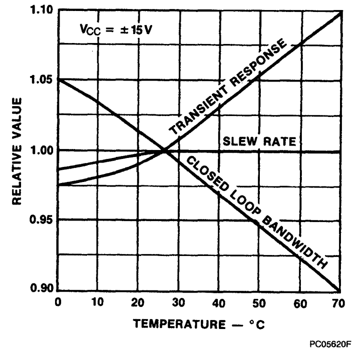
Power Consumption vs Temperature For μA747C/E



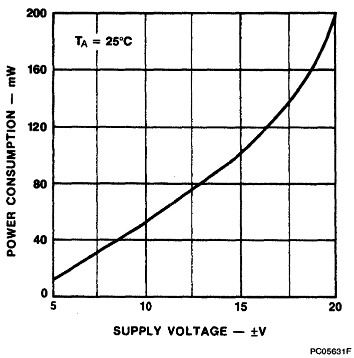
Short Circuit Current vs Temperature For μA747C/E



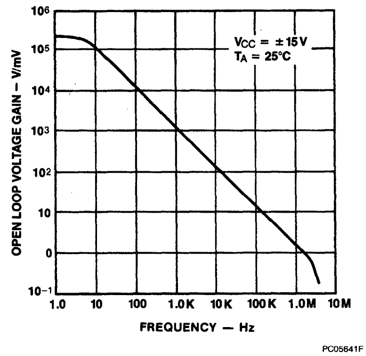
Frequency Characteristics vs Temperature For μA747C/E



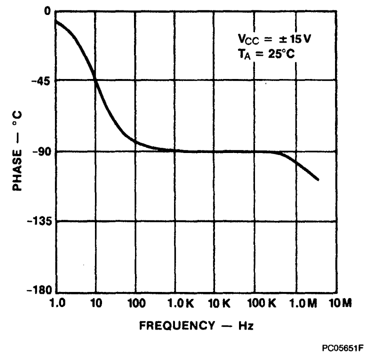
Power Consumption vs Supply Voltage



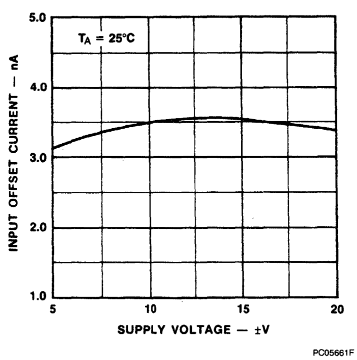
Open Loop Frequency Response



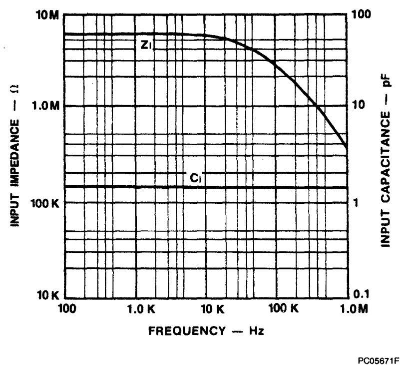
Open Loop Phase Response vs Frequency



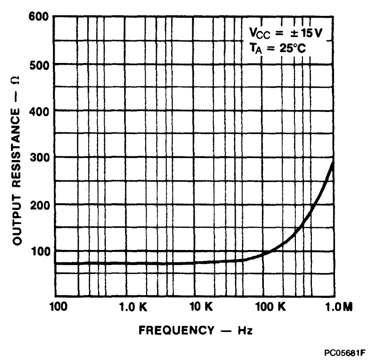
Input Offset Current vs Supply Voltage



Input Impedance and Input Capacitance vs Frequency

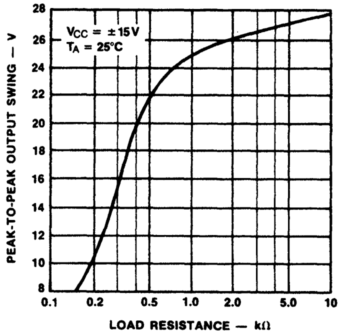


Output Resistance vs Frequency



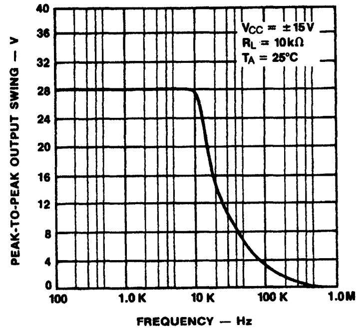
Typical Performance Curves (Cont.)

Output Voltage Swing vs Load Resistance



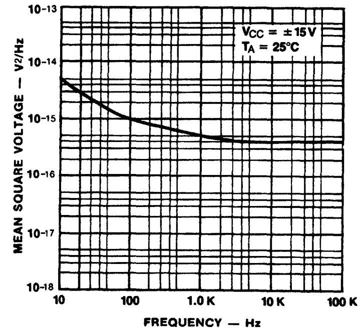
PC05690F

Output Voltage Swing vs Frequency



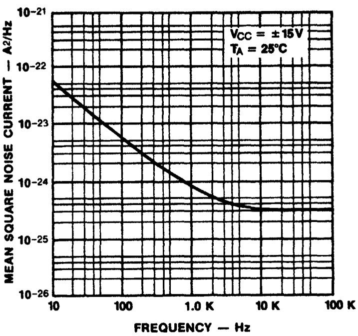
PC05701F

Input Noise Voltage Density vs Frequency



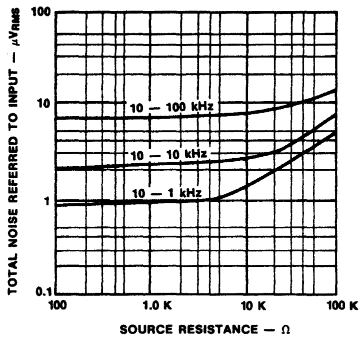
PC05711F

Input Noise Current Density vs Frequency



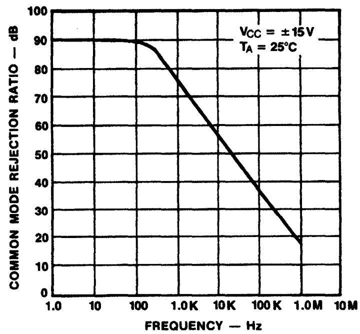
PC05721F

Broadband Noise for Various Bandwidths



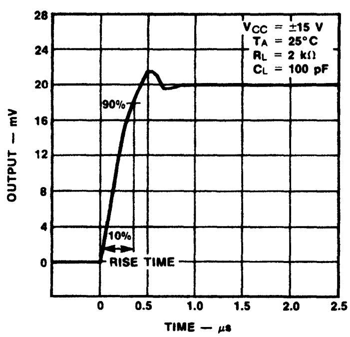
PC05731F

Common Mode Rejection Ratio vs and Frequency μA747/C



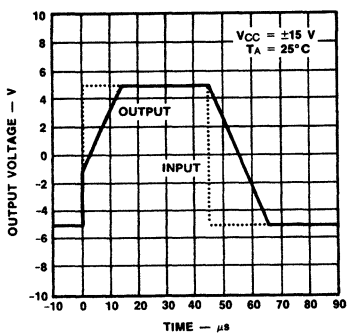
PC05741F

Transient Response For μA747/C



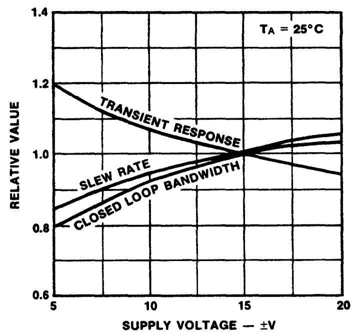
PC05751F

Voltage Follower Large Signal Pulse Response For μA747/C



PC05760F

Frequency Characteristics vs Supply Voltage For μA747/C

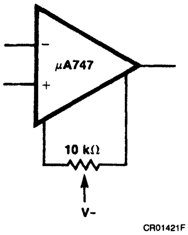


PC05770F

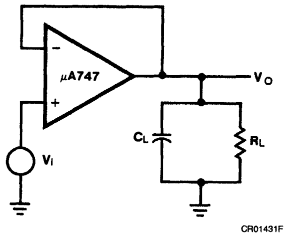
7

Test Circuits

Voltage Offset Null Circuit

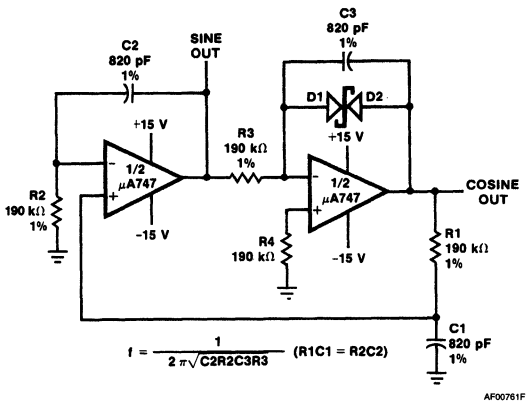


Transient Response Test Circuit

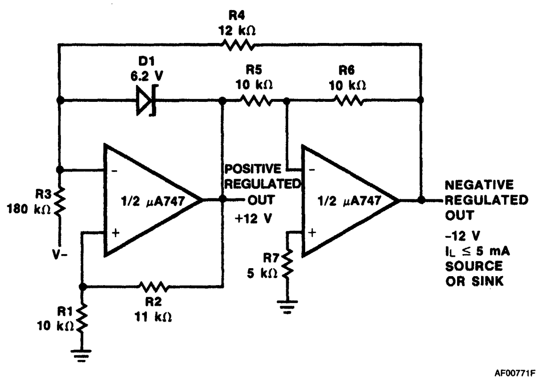


Typical Applications

Quadrature Oscillator



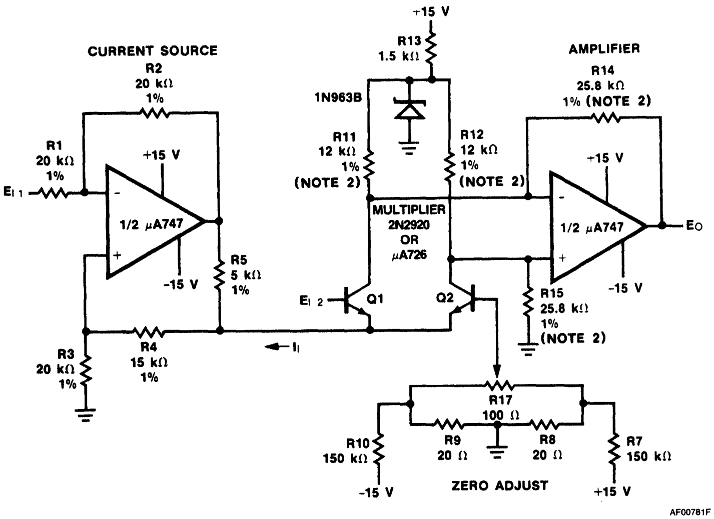
Tracking Positive and Negative Voltage References



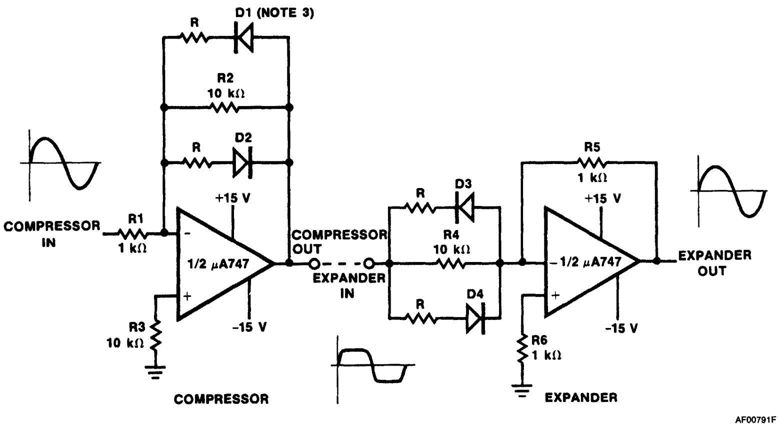
$$\text{Positive Output} = V_{D1} \times \frac{R1 + R2}{R2}$$

$$\text{Negative Output} = -\text{Positive Output} \times \frac{R6}{R5}$$

Analog Multiplier



Compressor/Expander Amplifiers (Note 1)



Notes

1. Maximum Compression Expansion Ratio = R/R (10 kΩ > R ⩾ 0)
2. Matched to 0.1% $E_O = 100\ E_{I1} \times E_{I2}$
3. Diodes D1 through D4 are matched FD666 or Equivalent

FAIRCHILD

A Schlumberger Company

μA748 Operational Amplifier

Description

The μA748 is a high performance monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch up make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short circuit protected and has the same lead configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor.

- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

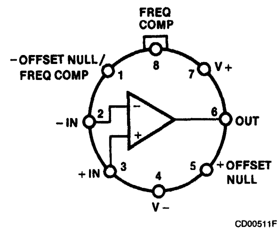
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (μA748M)	-55°C to +125°C
Commercial (μA748C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
8L-Ceramic DIP	1.30 W
SO-8	0.81 W
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[3]	±15 V
Output Short Circuit Duration[4]	Indefinite

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can and Ceramic DIP
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, the 8L-Ceramic DIP at 8.7 mW/°C, and the SO-8 at 6.5 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or +75°C ambient temperature.

Connection Diagram
8-Lead Metal Package
(Top View)

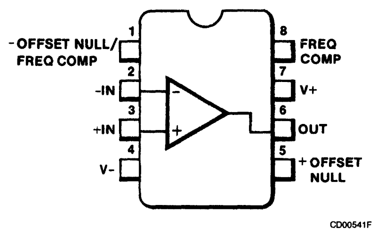


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA748HM	5W	Metal
μA748HC	5W	Metal

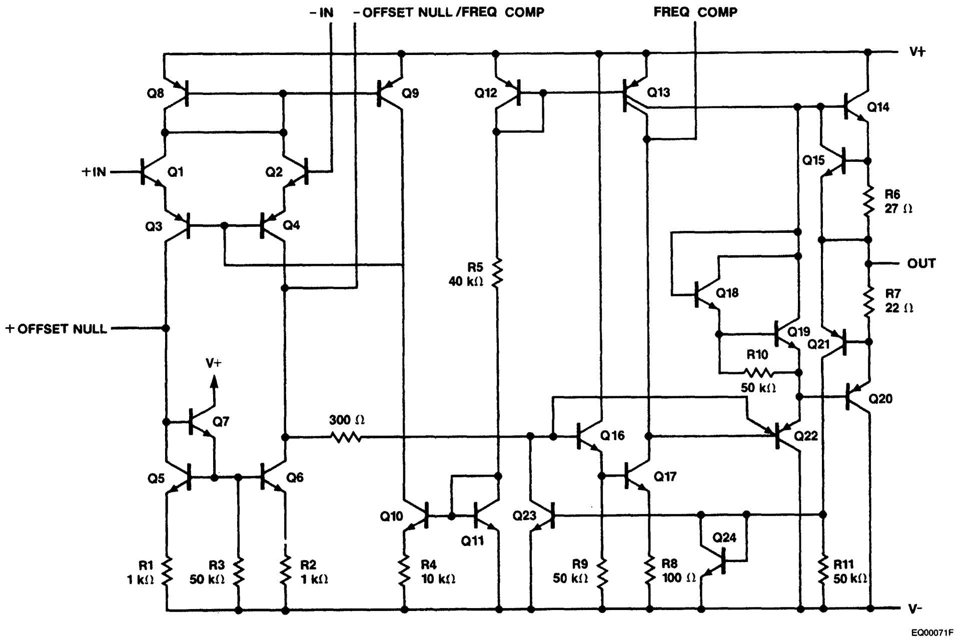
Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA748RC	6T	Ceramic DIP
μA748SC	KC	Molded Surface Mount
μA748TC	9T	Molded DIP

Equivalent Circuit



μA748

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, $C_C = 30$ pF, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				±15		mV
I_{IO}	Input Offset Current				20	200	nA
I_{IB}	Input Bias Current				80	500	nA
Z_I	Input Impedance			0.3	2.0		MΩ
I_{CC}	Supply Current				1.9	2.8	mA
P_c	Power Consumption				60	85	mW
I_{OS}	Output Short Circuit Current				25		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	50	150		V/mV
TR	Transient Response	Rise time	$V_I = 20$ mV, $C_C = 30$ pF, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.3		μs
		Overshoot			5.0		%
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$		0.5		V/μs
			$R_L = 2.0$ kΩ, $C_C = 3.5$ pF, $A_V = 10$		5.5		
The following specifications apply for $-55°C \leq T_A \leq 125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
I_{IO}	Input Offset Current		$T_A = T_{A\ Max}$		10	200	nA
			$T_A = T_{A\ Min}$		50	500	
I_{IB}	Input Bias Current		$T_A = T_{A\ Max}$		0.03	0.5	μA
			$T_A = T_{A\ Min}$		0.3	1.5	
I_{CC}	Supply Current		$T_A = T_{A\ Max}$		1.5	2.5	mA
			$T_A = T_{A\ Min}$		2.0	3.3	
P_c	Power Consumption		$T_A = T_{A\ Max}$		45	75	mW
			$T_A = T_{A\ Min}$		60	100	
CMR	Common Mode Rejection		$R_S \leq 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range			±12	±13		V
PSRR	Power Supply Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
A_{VS}	Large Signal Voltage Gain		$R_L \geq 2.0$ kΩ, $V_O = \pm 10$ V	25			V/mV
V_{OP}	Output Swing		$R_L = 10$ kΩ	±12	±14		V
			$R_L = 2.0$ kΩ	±10	±13		

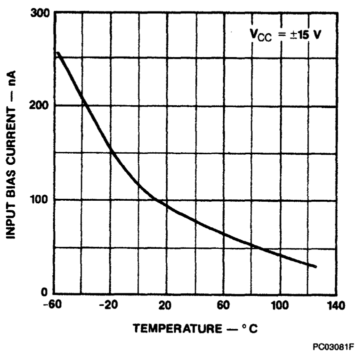
μA748C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, $C_C = 30$ pF, unless otherwise specified.

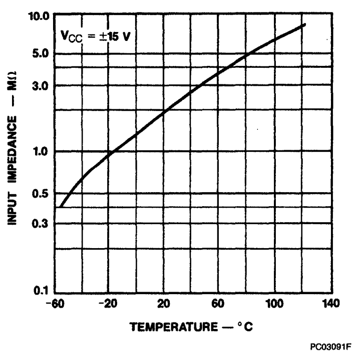
Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		2.0	6.0	mV
I_{IO}	Input Offset Current				20	200	nA
I_{IB}	Input Bias Current				80	500	nA
Z_I	Input Impedance			0.3	2.0		MΩ
I_{CC}	Supply Current				1.9	2.8	mA
P_c	Power Consumption				60	85	mW
I_{OS}	Output Short Circuit Current				25		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	20	150		V/mV
TR	Transient Response	Rise time	$V_I = 20$ mV, $C_C = 30$ pF, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.3		μs
		Overshoot			5.0		%
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$		0.5		V/μs
The following specifications apply for $0°C \leqslant T_A \leqslant 70°C$							
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		2.0	7.5	mV
I_{IO}	Input Offset Current		$T_A = T_{A\ Max}$			300	nA
			$T_A = T_{A\ Min}$			800	μA
I_{CC}	Supply Current		$T_A = T_{A\ Max}$		1.5	2.5	mA
			$T_A = T_{A\ Min}$		2.0	3.3	
P_c	Power Consumption		$T_A = T_{A\ Max}$		45	75	mW
			$T_A = T_{A\ Min}$		60	100	
CMR	Common Mode Rejection		$R_S \leqslant 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range			±12	±13		V
PSRR	Power Supply Rejection Ratio		$R_S \leqslant 10$ kΩ		30	150	μV/V
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 2.0$ kΩ, $V_O = \pm 10$ V	15			V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12	±14		V
			$R_L = 2.0$ kΩ	±10	±13		

Typical Performance Curves for μA748

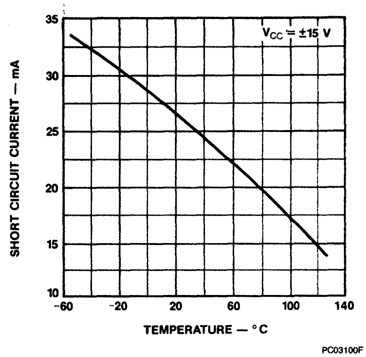
Input Bias Current vs Temperature



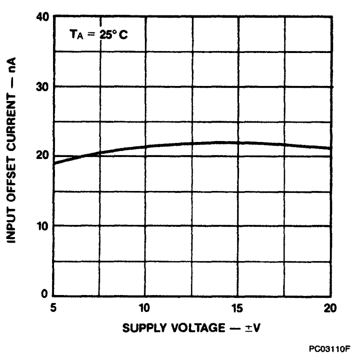
Input Impedance vs Temperature



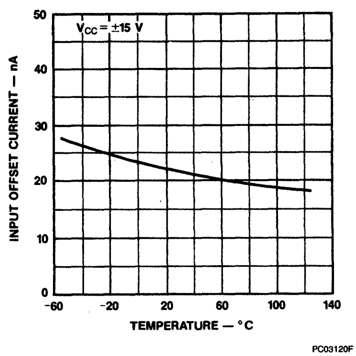
Short Circuit Current vs Temperature



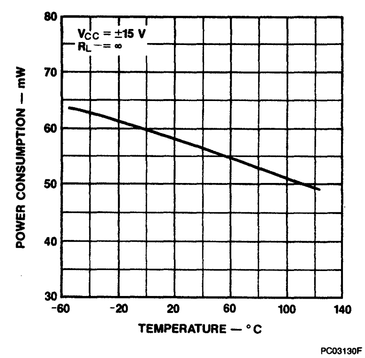
Input Offset Current vs Supply Voltage



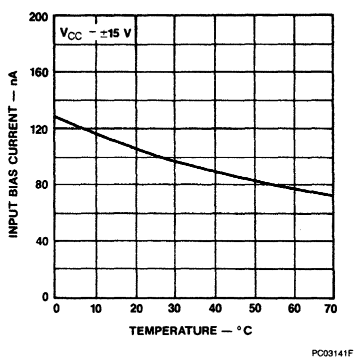
Input Offset Current vs Temperature



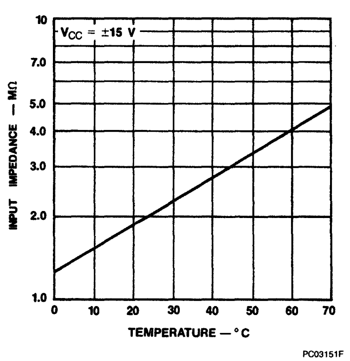
Power Consumption vs Temperature



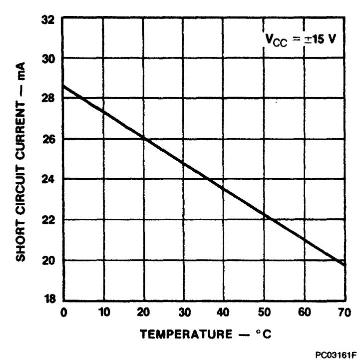
Input Bias Current vs Temperature for μA748C



Input Impedance vs Temperature for μA748C

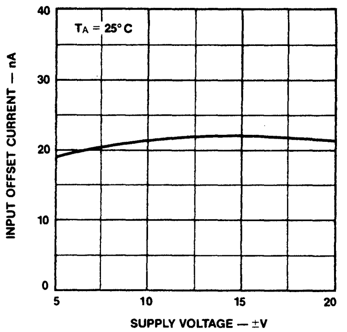


Short Circuit Current vs Temperature for μA748C



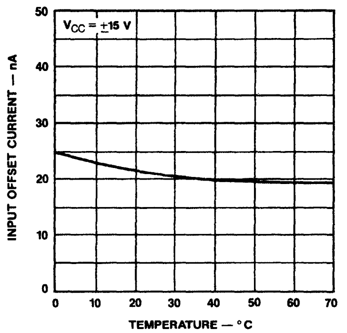
Typical Performance Curves for μA748 and μA748C (Cont.)

Input Offset Current vs Supply Voltage for μA748C



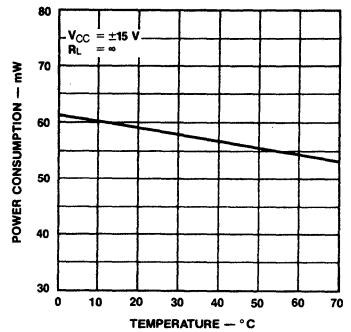
PC03170F

Input Offset Current vs Temperature for μA748C



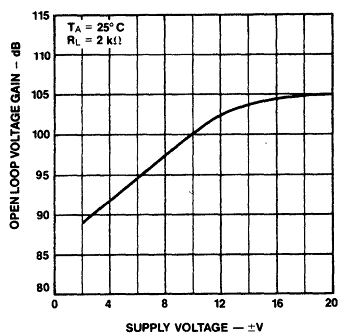
PC03181F

Power Consumption vs Temperature for μA748C



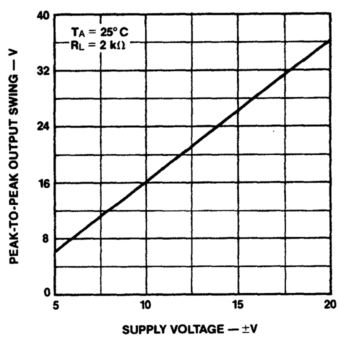
PC03190F

Voltage Gain vs Supply Voltage



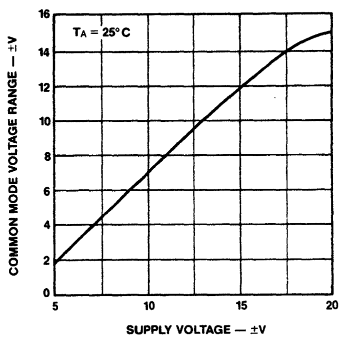
PC03200F

Output Voltage Swing vs Supply Voltage



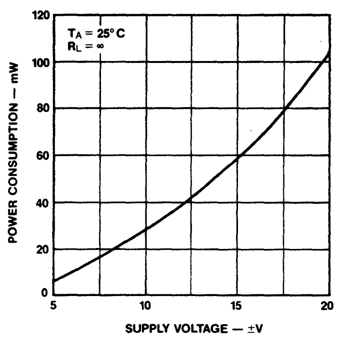
PC03210F

Input Common Mode Voltage Range vs Supply Voltage



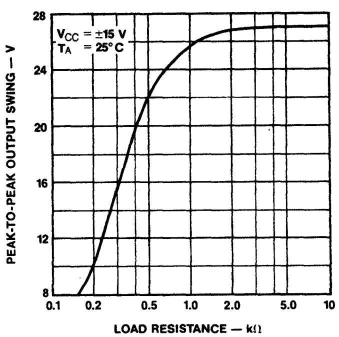
PC03220F

Power Consumption vs Supply Voltage



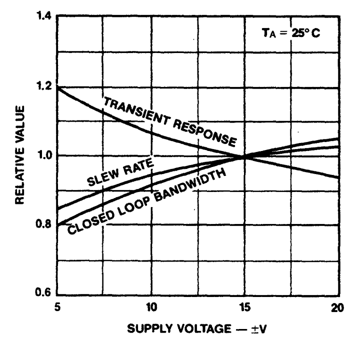
PC03230F

Output Voltage Swing vs Load Resistance



PC03240F

Frequency Characteristics vs Supply Voltage



PC03250F

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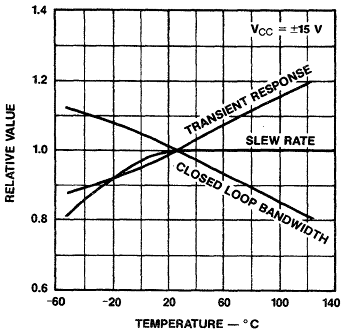
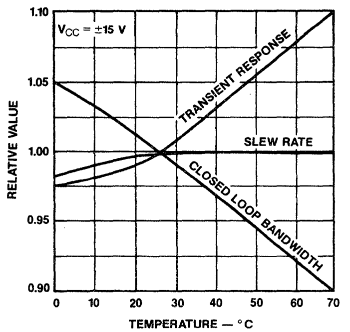
Typical Performance Curves for μA748 and μA748C (Cont.)

Frequency Characteristics vs Temperature for μA748



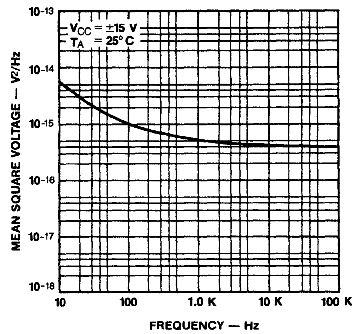
PC03270F

Frequency Characteristics vs Temperature for μA748C



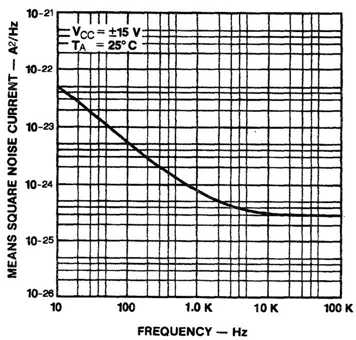
PC03260F

Input Noise Voltage vs Frequency



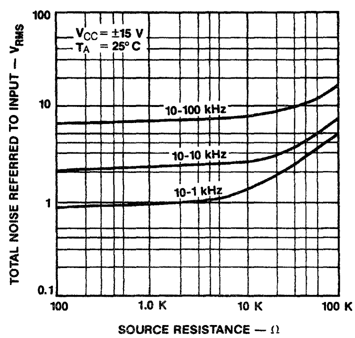
PC03281F

Input Noise Current vs Frequency



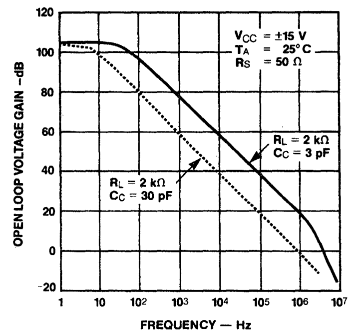
PC03291F

Broadband Noise for Various Bandwidths



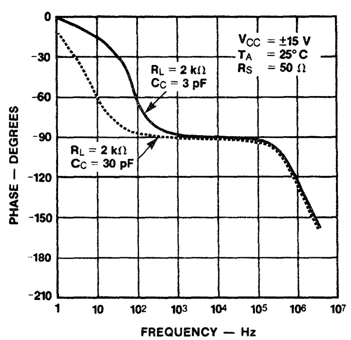
PC03301F

Open Loop Frequency Response for $R_L = 2$ kΩ



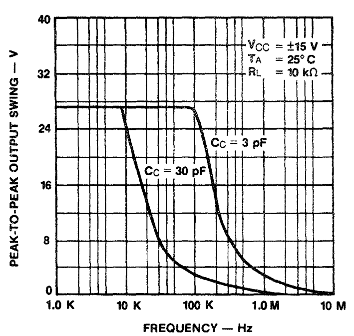
PC03311F

Open Loop Phase Response vs Frequency



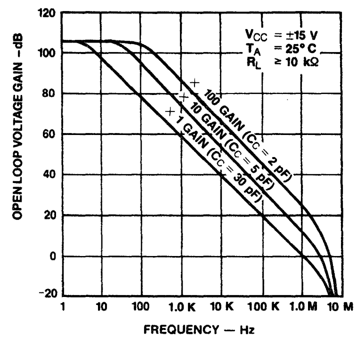
PC03321F

Output Voltage Swing vs Frequency



PC03331F

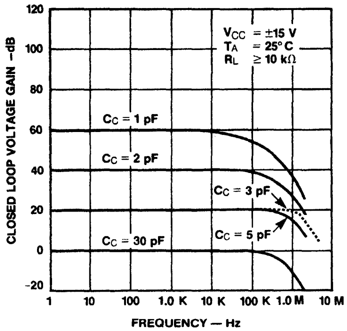
Open Loop Frequency Response for $R_L \geq 10$ kΩ



PC03341F

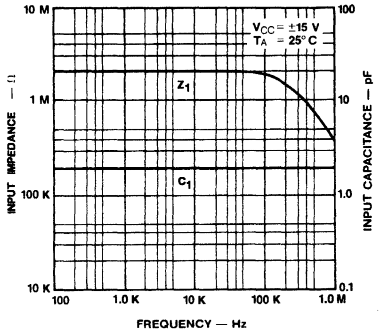
Typical Performance Curves for μA748 and μA748C (Cont.)

Frequency Response for Various Closed Loop Gains



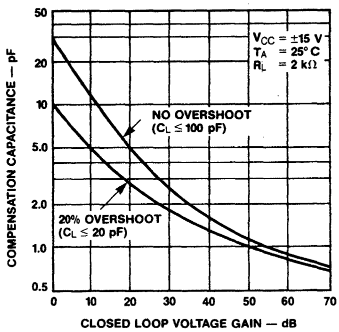
PC03351F

Input Impedance and Input Capacitance vs Frequency



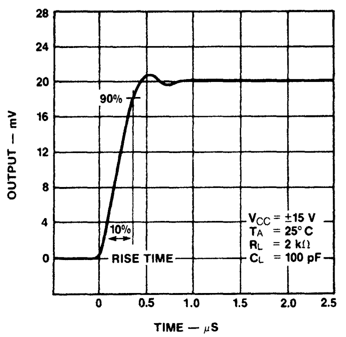
PC03371F

Compensation Capacitance vs Closed Loop Voltage Gain



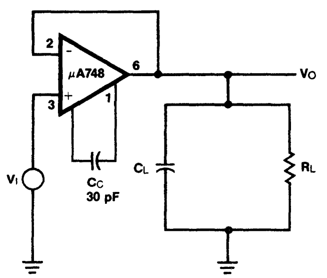
PC03360F

Voltage Follower Transient Response (Gain of 1)



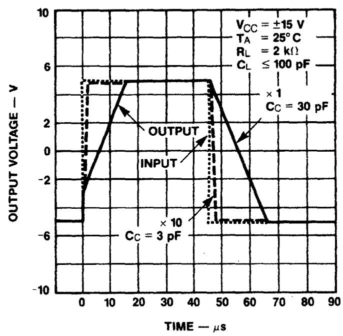
PC03961F

Transient Response Test Circuit



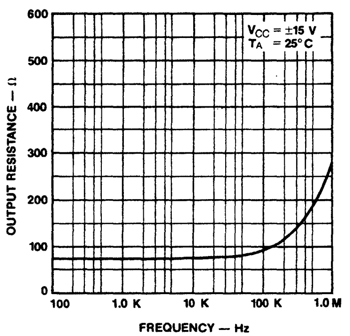
TC00010F

Voltage Follower Large Signal Pulse Response



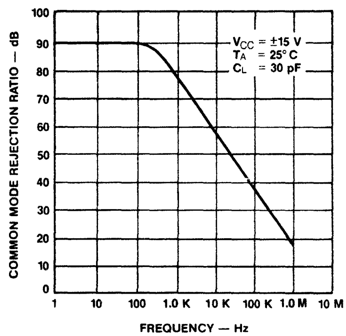
PC03381F

Output Resistance vs Frequency



PC03391F

Common Mode Rejection Ratio vs Frequency

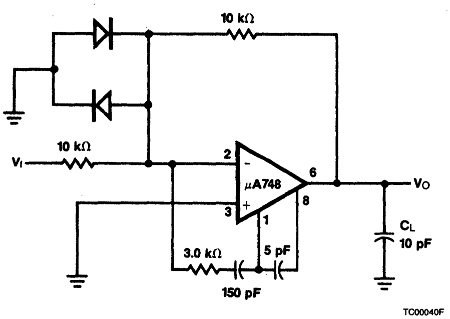


PC03401F

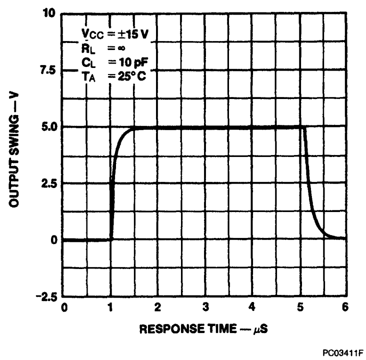
7

Test Circuits

Feed Forward Compensation

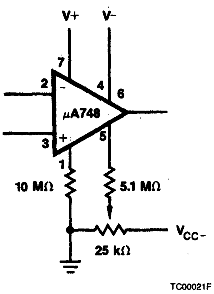


Large Signal Feed Forward Transient Response

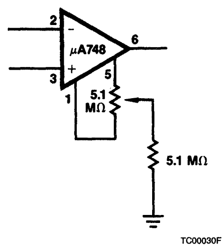


Voltage Offset Null Circuit

Suggested

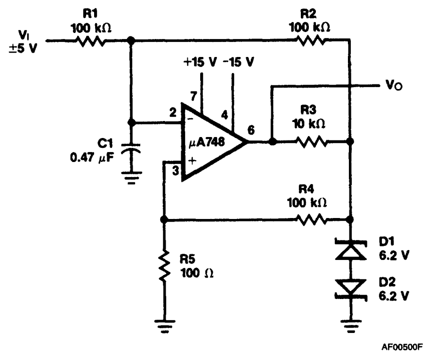


Alternate

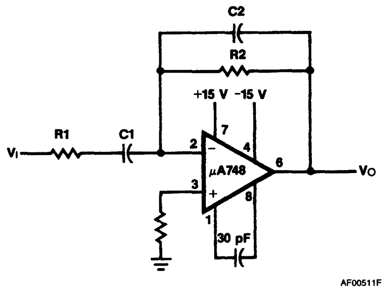


Typical Applications

Pulse Width Modulator



Practical Differentiator

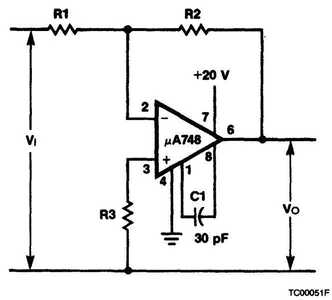


$$f_c = \frac{1}{2\pi\ R2\ C1}$$

$$f_h = \frac{1}{2\pi\ R1\ C1} = \frac{1}{2\pi\ R2\ C2}$$

$$f_c < f_h < f_{unity\ gain}$$

Circuit for Operating the μA748 Without a Negative Supply



μA759 • μA77000 Power Operational Amplifiers

Description

The μA759 and μA77000 are high performance monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. The μA759 provides 325 mA and the μA77000 provides 250 mA output current and feature small signal characteristics better than the μA741. The amplifiers are designed to operate from a single or dual power supply with the input common mode range including the negative supply. The high gain and high output power provide superior performance whenever an operational amplifier is needed. The μA759 and μA77000 employ internal current limiting, thermal shutdown, and safe-area compensation making them essentially indestructible. These amplifiers are intended for a wide range of applications including voltage regulators, audio amplifiers, servo amplifiers, and power drivers.

- **Output Current**
  - **μA759 — 325 mA Minimum**
  - **μA77000 — 250 mA Minimum**
- **Internal Short Circuit Current Limiting**
- **Internal Thermal Overload Protection**
- **Internal Output Transistors Safe-Area Protection**
- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**

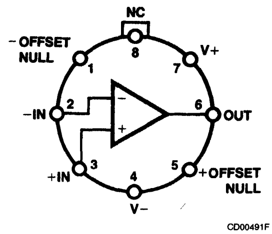
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Power Watt	-65°C to +150°C
Operating Junction Temperature Range	
Extended (μA759M)	-55 to +150°C
Commercial (μA759C, μA77000C)	0°C to +125°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Power Watt (soldering, 10 s)	265°C
Internal Power Dissipation[1]	Internally Limited
Supply Voltage	±18 V
Differential Input Voltage	30 V
Input Voltage[2]	±15 V

Notes

1. Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the Electrical Characteristics Table.
2. For a supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

Connection Diagram
8-Lead Metal Package
(Top View)

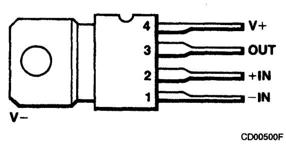


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA759HM	5W	Metal
μA759HC	5W	Metal

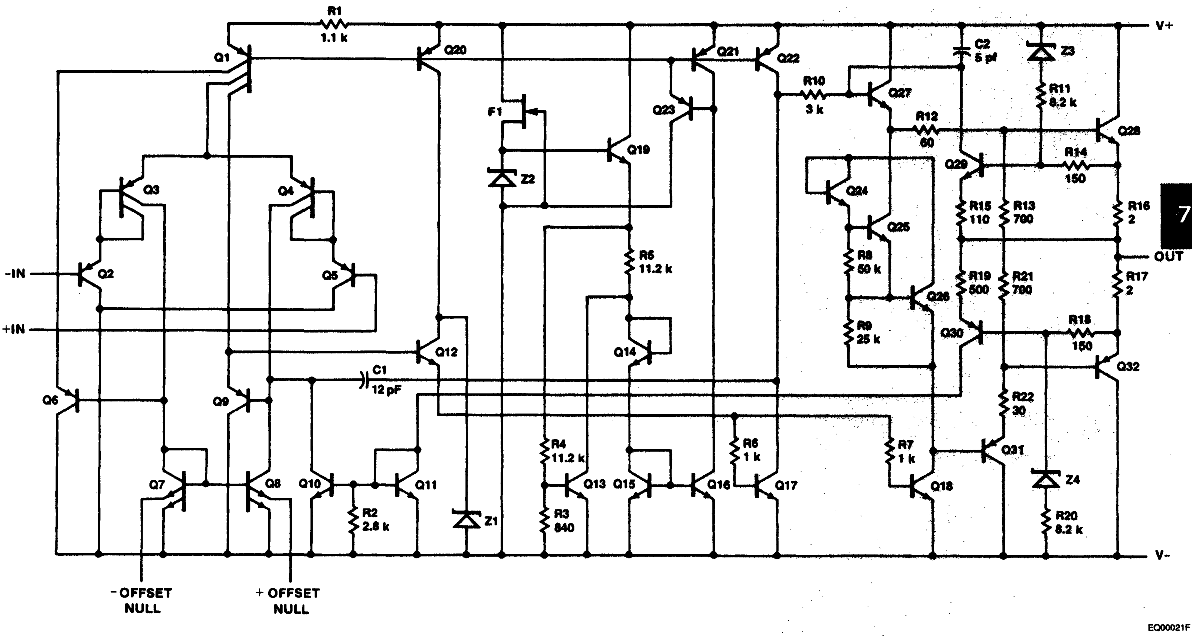
Connection Diagram
TO-202 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA759U1C	8Z	Power Watt
μA77000U1C	8Z	Power Watt

Equivalent Circuit



Note
All resistor values in ohms.

7

μA759

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ		1.0	3.0	mV
I_{IO}	Input Offset Current				5.0	30	nA
I_{IB}	Input Bias Current				50	150	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			+13 to V−	+13 to V−		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC} - V_O \rvert = 30$ V		± 200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0\ V \leqslant \lvert V_{CC} - V_O \rvert \leqslant 10$ V	± 325	± 500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 50$ Ω, $V_O = \pm 10$ V	50	200		V/mV
TR	Transient Response	Rise time	$R_L = 50$ Ω, $A_V = 1.0$		300		ns
		Overshoot			5.0		%
SR	Slew Rate		$R_L = 50$ Ω, $A_V = 1.0$		0.6		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $-55°C \leqslant T_J \leqslant +150°C$							
V_{IO}	Input Offset Voltage		$R_S \leqslant 10$ kΩ			4.5	mV
I_{IO}	Input Offset Current					60	nA
I_{IB}	Input Bias Current					300	nA
CMR	Common Mode Rejection		$R_S \leqslant 10$ kΩ	80	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leqslant 10$ kΩ	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geqslant 50$ Ω, $V_O = \pm 10$ V	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50$ Ω	± 10	± 12.5		V

μA759C

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			+13 to V−	+13 to V−		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC} - V_O \rvert = 30$ V		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0\ V \leq \lvert V_{CC} - V_O \rvert \leq 10$ V	±325	±500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_O = \pm 10$ V	25	200		V/mV
TR	Transient Response	Rise time	$R_L = 50$ Ω, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50$ Ω, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ			7.5	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMR	Common Mode Rejection		$R_S \leq 10$ kΩ	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_O = \pm 10$ V	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50$ Ω	±10	±12.5		V

7

μA77000

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	8.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			+13 to V−	+13 to V−		V
I_{OS}	Output Short Circuit Current		$\|V_{CC} - V_O\| = 30$ V		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0\ V \leq \|V_{CC} - V_O\| \leq 10$ V	±250	±400		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_O = \pm 10$ V	25	200		V/mV
TR	Transient Response	Rise time	$R_L = 50$ Ω, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50$ Ω, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ			10	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMR	Common Mode Rejection		$R_S \leq 10$ kΩ	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10$ kΩ	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50$ Ω, $V_O = \pm 10$ V	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50$ Ω	±10	±12.5		V

Package	Typ	Max	Typ	Max
	θ_{JC} °C/W	θ_{JC} °C/W	θ_{JA} °C/W	θ_{JA} °C/W
Power Watt (U1)	8.0	12	75	80
Metal Can (H)	30	40	120	150

$$P_{D\,Max} = \frac{T_{J\ Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\ Max} - T_A}{\theta_{JA}} \text{ (Without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D\theta_{JA} \text{ (Without a heat sink)}$$

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction to ambient thermal resistance
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case to ambient thermal resistance
- θ_{CS} = Case to heat sink thermal resistance
- θ_{SA} = Heat sink to ambient thermal resistance

Mounting Hints

Metal Can Package (μA759HC/μA759HM)

The μA759 in the 8-Lead TO-99 metal can package must be used with a heat sink. With ± 15 V power supplies, the μA759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the μA759 is internally connected to the negative power supply terminal.

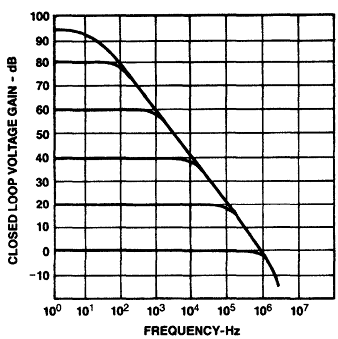
Power Watt Package (μA759U1C/μA77000U1C)

The μA759U1C and μA77000U1C are designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

7

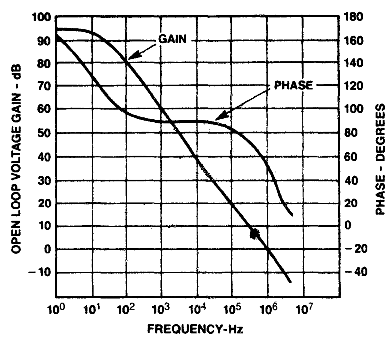
Typical Performance Curves

Frequency Response For Various Closed Loop Gains



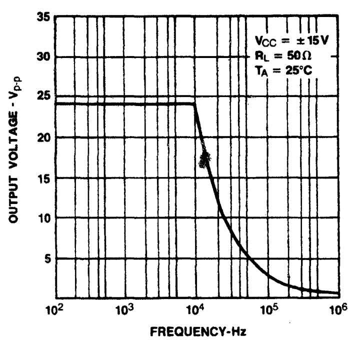
PC02471F

Open Loop vs Frequency Response



PC02480F

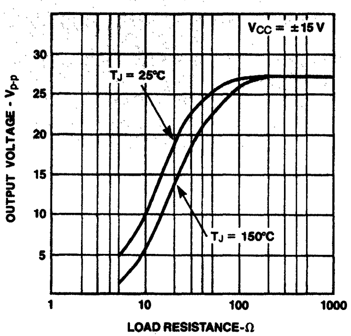
Output Voltage vs Frequency



PC02491F

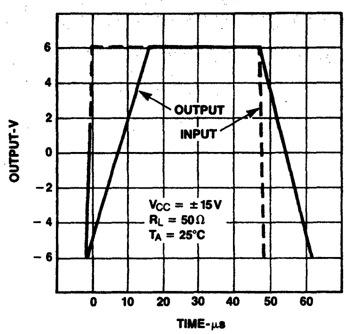
Typical Performance Curves (Cont.)

Output Voltage vs Load Resistance



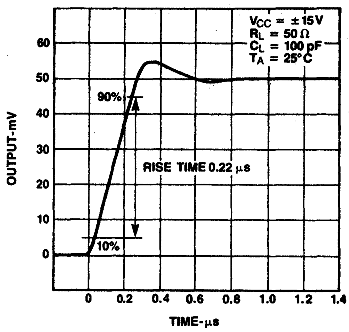
PC02501F

Voltage Follower Large Signal Pulse Response



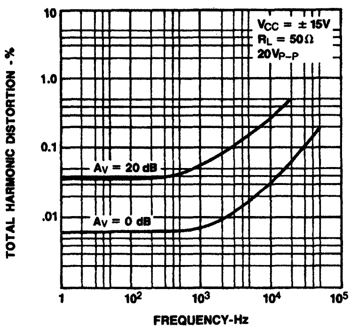
PC02510F

Voltage Follower Transient Response



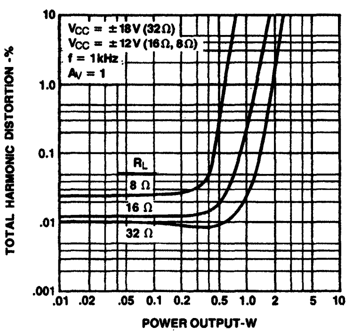
PC02520F

Total Harmonic Distortion vs Frequency



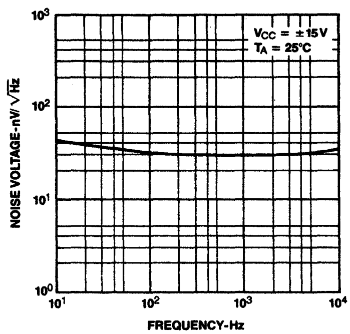
PC02531F

Total Harmonic Distortion vs Power Output



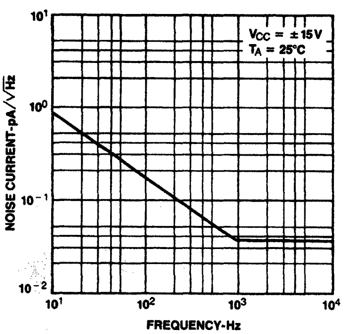
PC02541F

Input Noise Voltage vs Frequency



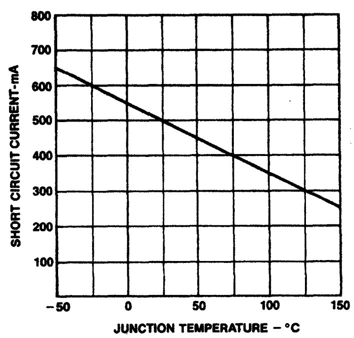
PC02550F

Noise Current vs Frequency



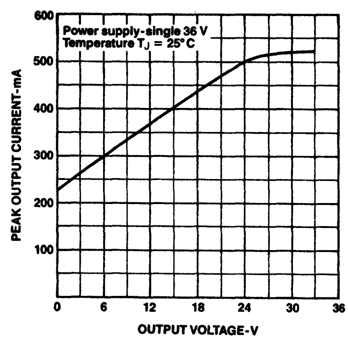
PC02561F

Short Circuit Current vs Junction Temperature



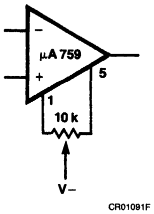
PC02571F

Peak Output Current vs Output Voltage

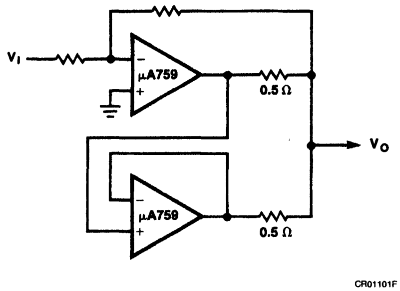


PC02580F

Offset Null Circuit



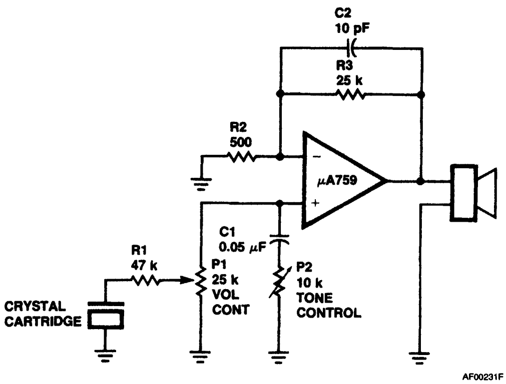
Paralleling μA759 Power Op Amps



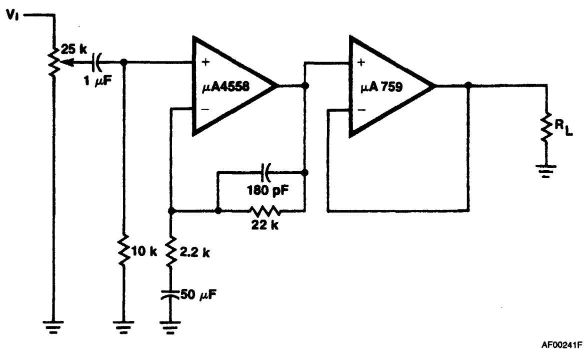
Speaker Impedance (ohms)	Output Power (watts)	Min Supply (volts)	V_{Op-p} (volts)
4	.18	9	2.4
8	.36	12	4.8
16	.72	15	9.6
32	1.44	25	19.2

Audio Applications

Low Cost Phono Amplifier



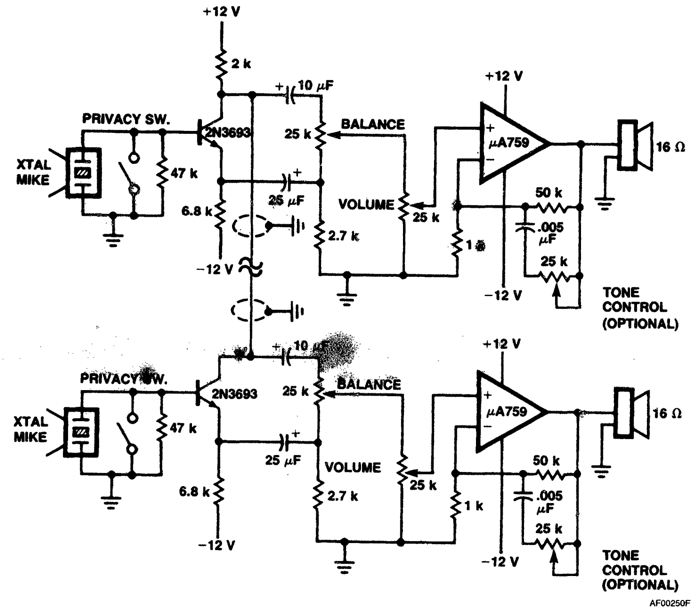
Headphone Amplifier



Note
1. All resistor values in ohms.

7

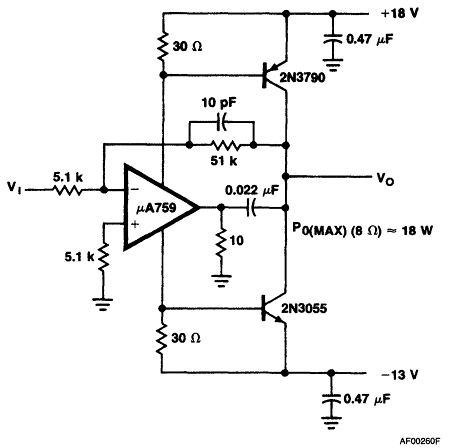
Bi-Directional Intercom System Using the μA759 Power Op Amp



Features
Circuit Simplicity
1 Watt of Audio Output
Duplex operation with only one two-wire cable as interconnect.

Note
1. All resistor values in ohms.

High Slew Rate Power OP Amp/Audio Amp

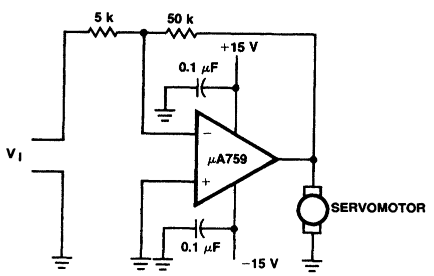


Features
High Slew Rate 9 V/μs
High 3 dB Power Bandwidth 85 kHz
18 Watts Output Power Into an 8 Ω Load.
Low Distortion — .2%, 10 VRMS, 1 kHz Into 8 Ω

Design Consideration
$A_V \geqslant 10$

Servo Applications

DC Servo Amplifiers

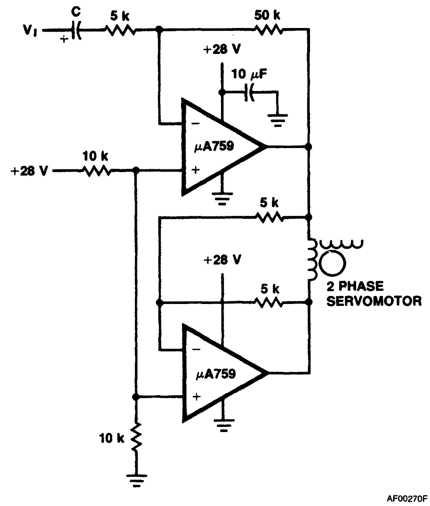


Features
Circuit Simplicity
One Chip Means Excellent Reliability

Design Considerations
$I_O \leqslant 325$ mA

Note
1. All resistor values in ohms.

AG Servo Amplifier - Bridge Type



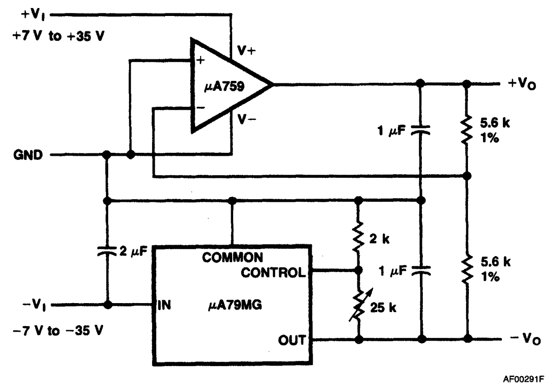
Features
Gain of 10
Use of μA759 Means Simple Inexpensive Circuit

Design Considerations
325 mA Max Output Current

7

Regulator Applications

Adjustable Dual Tracking Regulator

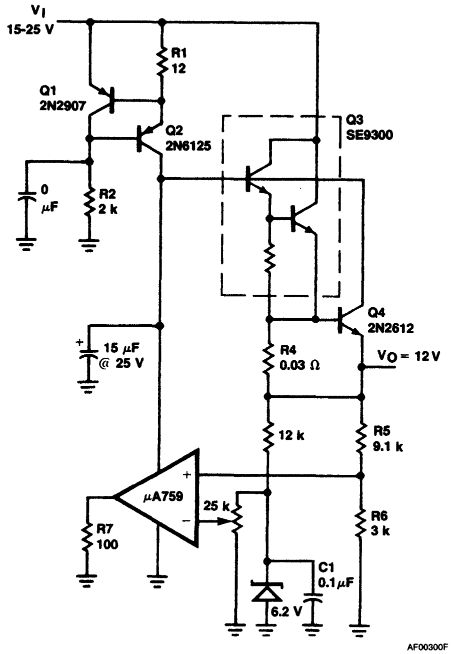


Features
Wide Output Voltage Range (±2.2 to ±30 V)
Excellent Load Regulation $\Delta V_O < \pm 5$ mV for $\Delta I_O = \pm 0.2$ A
Excellent Line Regulation $\Delta V_O < \pm 2$ mV for $\Delta V_I = 10$ V

Note
1. All resistor values in ohms.

Regulator Applications (Cont.)

10 Amp – 12 Volt Regulator



Features
Excellent Load and Line Regulation
Excellent Temperature Coefficient-Depends
Largely on Tempco of the Reference Zener

Note
1. All resistor values in ohms.

FAIRCHILD
A Schlumberger Company

μA771
Operational Amplifier

Description

This monolithic JFET Input Operational Amplifier incorporates well matched ion implanted JFETs on the same chip with standard bipolar transistors. The key features of this op amp are low input bias current in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

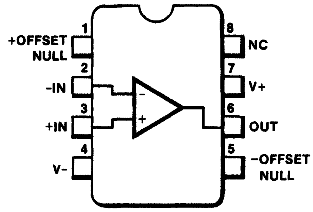
- **Low Input Bias Current — 200 pA**
- **Low Input Offset Current — 100 pA**
- **High Slew Rate — 13 V/μs Typically**
- **Wide Bandwidth — 3.0 MHz Typically**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (μA771AM, μA771BM)	-55°C to +125°C
Commercial (μA771C, μA771AC, μA771BC, μA771LC)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	±18 V
Differential Input Voltage	30 V
Input Voltage[3]	±16 V
Output Short Circuit Duration	Indefinite

Notes
1. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)

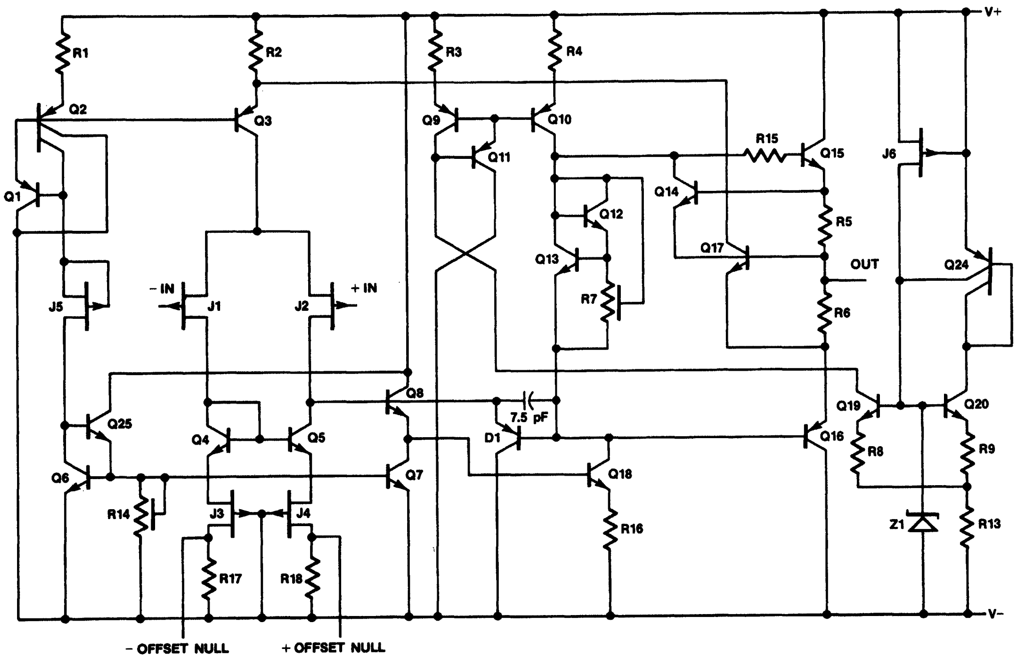


CD00761F

Order Information

Device Code	Package Code	Package Description
μA771RC	6T	Ceramic DIP
μA771SC	KC	Molded Surface Mount
μA771TC	9T	Molded DIP
μA771ARM	6T	Ceramic DIP
μA771ARC	6T	Ceramic DIP
μA771ASC	KC	Molded Surface Mount
μA771ATC	9T	Molded DIP
μA771BRM	6T	Ceramic DIP
μA771BRC	6T	Ceramic DIP
μA771BSC	KC	Molded Surface Mount
μA771BTC	9T	Molded DIP
μA771LRC	6T	Ceramic DIP
μA771LSC	KC	Molded Surface Mount
μA771LTC	9T	Molded DIP

Equivalent Circuit



EQ00051F

μA771 and μA771L
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771 Min	μA771 Typ	μA771 Max	μA771L Min	μA771L Typ	μA771L Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			10.0			15.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			100			100	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	200		50	200	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	50	100		50	100		V/mV
The following specifications apply for $0°C \leq T_A \leq +70°C$, $V_{CC} = \pm 15$ V									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			13			20	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			8.0			8.0	nA
I_{CC}	Supply Current				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	70			70			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	70			70			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μA771A and μA771B
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771A Min	μA771A Typ	μA771A Max	μA771B Min	μA771B Typ	μA771B Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			2.0			5.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			50			50	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	50	100		50	100		V/mV
The following specifications apply for $0°C \leq T_A \leq +70°C$, $V_{CC} = \pm 15$ V									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			4.0			7.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			2.0			2.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{CC}	Supply Current				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	80			80			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μA771AM and μA771BM
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771AM Min	μA771AM Typ	μA771AM Max	μA771BM Min	μA771BM Typ	μA771BM Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ Ω			2.0			5.0	mV
I_{IO}	Input Offset Current	$V_{CM} = 0$ V, $T_J = 25°C$			50			50	pA
I_{IB}	Input Bias Current	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50$ Ω	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ±18 V, $R_S = 50$ Ω	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50			50			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	μA771AM Min	μA771AM Typ	μA771AM Max	μA771BM Min	μA771BM Typ	μA771BM Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ Ω			5.0			8.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50$ Ω		10			10		μV°/C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			20			20	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			50			50	nA
I_{CC}	Supply Current				3.4			3.4	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50$ Ω	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ±18 V, $R_S = 50$ Ω	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μ**A771** (Cont.)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

AC Characteristics

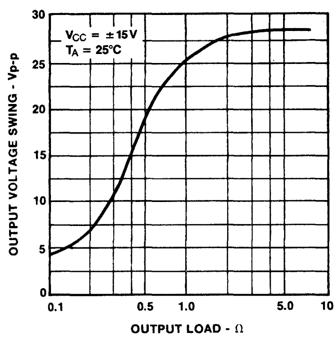
Symbol	Characteristic	Condition	All Grades			Unit
			Min	Typ	Max	
BW	Bandwidth	*(Figure 2)* $A_V = -10$		3.0		MHz
SR	Slew Rate	*(Figure 1)*		13		V/μs
e_n	Input Noise Voltage	$R_S = 100\ \Omega$, f = 1000 Hz		16		nV/$\sqrt{Hz}$
i_n	Input Noise Current	f = 1000 Hz		0.01		pA/$\sqrt{Hz}$

Note

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

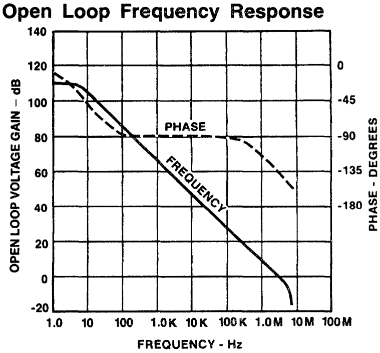
Typical Performance Curves

Output Voltage Swing vs Load Resistance



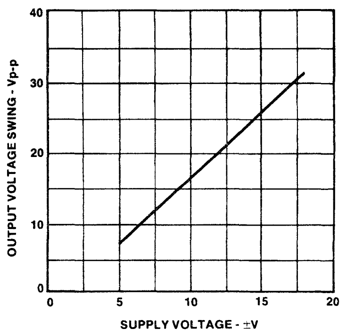
PC02830F

Open Loop Frequency Response



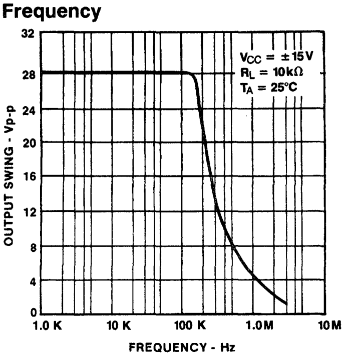
PC02851F

Output Voltage Swing vs Supply Voltage



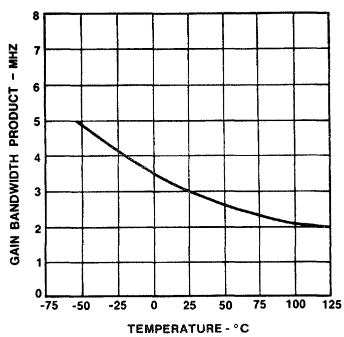
PC02840F

Maximum Undistorted Output vs Frequency



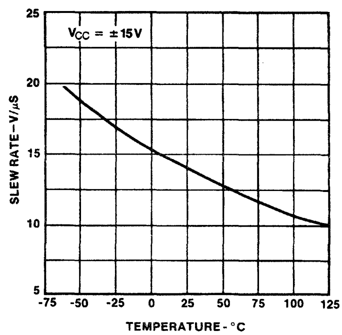
PC02861F

Gain Bandwidth Product vs Temperature



PC02871F

Slew Rate vs Temperature



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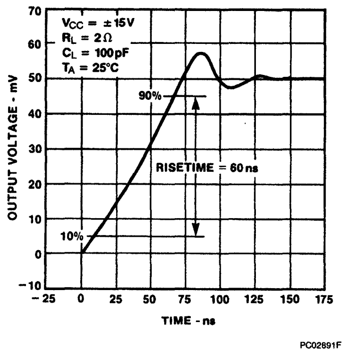
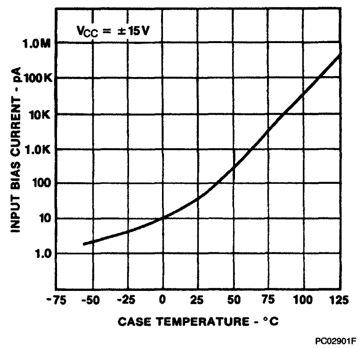
Typical Performance Curves (Cont.)

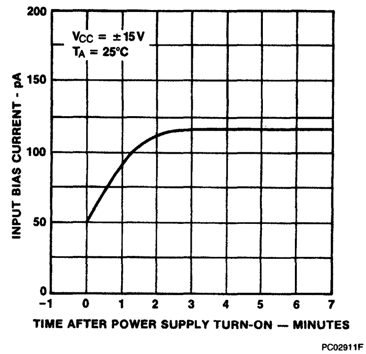
Small Signal Pulse Response



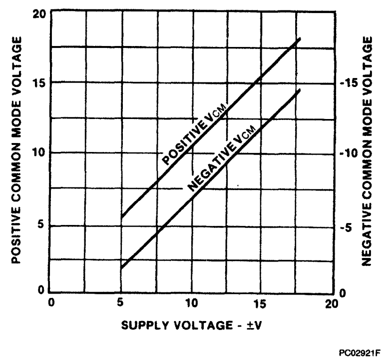
Input Bias Current vs Case Temperature



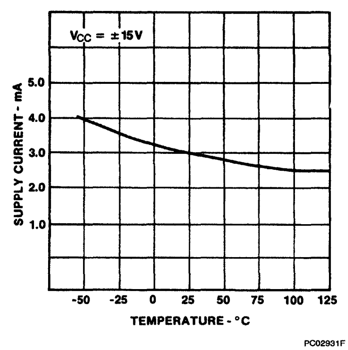
Bias Current Warm up Change



Maximum Common Mode Input Voltage vs Supply Voltage



Supply Current vs Temperature



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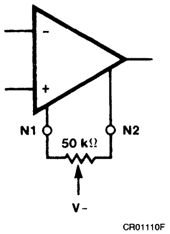
Test Circuit

Input Offset Voltage Null Circuit



Typical Applications

Figure 1 Unity Gain Amplifier

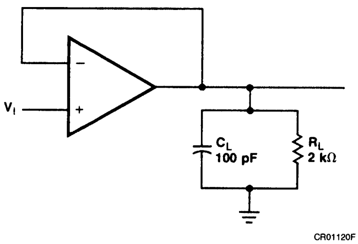
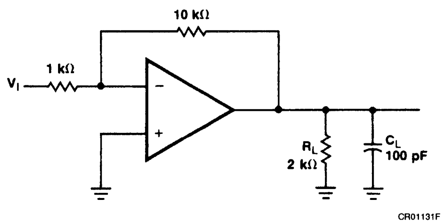


Figure 2 Gain-of-10 Inverting Amplifier



FAIRCHILD

A Schlumberger Company

μA772 Dual Operational Amplifier

Linear Division Operational Amplifiers

Description

This monolithic JFET Input operational amplifier incorporates well matched ion implanted JFETs on the same chip with standard bipolar transistors. The key features of this op amp are low input bias current in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

- **Low Input Bias Current — 200 pA**
- **Low Input Offset Current — 100 pA**
- **High Slew Rate — 13 V/μs Typically**
- **Wide Bandwidth — 3.0 MHz Typically**

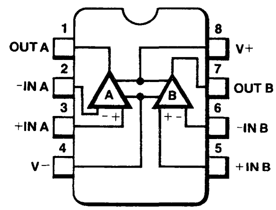
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA772AM, μA772BM)	−55°C to +125°C
Commercial (μA772C, μA772AC, μA772BC, μA772LC)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	±18 V
Differential Input Voltage	30 V
Input Voltage[3]	±16 V
Output Short Circuit Duration	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)

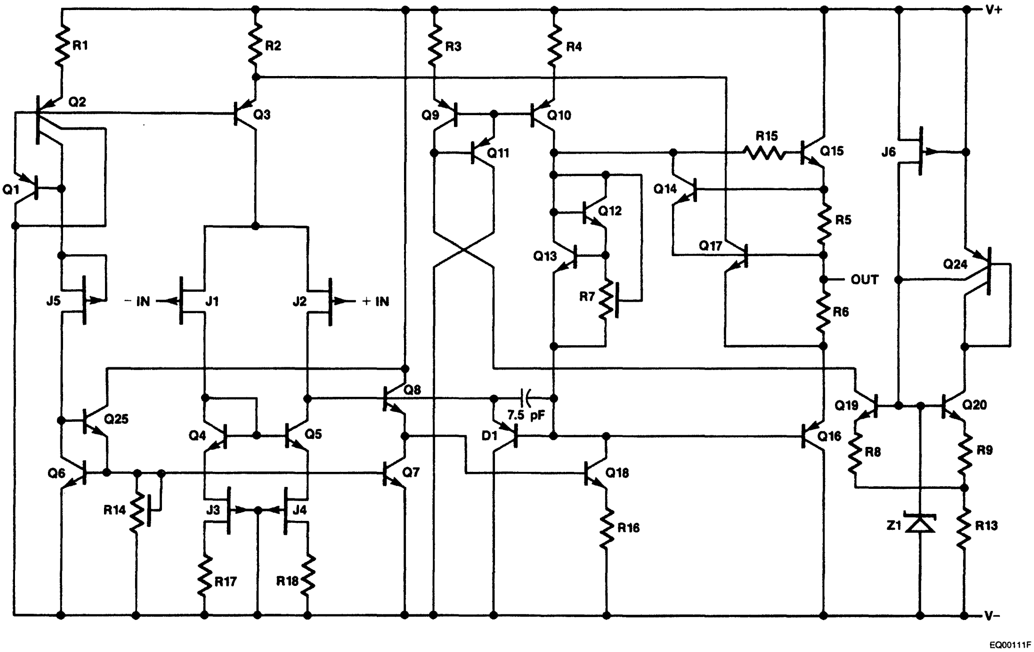


CD00650F

Order Information

Device Code	Package Code	Package Description
μA772RC	6T	Ceramic DIP
μA772SC	KC	Molded Surface Mount
μA772TC	9T	Molded DIP
μA772ARM	6T	Ceramic DIP
μA772ARC	6T	Ceramic DIP
μA772ASC	KC	Molded Surface Mount
μA772ATC	9T	Molded DIP
μA772BRM	6T	Ceramic DIP
μA772BRC	6T	Ceramic DIP
μA772BSC	KC	Molded Surface Mount
μA772BTC	9T	Molded DIP
μA772LRC	6T	Ceramic DIP
μA772LSC	KC	Molded Surface Mount
μA772LTC	9T	Molded DIP

Equivalent Circuit (1/2 of Circuit)



μa772 and μA772L
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA772			μA772L			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			10.0			15.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			100			100	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	200		50	200	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50	100		50	100		V/mV

The following specifications apply for $V_{CC} = \pm 15$ V, $0°C \leqslant T_A \leqslant +70°C$

Symbol	Characteristic	Condition	μA772 Min	μA772 Typ	μA772 Max	μA772L Min	μA772L Typ	μA772L Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			13			20	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			8.0			8.0	nA
I_{CC}	Supply Current (Per Amplifier)				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	70			70			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	70			70			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μA772A and μA772B

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA772A Min	μA772A Typ	μA772A Max	μA772B Min	μA772B Typ	μA772B Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ kΩ			2.0			5.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			50			50	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50	100		50	100		V/mV
The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$, $V_{CC} = \pm 15$ V									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ Ω			4.0			7.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50$ Ω		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			2.0			2.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{CC}	Supply Current (Per Amplifier)				3.0			3.0	mA
CMR	Common Mode Rejection	$R_S = 50$ Ω, $V_{CM} = \pm 11$ V	80			80			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$R_S = 50$ Ω, $V_{CC} = \pm 10$ V to ±18 V	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

µA772AM and µA772BM
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	µA772AM Min	µA772AM Typ	µA772AM Max	µA772BM Min	µA772BM Typ	µA772BM Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			2.0			5.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50			50	pA	
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
V_{IR}	Input Voltage Range		+11	+15		+11	+15		V
			−11	−12		−11	−12		
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	50			50			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			
The following specifications apply for $V_{CC} = \pm 15$ V, $-55°C \leq T_A \leq 125°C$									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S \leq 50\ \Omega$			5.0			8.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		µV°/C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			20			20	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			50			50	nA
I_{CC}	Supply Current (Per Amplifier)				3.4			3.4	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

Electrical Characteristics (Cont.) $V_{CC} = \pm 15$ V, $T_A = 25°C$

AC Characteristics

Symbol	Characteristic	Condition	All Grades			Unit
			Min	Typ	Max	
BW	Bandwidth	*(Figure 2)* $A_V = -10$		3.0		MHz
SR	Slew Rate	*(Figure 1)*		13		V/μs
e_n	Input Noise Voltage	$R_S = 100\ \Omega$, f = 1000 Hz		16		nV/√Hz
i_n	Input Noise Current	f = 1000 Hz		0.01		pA/√Hz

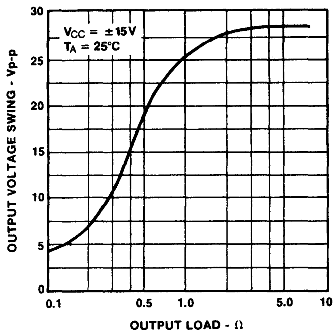
Note

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

7

Typical Performance Curves

Output Voltage Swing vs Load Resistance



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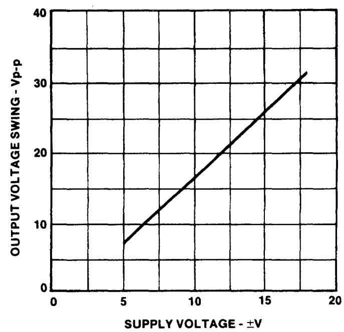
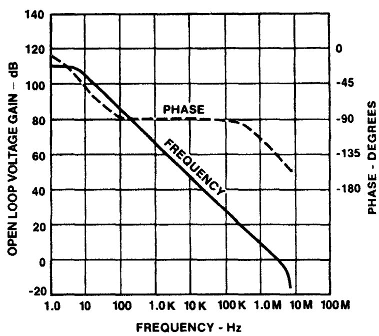
Output Voltage Swing vs Supply Voltage



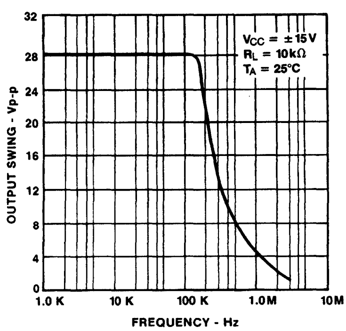
PC02840F

Open Loop Frequency Response



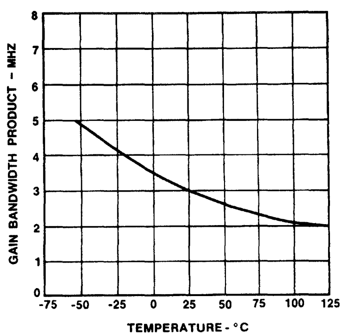
PC02851F

Maximum Undistorted Output vs Frequency



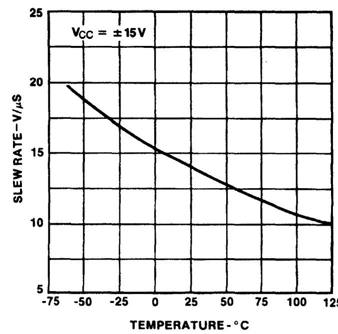
PC02861F

Gain Bandwidth Product vs Temperature



PC02871F

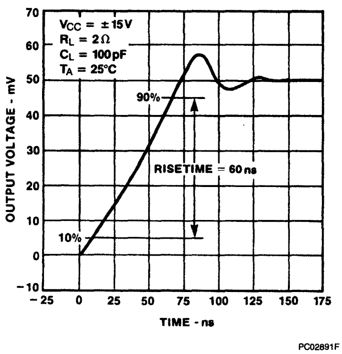
Slew Rate vs Temperature



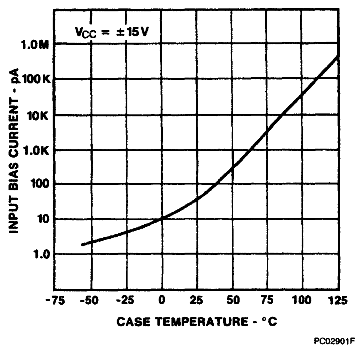
PC02881F

Typical Performance Curves (Cont.)

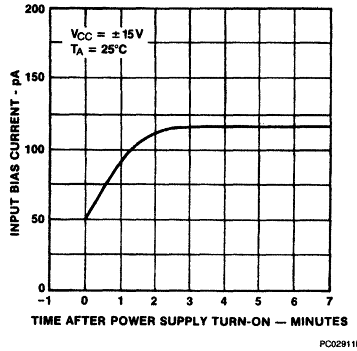
Small Signal Pulse Response



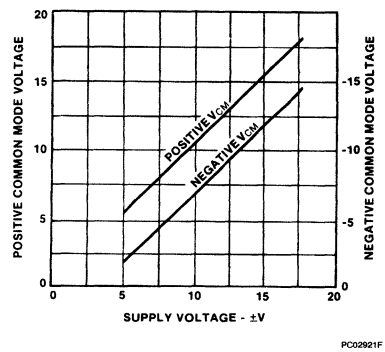
Input Bias Current vs Case Temperature



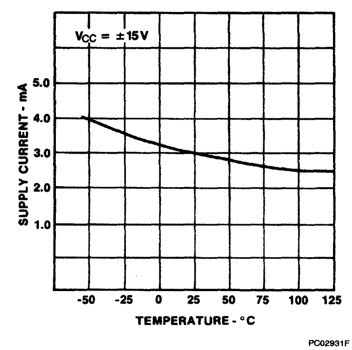
Bias Current Warm up Change



Maximum Common Mode Input Voltage vs Supply Voltage



Supply Current vs Temperature



Typical Applications

Figure 1 Unity Gain Amplifier

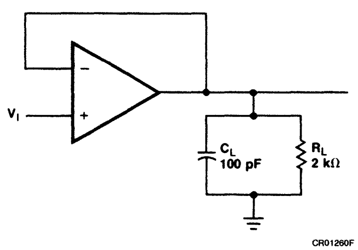
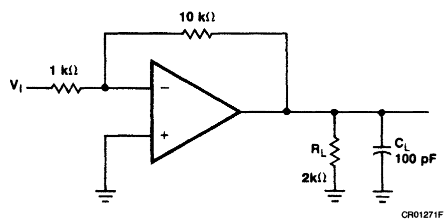


Figure 2 Gain-of-10 Inverting Amplifier



FAIRCHILD

A Schlumberger Company

μA774 Quad Operational Amplifier

Description

This monolithic JFET Input Operational Amplifier incorporates well matched ion implanted JFET on the same chip with standard bipolar transistors. The key features of this op amp are low input bias current in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

- **Low Input Bias Current — 200 pA**
- **Low Input Offset Current — 100 pA**
- **High Slew Rate — 13 V/μs Typically**
- **Wide Bandwidth — 3.0 MHz Typically**

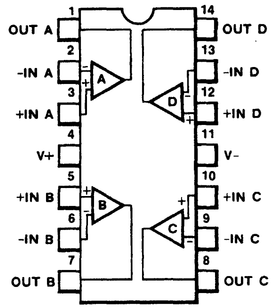
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA774M, μA774BM)	-55°C to +125°C
Commercial (μA774C, μA774BC, μA774LC)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	±18 V
Differential Input Voltage	30 V
Input Voltage[3]	±16 V
Output Short Circuit Duration	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Connection Diagram
4-Lead DIP and SO-14 Package
(Top View)

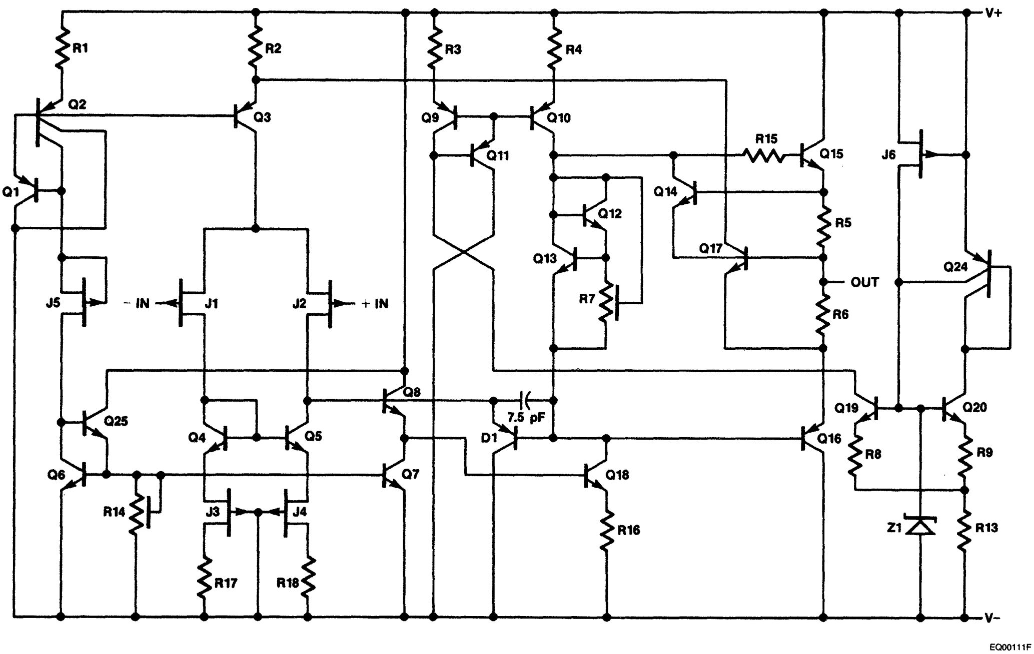


CD00561F

Order Information

Device Code	Package Code	Package Description
μA774DM	7A	Ceramic DIP
μA774DC	7A	Ceramic DIP
μA774PC	9A	Molded DIP
μA774SC	KD	Molded Surface Mount
μA774BDM	7A	Ceramic DIP
μA774BDC	7A	Ceramic DIP
μA774BPC	9A	Molded DIP
μA774LDC	7A	Ceramic DIP
μA774LPC	9A	Molded DIP

Equivalent Circuit (1/4 of Circuit)



μA774, μA774L

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA774			μA774L			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			10.0			15.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			100			100	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	200		50	200	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50	100		50	100		V/mV

The following specifications apply for $0°C \leqslant T_A \leqslant +70°C$, $V_{CC} = \pm 15$ V

Symbol	Characteristic	Condition	μA774 Min	μA774 Typ	μA774 Max	μA774L Min	μA774L Typ	μA774L Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			13			20	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			8.0			8.0	nA
I_{CC}	Supply Current (Per Amplifier)				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	70			70			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	70			70			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μA774A, μA774B
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA774A Min	μA774A Typ	μA774A Max	μA774B Min	μA774B Typ	μA774B Max	Unit
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ kΩ			2.0			5.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			50			50	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	50	100		50	100		V/mV
The following specifications apply for $V_{CC} = \pm 15$ V, $0°C \leqslant T_A \leqslant +70°C$									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50$ Ω			4.0			7.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50$ Ω		10			10		μV/°C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			2.0			2.0	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			4.0			4.0	nA
I_{CC}	Supply Current (Per Amplifier)				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50$ Ω	80			80			dB
V_{IR}	Input Voltage Range		±11	+15 −12		±11	+15 −12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50$ Ω	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geqslant 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

μA774AM, μA774BM
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA774AM			μA774BM			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S = 50\ \Omega$			2.0			5.0	mV
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$			50			50	pA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V, $T_J = 25°C$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current (Per Amplifier)				2.8			2.8	mA
V_{IR}	Input Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	50			50			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			
The following specifications apply for $-55°C \leq T_A \leq +125°C$, $V_{CC} = \pm 15$ V									
V_{IO}	Input Offset Voltage	$V_{CM} = 0$ V, $R_S \leq 50\ \Omega$			5.0			8.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		μV°/C
I_{IO}	Input Offset Current[1]	$V_{CM} = 0$ V			20			20	nA
I_{IB}	Input Bias Current[1]	$V_{CM} = 0$ V			50			50	nA
I_{CC}	Supply Current (Per Amplifier)				3.4			3.4	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11$ V, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10$ V to ± 18 V, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0$ kΩ	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12			±12			V
		$R_L = 2.0$ kΩ	±10			±10			

Electrical Characteristics (Cont.) $T_A = 25°C$, $V_{CC} = \pm 15$ V

AC Characteristics

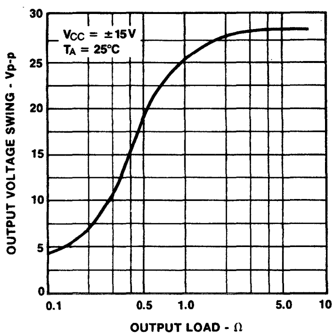
Symbol	Characteristic	Condition	All Grades Min	Typ	Max	Unit
BW	Bandwidth	*(Figure 2)* $A_V = -10$		3.0		MHz
SR	Slew Rate	*(Figure 1)*		13		V/μs
e_n	Input Noise Voltage	$R_S = 100\ \Omega$, f = 1000 Hz		16		nV/√Hz
i_n	Input Noise Current	f = 1000 Hz		0.01		pA/√Hz

Note

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

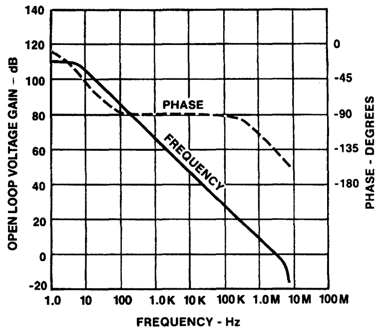
Typical Performance Curves

Output Voltage Swing vs Load Resistance



PC02830F

Open Loop Frequency Response



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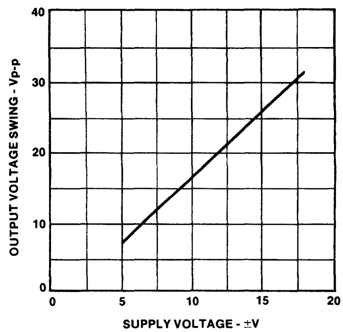
Output Voltage Swing vs Supply Voltage



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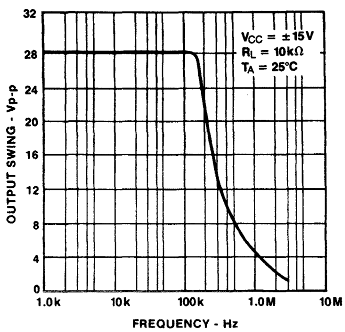
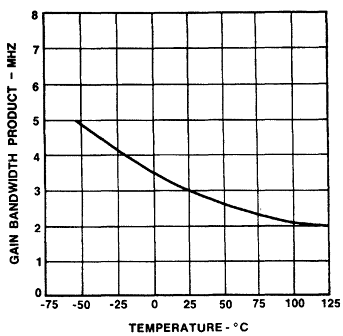
Maximum Undistorted Output vs Frequency



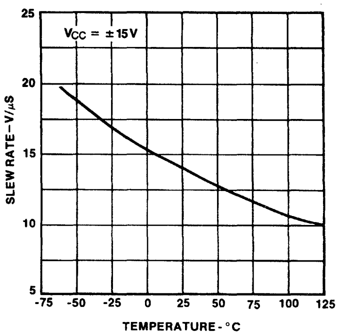
PC02860F

Gain Bandwidth Product vs Temperature



PC02871F

Slew Rate vs Temperature



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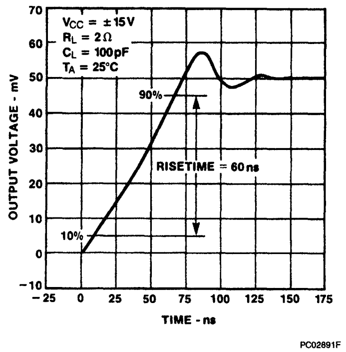
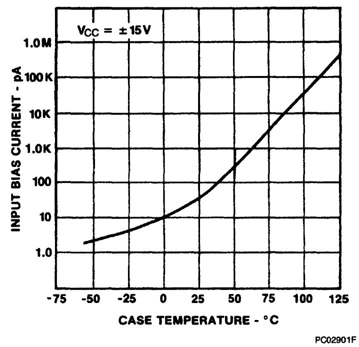
Typical Performance Curves (Cont.)

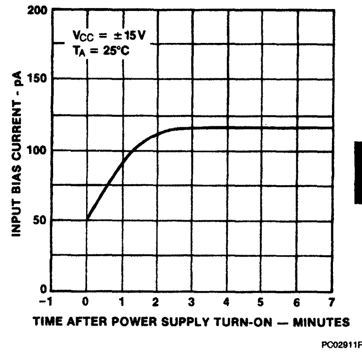
Small Signal Pulse Response



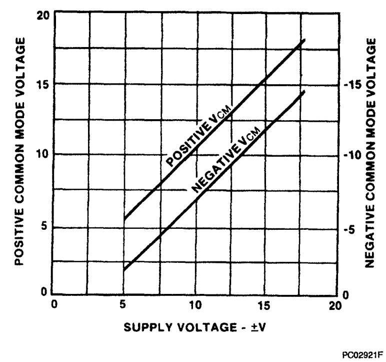
Input Bias Current vs Case Temperature



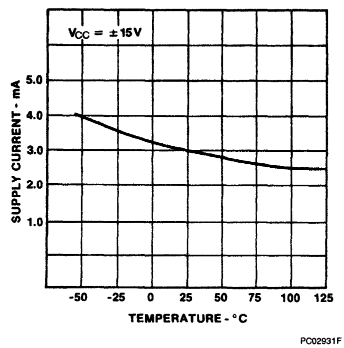
Bias Current Warm Up Change



Maximum Common Mode Input Voltage vs Supply Voltage



Supply Current vs Temperature



Typical Applications

Figure 1 Unity Gain Amplifier

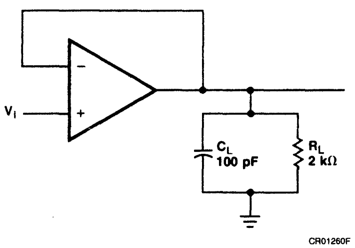
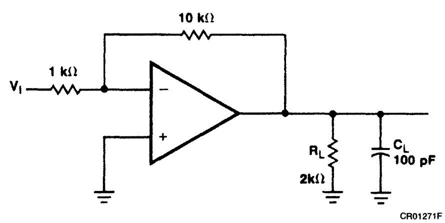


Figure 2 Gain-of-10 Inverting Amplifier



FAIRCHILD

A Schlumberger Company

μA776 Multi-Purpose Programmable Operational Amplifier

Description

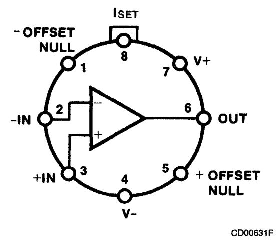
The μA776 Programmable Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input noise voltage and current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch up, high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

- **Micropower Consumption**
- **±1.2 V To ±18 V Operation**
- **No Frequency Compensation Required**
- **Low Input Bias Currents**
- **Wide Programming Range**
- **High Slew Rate**
- **Low Noise**
- **Short Circuit Protection**
- **Offset Null Capability**
- **No Latch Up**

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA776M)	-55°C to +125°C
Commercial (μA776C)	0°C to +70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage[3]	±15 V
Voltage Between Offset Null and V−	±0.5 V
Output Short Circuit Duration[4]	Indefinite
I_{SET} (Maximum Current at I_{SET})	500 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	(V+ −2.0 V) $\leq V_{SET} \leq$ V+

Connection Diagram 8-Lead Metal Package (Top View)

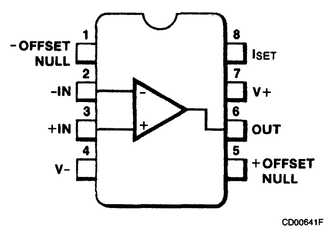


Lead 4 connected to case.

Order Information

Device Code	Package Code	Package Description
μA776HM	5W	Metal
μA776HC	5W	Metal

Connection Diagram 8-Lead DIP (Top View)



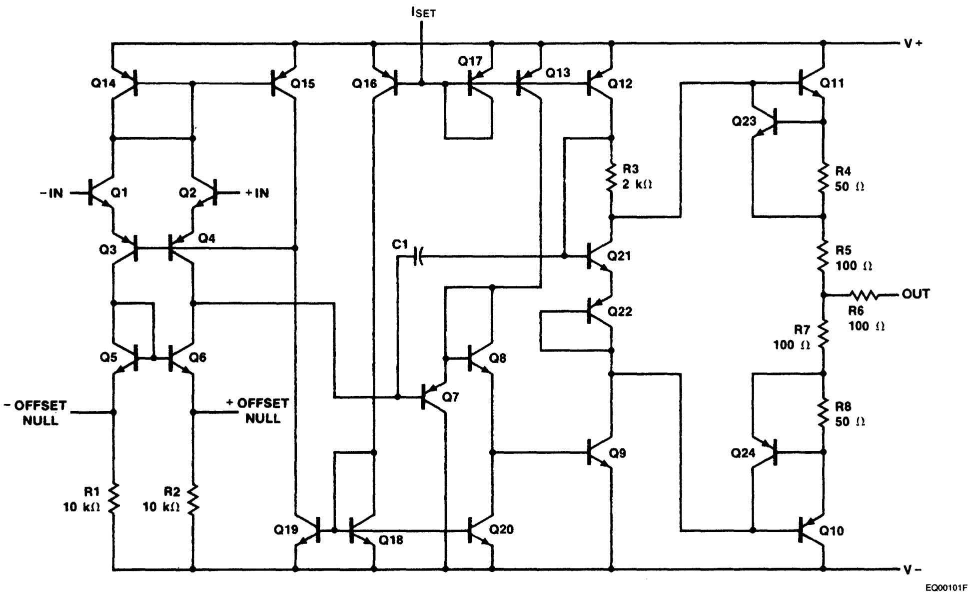
Order Information

Device Code	Package Code	Package Description
μA776TC	9T	Molded DIP

Notes

1. T_J Max = 150°C for the Molded DIP, and 175°C for the Metal Can.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short Circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature for $I_{SET} \leq 30$ μA.

Equivalent Circuit



μA776

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	$I_{SET} = 1.5\mu A$ Min	Typ	Max	$I_{SET} = 15\mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	5.0		2.0	5.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	3.0		2.0	15	nA
I_{IB}	Input Bias Current				2.0	7.5		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				20	25		160	180	μA
P_c	Power Consumption					0.75			5.4	mW
I_{OS}	Output Short Circuit Current				3.0			12		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L \geq 75$ kΩ	200	400					V/mV
			$V_O = \pm 10$ V, $R_L \geq 5.0$ kΩ				100	400		
V_{OP}	Output Voltage Swing		$R_L = 75$ kΩ	±12	±14					V
			$R_L = 5.0$ kΩ				±10	±13		
TR	Transient Response	Rise time	$V_I = 20$ mV, $R_L = 5.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		1.6			0.35		μs
		Overshoot			0			10		%
SR	Slew Rate		$R_L = 5.0$ kΩ, $A_V = 1.0$		0.1			0.8		V/μs

The following specifications apply $-55°C \leq T_A \leq +125°C$

Symbol	Characteristic	Condition	$I_{SET} = 1.5\mu A$ Min	Typ	Max	$I_{SET} = 15\mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			6.0	mV
I_{IO}	Input Offset Current	$T_A = +125°C$			5.0			15	nA
		$T_A = -55°C$			10			40	
I_{IB}	Input Bias Current	$T_A = +125°C$			7.5			50	nA
		$T_A = -55°C$			20			120	
I_{CC}	Supply Current				30			200	μA
P_c	Power Consumption				0.9			6.0	mW
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range		±10			±10			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		25	150		25	150	μV/V
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 75$ kΩ	100			75			V/mV
V_{OP}	Output Voltage Swing	$R_L = 75$ kΩ	±10			±10			V

μA776

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 3.0$ V, unless otherwise specified.

Symbol	Characteristic	Condition	$I_{SET} = 1.5 \mu A$ Min	Typ	Max	$I_{SET} = 15 \mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	5.0		2.0	5.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range			9.0			18		mV
I_{IO}	Input Offset Current			0.7	3.0		2.0	15	nA
I_{IB}	Input Bias Current			2.0	7.5		15	50	nA
Z_I	Input Impedance			50			5.0		MΩ
I_{CC}	Supply Current			13	20		130	160	μA
P_c	Power Consumption			78	120		780	960	μW
I_{OS}	Output Short Circuit Current			3.0			5.0		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 1.0$ V, $R_L \geq 75$ kΩ	50	200					V/mV
		$V_O = \pm 1.0$ V, $R_L \geq 5.0$ kΩ				50	200		
TR	Transient Response: Rise time	$V_I = 20$ mV, $R_L = 5.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		3.0			0.6		μs
	Transient Response: Overshoot			0			5		%
SR	Slew Rate	$R_L = 5.0$ kΩ, $A_V = 1.0$		0.03			0.35		V/μs

The following specifications apply $-55°C \leq T_A \leq +125°C$

Symbol	Characteristic	Condition	$I_{SET} = 1.5 \mu A$ Min	Typ	Max	$I_{SET} = 15 \mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			6.0	mV
I_{IO}	Input Offset Current	$T_A = +125°C$			5.0			15	nA
		$T_A = -55°C$			10			40	nA
I_{IB}	Input Bias Current	$T_A = +125°C$			7.5			50	nA
		$T_A = -55°C$			20			120	
I_{CC}	Supply Current				25			180	μA
P_c	Power Consumption				150			1080	μW
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	86		70	86		dB
V_{IR}	Input Voltage Range		±1.0			±1.0			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		25	150		25	150	μV/V
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 1.0$ V, $R_L \geq 75$ kΩ	25						V/mV
		$V_O = \pm 1.0$ V, $R_L \geq 5.0$ kΩ				25			
V_{OP}	Output Voltage Swing	$R_L = 75$ kΩ	±2.0	±2.4					V
		$R_L = 5.0$ kΩ				±1.9	±2.1		

μA776C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	$I_{SET} = 1.5\mu A$ Min	Typ	Max	$I_{SET} = 15\mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage		$R_S \leq 10$ kΩ		2.0	6.0		2.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range				9.0			18		mV
I_{IO}	Input Offset Current				0.7	6.0		2.0	25	nA
I_{IB}	Input Bias Current				2.0	10		15	50	nA
Z_I	Input Impedance				50			5.0		MΩ
I_{CC}	Supply Current				20	30		160	190	μA
P_c	Power Consumption					0.9			5.7	mW
I_{OS}	Output Short Circuit Current				3.0			12		mA
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L \geq 75$ kΩ	50	400					V/mV
			$V_O = \pm 10$ V, $R_L \geq 5.0$ kΩ				50	400		
V_{OP}	Output Voltage Swing		$R_L = 75$ kΩ	±12	±14					V
			$R_L = 5.0$ kΩ				±10	±13		
TR	Transient Response	Rise time	$V_I = 20$ mV, $R_L \geq 5.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		1.6			0.35		μs
		Overshoot			0			10		%
SR	Slew Rate		$R_L = 5.0$ kΩ, $A_V = 1.0$		0.1			0.8		V/μs

The following specifications apply $0°C \leq T_A \leq +70°C$

Symbol	Characteristic	Condition	$I_{SET} = 1.5\mu A$ Min	Typ	Max	$I_{SET} = 15\mu A$ Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			7.5	mV
I_{IO}	Input Offset Current	$T_A = 70°C$			6.0			25	nA
		$T_A = 0°C$			10			40	
I_{IB}	Input Bias Current	$T_A = 70°C$			10			50	nA
		$T_A = 0°C$			20			100	
I_{CC}	Supply Current				35			200	μA
P_c	Power Consumption				1.05			6.0	mW
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range		±10			±10			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		25	200		25	200	μV/V
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 75$ kΩ	50			50			V/mV
V_{OP}	Output Voltage Swing	$R_L = 75$ kΩ	±10			±10			V

µA776C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 3.0$ V, unless otherwise specified.

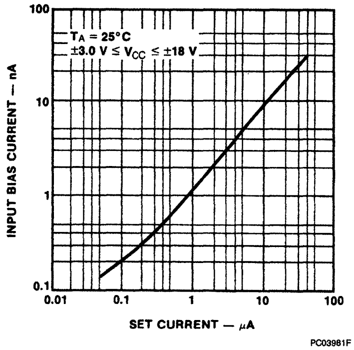
Symbol	Characteristic	Condition	$I_{SET} = 1.5\mu A$ Min	$I_{SET} = 1.5\mu A$ Typ	$I_{SET} = 1.5\mu A$ Max	$I_{SET} = 15\mu A$ Min	$I_{SET} = 15\mu A$ Typ	$I_{SET} = 15\mu A$ Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		2.0	6.0	mV
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range			9.0			18		mV
I_{IO}	Input Offset Current			0.7	6.0		2.0	25	nA
I_{IB}	Input Bias Current			2.0	10		15	50	nA
Z_I	Input Impedance			50			5.0		MΩ
I_{CC}	Supply Current			13	20		130	170	µA
P_c	Power Consumption			78	120		780	1020	µW
I_{OS}	Output Short Circuit Current			3.0			5.0		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 1.0$ V, $R_L \geq 75$ kΩ	25	200					V/mV
		$V_O = \pm 1.0$ V, $R_L \geq 5.0$ kΩ				25	200		
TR	Transient Response — Rise time	$V_I = 20$ mV, $R_L \geq 5.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		3.0			0.6		µs
	Transient Response — Overshoot			0			5		%
SR	Slew Rate	$R_L = 5.0$ kΩ, $A_V = 1.0$		0.03			0.35		V/µs

The following specifications apply $0°C \leq T_A \leq +70°C$

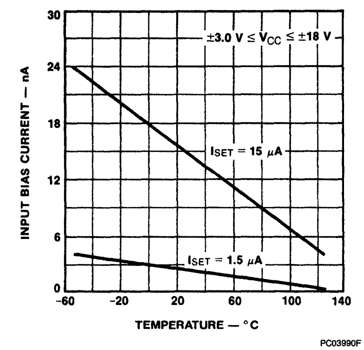
Symbol	Characteristic	Condition	$I_{SET} = 1.5\mu A$ Min	$I_{SET} = 1.5\mu A$ Typ	$I_{SET} = 1.5\mu A$ Max	$I_{SET} = 15\mu A$ Min	$I_{SET} = 15\mu A$ Typ	$I_{SET} = 15\mu A$ Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			7.5	mV
I_{IO}	Input Offset Current	$T_A = 70°C$			6.0			25	nA
		$T_A = 0°C$			10			40	
I_{IB}	Input Bias Current	$T_A = 70°C$			10			50	nA
		$T_A = 0°C$			20			100	
I_{CC}	Supply Current				25			180	µA
P_c	Power Consumption				150			1080	µW
CMR	Common Mode Rejection	$R_S \leq 10$ kΩ	70	86		70	86		dB
V_{IR}	Input Voltage Range		±1.0			±1.0			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		25	200		25	200	µV/V
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 1.0$ V, $R_L \geq 75$ kΩ	25						V/mV
		$V_O = \pm 1.0$ V, $R_L \geq 5.0$ kΩ				25			
V_{OP}	Output Voltage Swing	$R_L = 75$ kΩ	±2.0	±2.4					V
		$R_L = 5.0$ kΩ				±2.0	±2.1		

Typical Performance Curves for μA776 and μA776C

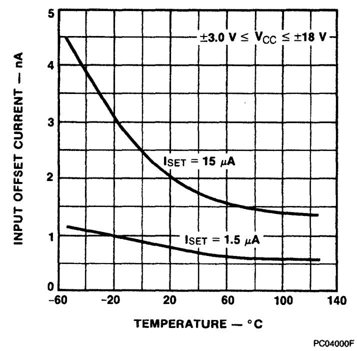
Input Bias Current vs Set Current



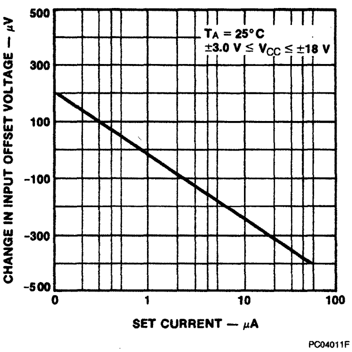
Input Bias Current vs Temperature



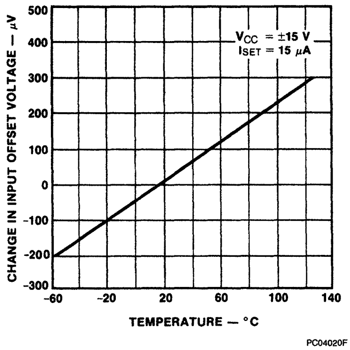
Input Offset Current vs Temperature



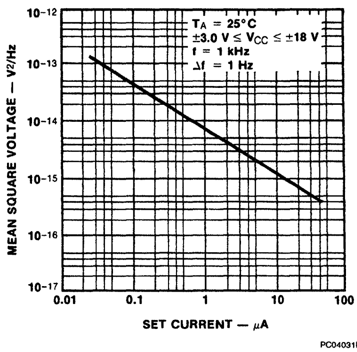
Change in Input Offset Voltage vs Set Current



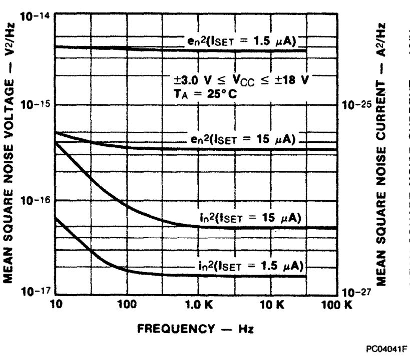
Change in Input Offset Voltage vs Temperature (Unnulled)



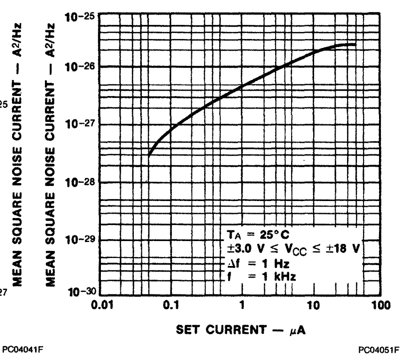
Input Noise Voltage vs Set Current



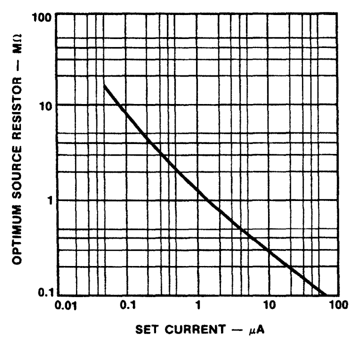
Input Noise Voltage and Current vs Frequency



Input Noise Current vs Set Current

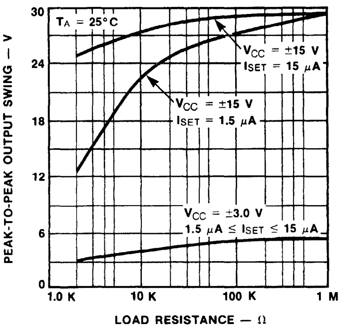


Optimum Source Resistor for Minimum Noise vs Set Current



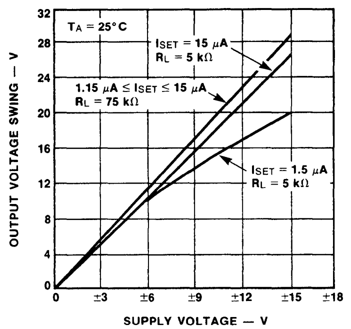
Typical Performance Curves for μA776 and μA776C (Cont.)

Output Voltage Swing vs Load Resistance



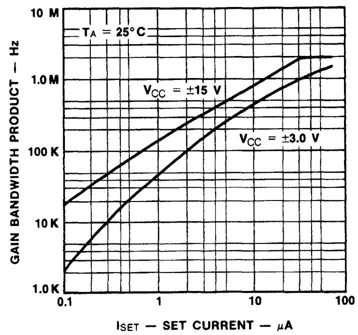
PC04071F

Output Voltage Swing vs Supply Voltage



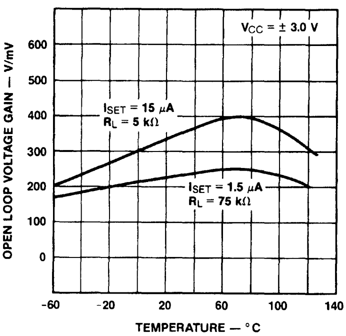
PC04080F

Gain Bandwidth Product vs Set Current



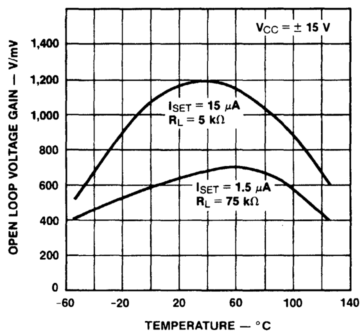
PC04091F

Voltage Gain vs Temperature



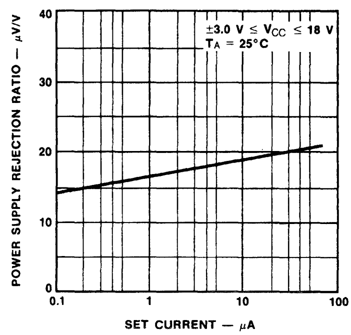
PC04101F

Voltage Gain vs Temperature



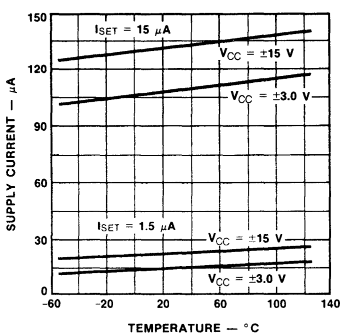
PC04111F

Power Supply Rejection Ratio vs Set Current



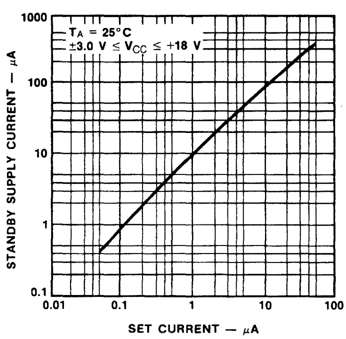
PC04121F

Supply Current vs Temperature



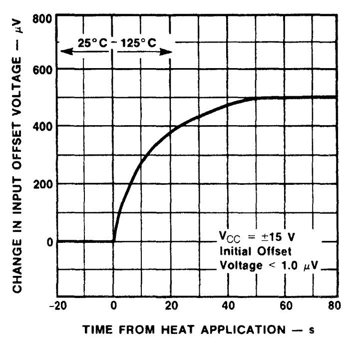
PC04130F

Standby Supply Current vs Set Current



PC04141F

Thermal Response Of Input Offset Voltage To Step Change Of Case Temperature



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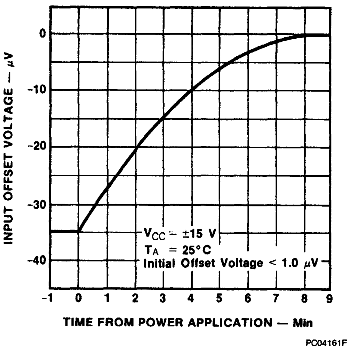
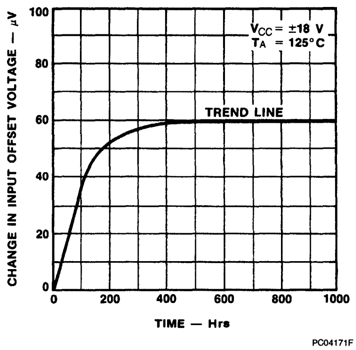
Typical Performance Curves for μA776 and μA776C (Cont.)

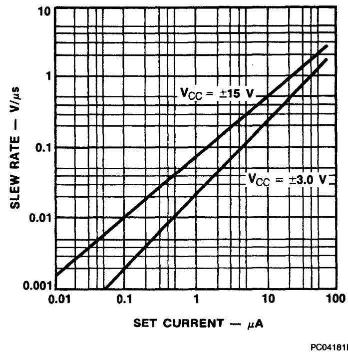
Stabilization Time Of Input Offset Voltage From Power On



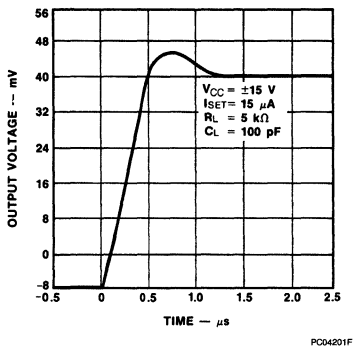
Input Offset Voltage Drift vs Time



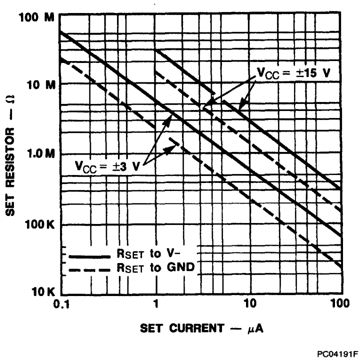
Slew Rate vs Set Current



Voltage Follower Transient Response (Unity Gain)



Set Current vs Set Resistor



Quiescent Current Setting Resistor (I_{SET} to V^-)

V_S	I_{SET} 1.5 μA	I_{SET} 15 μA
±1.5 V	1.7 MΩ	170 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Note
The μA776 may be operated with R_{SET} connected to ground or V−

I_{SET} Equations

$$I_{SET} = \frac{(V+)-0.7-(V-)}{R_{SET}}$$

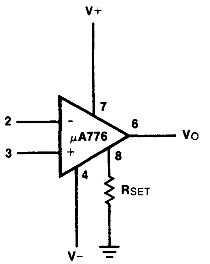
where:
R_{SET} is connected to V−

$$I_{SET} = \frac{(V+)-0.7}{R_{SET}}$$

where:
R_{SET} is connected to ground.

Biasing Circuits

Resistor Biasing



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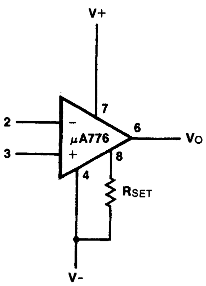
R_{SET} Connected to Ground



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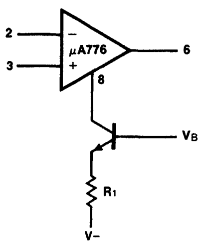
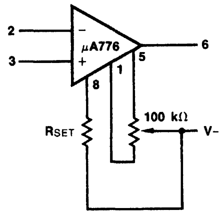
R_{SET} Connected to V−
*Recommended for supply voltages less than ±6 V.

Transistor Current Source Biasing



AF00621F

Voltage Offset Null Circuit



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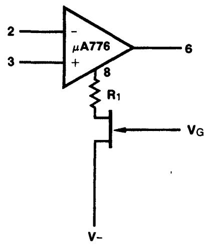
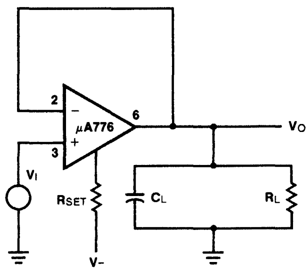
FET Current Source Biasing



AF00610F

Transient Response Test Circuit



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7

FAIRCHILD

A Schlumberger Company

μA798 Dual Operational Amplifier

Linear Division Operational Amplifiers

Description

The μA798 consists of a monolithic pair of independent, high gain, internally frequency compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage. The μA798 is constructed using the Fairchild Planar Epitaxial process.

- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**
- **Output Voltage Can Swing Near Ground Or Negative Supply**
- **Internally Compensated**
- **Wide Power Supply Range Single Supply Of 3.0 V To 36 V Dual Supply of ±1.5 V To ±18 V**
- **Class AB Output Stage For Minimal Crossover Distortion**
- **Short Circuit Protected Output**
- **High Open Loop Gain — 200 k Typ**
- **Exceeds μA1458 Type Performance**
- **Operation Specified At ±15 V And +5.0 V Power Supplies**
- **High Output Current Sink Capability 0.8 mA At V_O = 400 mV Typ**

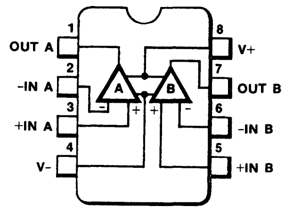
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage Between V+ and V−	36 V
Differential Input Voltage	±30 V
Input Voltage[3]	−0.3 V (V−) to V+
Output Short Circuit Duration[4]	Indefinite

Notes

1. $T_{J\ Max}$ = 150°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.
3. For supply voltage less than 30 V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.
4. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)

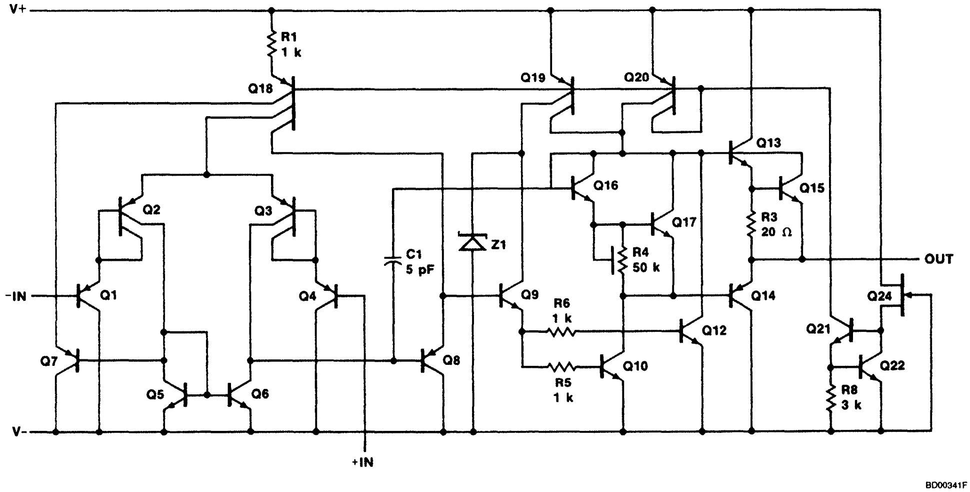


CD00690F

Order Information

Device Code	Package Code	Package Description
μA798SC	KC	Molded Surface Mount
μA798TC	9T	Molded DIP

Equivalent Circuit (1/2 of circuit shown)



Note

1. All resistor values in ohm.

7

μA798

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage				2.0	6.0	mV
I_{IO}	Input Offset Current				10	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.3	1.0		MΩ
R_O	Output Resistance				800		Ω
I_{CC}	Supply Current		$V_O = 0$, $R_L = \infty$		2.0	4.0	mA
CMR	Common Mode Rejection		$R_S \leq 10$ kΩ	70	90		dB
V_{IR}	Input Voltage Range			+13 to V–	+13.5 to V–		V
PSRR	Power Supply Rejection Ratio		Positive		30	150	μV/V
			Negative		30	150	
I_{OS}	Output Short Circuit Current[1,2]		$V_O = -15$ V, $V_{ID} = 1.0$ V	10	30	45	mA
	(Per Amplifier)		$V_O =$ Gnd, $V_{ID} = -1.0$ V	10	70	85	
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	20	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±13	±14		V
			$R_L = 2.0$ kΩ	±12	±13.5		
TR	Transient Response	Rise Time	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		0.3		μs
		Fall Time	$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		0.3		
		Overshoot	$V_O = 50$ mV $A_V = 1.0$, $R_L = 10$ kΩ		20		%
BW	Bandwidth		$V_O = 50$ mV, $A_V = 1.0$, $R_L = 10$ kΩ		1.0		MHz
SR	Slew Rate		$V_I = -10$ V to +10 V, $A_V = 1.0$		0.6		V/μs
CS	Channel Separation		f = 1.0 kHz to 20 kHz (Input Referenced)		–120		dB

The following specifications apply for $0°C \leq T_A \leq +70°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage				7.5	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10		μV/°C
I_{IO}	Input Offset Current				200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50		pA/°C
I_{IB}	Input Bias Current				400	nA

μ**A798** (Cont.)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
A_{VS}	Large Signal Voltage Gain	$R_L = 2.0$ kΩ, $V_O = \pm 10$ V	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0$ kΩ	±10			V

The following specifications apply for $T_A = 25°C$, V+ = 5.0 V, V−=GND

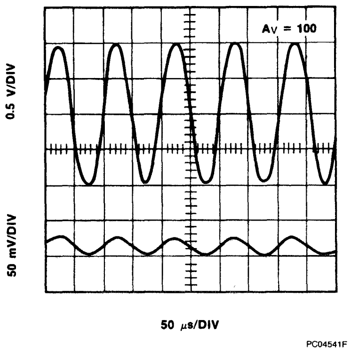
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage			2.0	7.5	mV
I_{IO}	Input Offset Current			10	50	nA
I_{IB}	Input Bias Current			80	250	nA
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 2.0$ kΩ	20	200		V/mV
PSRR	Power Supply Rejection Ratio				150	μV/V
V_{OP}	Output Voltage Swing[3]	$R_L = 10$ kΩ	4.0			V_{p-p}
		$5.0 \text{ V} \leqslant V+ \leqslant 30$ V $R_L = 10$ kΩ	(V+) −1.5			
I_{O-}	Output Sink Current	$V_O = 200$ mV, $V_{ID} = 1.0$ V	0.35			mA
I_{CC}	Supply Current			2.0	4.0	mA

Notes

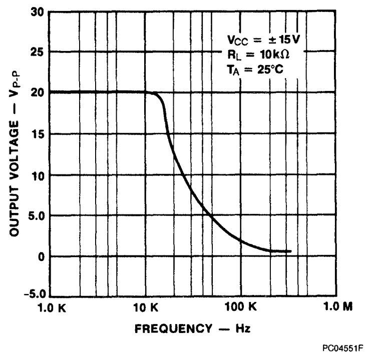
1. Not to exceed maximum package power dissipation.
2. Indefinite on shorts to ground or V− supply. Shorts to V+ supply may result in power dissipation exceeding the absolute maximum rating.
3. Output will swing to ground.

Typical Performance Curves

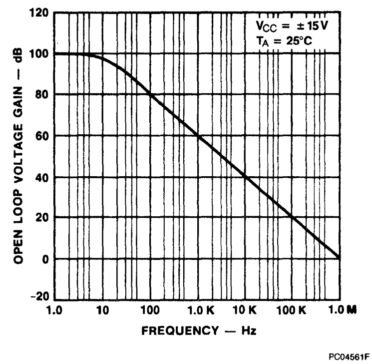
Sinewave Response



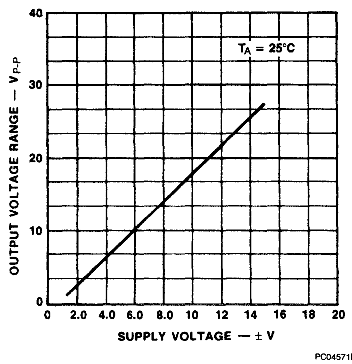
Output Voltage vs Frequency



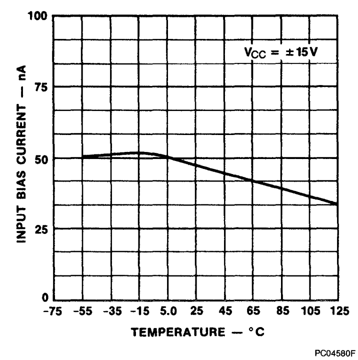
Open Loop Frequency Response



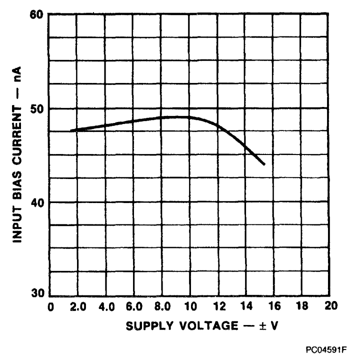
Output Swing vs Supply Voltage



Input Bias Current vs Temperature

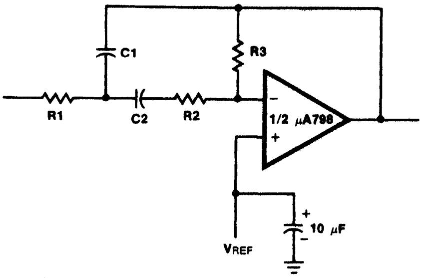


Input Bias Current vs Supply Voltage



Typical Applications

Multiple Feedback Bandpass Filter



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$f_o \stackrel{\Delta}{=}$ center frequency

$BW \stackrel{\Delta}{=}$ Bandwidth

R in kΩ

C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

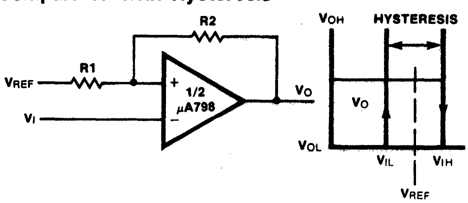
$\left.\begin{array}{l} R1 = R2 = 1 \\ R3 = 9Q^2 - 1 \end{array}\right\}$ Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:
given: Q = 5, f_o = 1.0 kHz
Let R1 = R2 = 10 kΩ
then R3 = $9(5)^2 - 10$
R3 = 215 kΩ

$$C = \frac{5}{3} = 1.6\ \mu F$$

Comparator With Hysteresis



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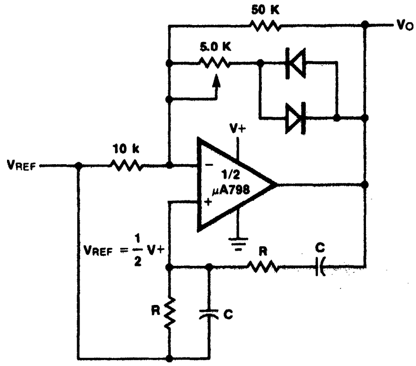
$$V_{IL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH}\ V_{OL})$$

$$f = \frac{R1 + R2}{4CR_fR1} \text{ if } R3 = \frac{R2R1}{R2 + R1}$$

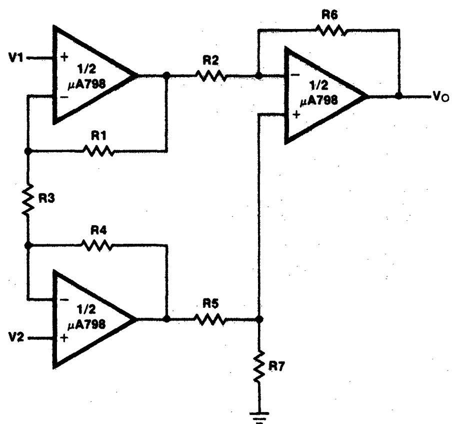
Wein Bridge Oscillator



AF00671F

$f_o = \frac{1}{2\pi RC}$ for f_o = 1.0 kHz
R = 16 kΩ
C = 0.01 μF

High Impedance Differential Amplifier



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$V_O = C\ (1 + a + b)(V2 - V1)$

$\frac{R2}{R5} \equiv \frac{R6}{R7}$ for best CMRR

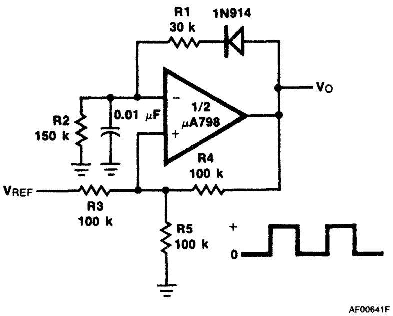
R1 = R4
R2 = R5

$$\text{Gain} = \frac{R6}{R2}\left(1 + \frac{2R1}{R3}\right) = C\ (1 + a + b)$$

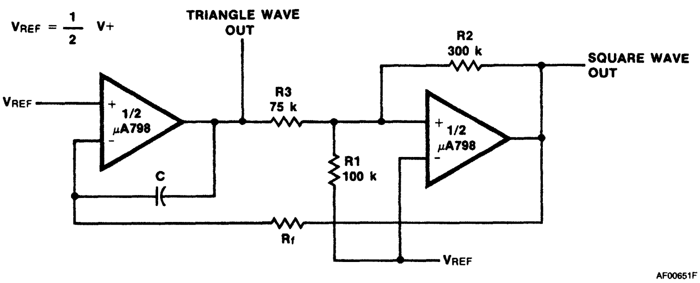
Note
1. All resistor values in ohms.

Typical Applications (Cont.)

Pulse Generator



Function Generator



Note

1. All resistor values are in ohms.

FAIRCHILD

A Schlumberger Company

μA111 • μA311 Voltage Comparators

Description

The μA111 and μA311 are monolithic, low input current voltage comparators, each constructed using the Fairchild Planar Epitaxial process. The μA111 series operates from the single 5.0 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA111 series is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.

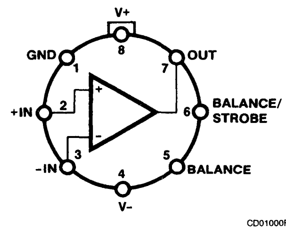
- **Low Input Bias Current 100 nA Max (μA111), 250 nA Max (μA311)**
- **Low Input Offset Current 10 nA Max (μA111), 50 nA Max (μA311)**
- **Differential Input Voltage ±30 V**
- **Power Supply Voltage Single 5.0 V Supply To ±15 V**
- **Offset Voltage Null Capability**
- **Strobe Capability**

Absolute Maximum Ratings[1]

Storage Temperature Range	
Metal Can	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C
Operating Temperature Range	
Extended (μA111M)	-55°C to +125°C
Commercial (μA311C)	0°C to 70°C
Lead Temperature	
Metal Can (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[2, 3]	
8L-Metal Can	1.00 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Voltage between V+ and V–	36 V
Output to V–	
(μA111)	50 V
(μA311)	40 V
Ground to V–	30 V
Differential Input Voltage	±30 V
Input Voltage	±15 V
Output Short Circuit Duration	10 s

Notes
1. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
2. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-8, and 175°C for the Metal Can.
3. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.

Connection Diagram
8-Lead Metal Package
(Top View)

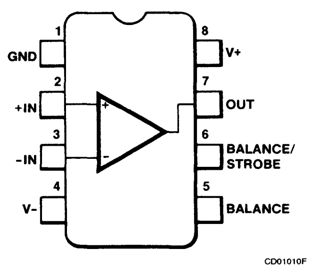


Lead 4 connected to case

Order Information

Device Code	Package Code	Package Description
μA111HM	5W	Metal
μA311HC	5W	Metal

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA311TC	9T	Molded DIP
μA311SC	KC	Molded Surface Mount

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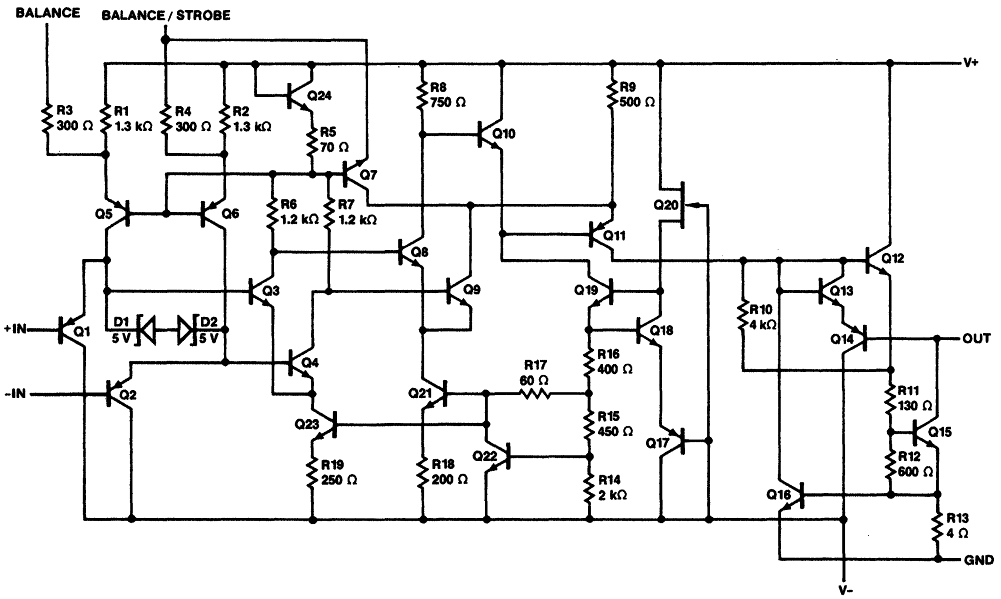
Equivalent Circuit



EQ00381F

μA111

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.[1]

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage[2]	$R_S \leqslant 50$ kΩ		0.7	3.0	mV
I_{IO}	Input Offset Current[2]			4.0	10	nA
I_{IB}	Input Bias Current			60	100	nA
A_{VS}	Large Signal Voltage Gain			200		V/mV
t_{PD}	Response Time[3]			200		ns
V_{SAT}	Saturation Voltage	$V_I \leqslant -5.0$ mV, $I_{OL} = 50$ mA		0.75	1.5	V
$I_{O(ST)}$	Strobe On Current			3.0		mA
I_{CEX}	Output Leakage Current	$V_I \geqslant 5.0$ mV, $V_O = 35$ V		0.2	10	nA
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$.						
V_{IO}	Input Offset Voltage[2]	$R_S \leqslant 50$ kΩ			4.0	mV
I_{IO}	Input Offset Current[2]				20	nA
I_{IB}	Input Bias Current				150	nA
V_{IR}	Input Voltage Range			±14		V
V_{SAT}	Saturation Voltage	$V+ \geqslant 4.5$ V, $V- = 0$ V, $V_I \leqslant -6.0$ mV, $I_{OL} \leqslant 8.0$ mA		0.23	0.4	V

μA111 (Cont.)

Electrical Characteristics $-55°C \leq T_A \leq +125°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.[1]

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{CEX}	Output Leakage Current	$V_I \geq 5.0$ mV, $V_O = 35$ V		0.1	0.5	μA
I+	Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
I–	Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

μA311

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15$ V, unless otherwise specified.[1]

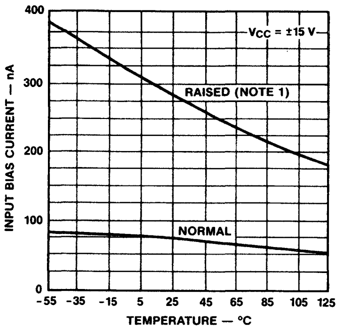
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage[2]	$R_S \leq 50$ kΩ		2.0	7.5	mV
I_{IO}	Input Offset Current[2]			6.0	50	nA
I_{IB}	Input Bias Current			100	250	nA
A_{VS}	Large Signal Voltage Gain			200		V/mV
t_{PD}	Response Time[3]			200		ns
V_{SAT}	Saturation Voltage	$V_I \leq -10$ mV, $I_O = 50$ mA		0.75	1.5	V
$I_{O(ST)}$	Strobe On Current			3.0		mA
I_{CEX}	Output Leakage Current	$V_I \geq 10$ mV, $V_O = 35$ V		0.2	50	nA
The following specifications apply for $0°C \leq T_A \leq +70°C$.						
V_{IO}	Input Offset Voltage[2]	$R_S \leq 50$ kΩ			10	mV
I_{IO}	Input Offset Current[2]				70	nA
I_{IB}	Input Bias Current				300	nA
V_{IR}	Input Voltage Range			±14		V
V_{SAT}	Saturation Voltage	$V+ \geq 4.5$ V, $V- = 2.25$ V, $V_I \leq -10$ mV, $I_{OL} \leq 8.0$ mA		0.23	0.4	V
I+	Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
I–	Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Notes

1. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 V supply to ±15 V supplies.
2. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive.

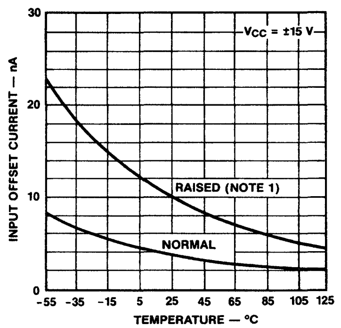
Typical Performance Curves for μA111

Input Bias Current vs Temperature



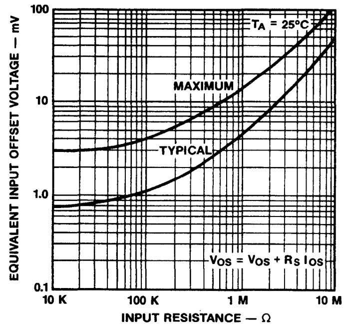
PC06720F

Input Offset Current vs Temperature



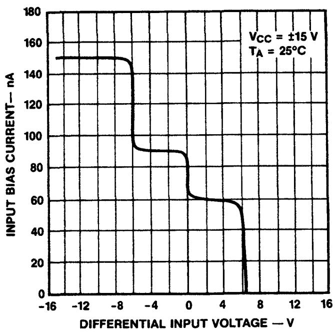
PC06730F

Offset Voltage vs Input Resistance



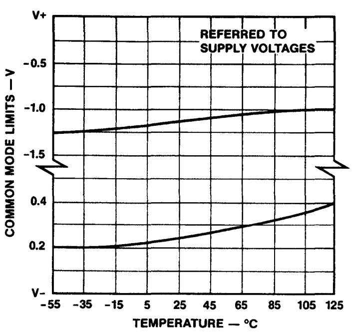
PC06740F

Input Bias Current vs Differential Input Voltage



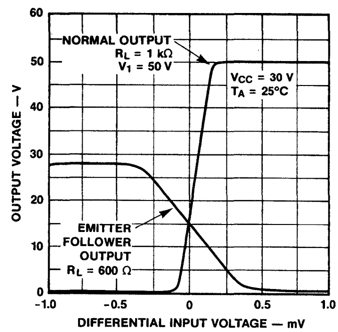
PC06750F

Common Mode Limits vs Temperature



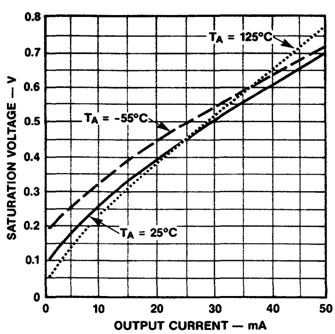
PC06760F

Output Voltage vs Differential Input Voltage



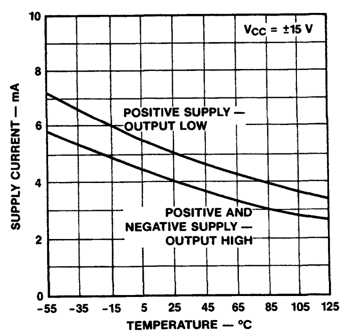
PC06770F

Saturation Voltage vs Output Current



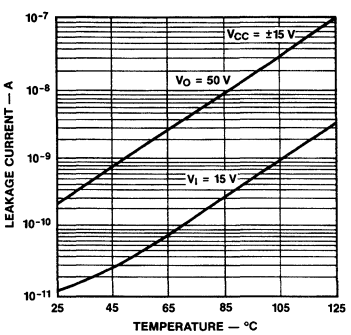
PC06780F

Supply Current vs Temperature



PC06790F

Leakage Current vs Temperature



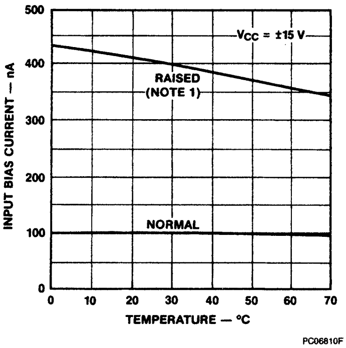
PC06800F

Note

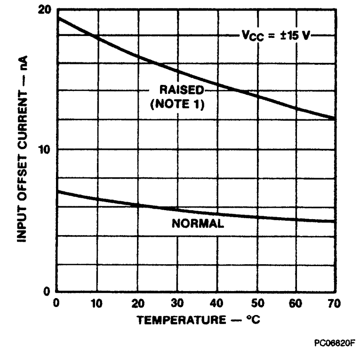
1. Leads 5, 6 and 8 are shorted.

Typical Performance Curves for μA311

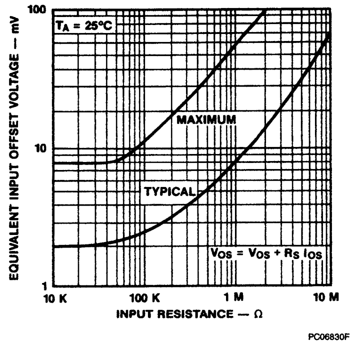
Input Bias Current vs Temperature



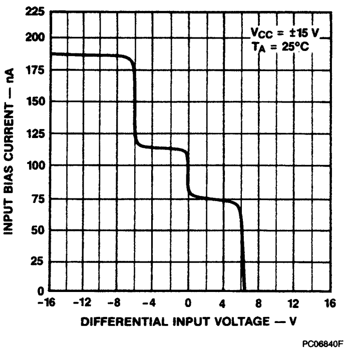
Input Offset Current vs Temperature



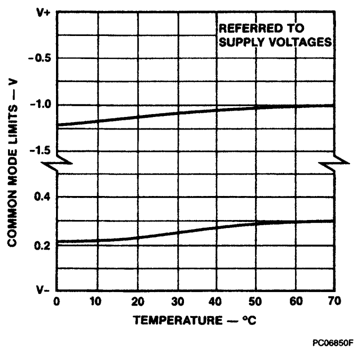
Offset Voltage vs Input Resistance



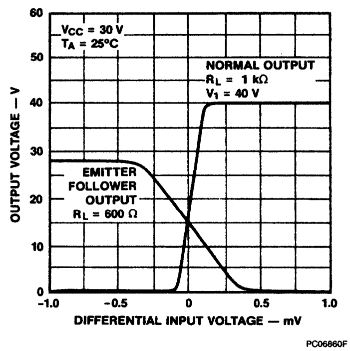
Input Bias Current vs Differential Input Voltage



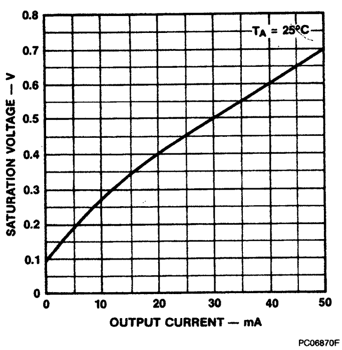
Common Mode Limits vs Temperature



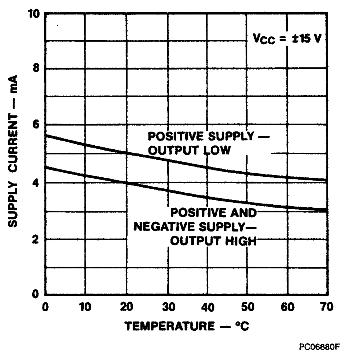
Output Voltage vs Differential Input Voltage



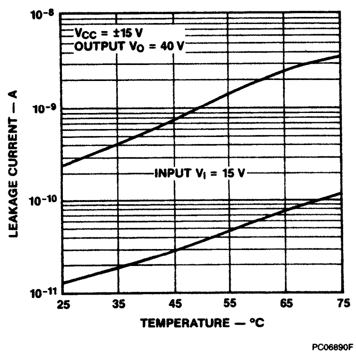
Saturation Voltage vs Output Current



Supply Current vs Temperature



Leakage Current vs Temperature

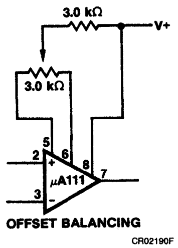


Note

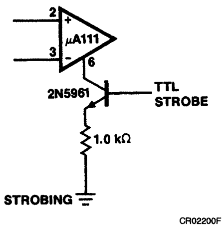
1. Leads 5, 6 and 8 are shorted.

Typical Applications

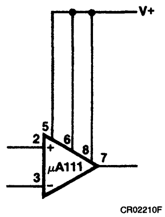
Offset Null Circuit



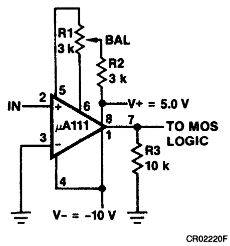
Strobe Circuit



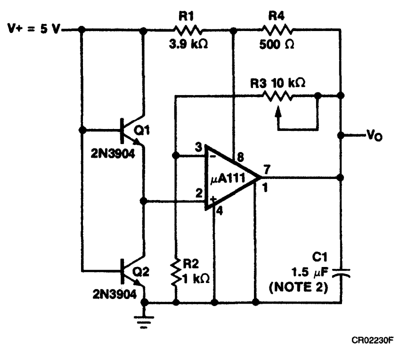
Increasing Input Stage Current (Note 1)



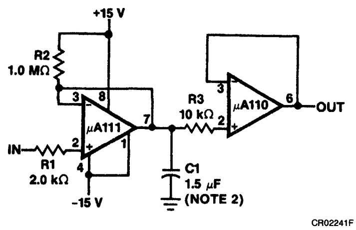
Zero Crossing Detector Driving MOS Logic (Note 3)



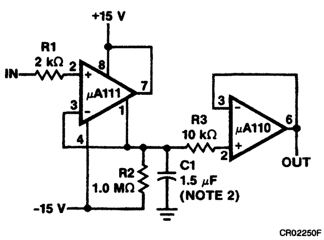
Adjustable Low Voltage Reference Supply



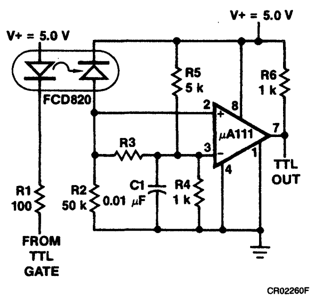
Negative Peak Detector



Positive Peak Detector



Digital Transmission Isolator (Note 3)

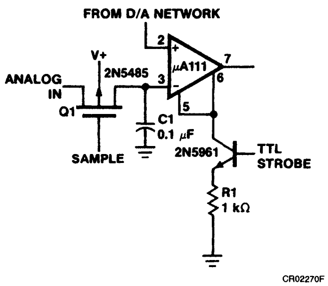


Notes

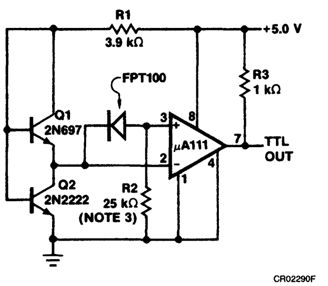
1) Increases typical common mode slew rate from 7.0 V/μs to 18 V/μs.
2) Solid Tantalum.
3) All resistor values in ohms.

Typical Applications (Cont.)

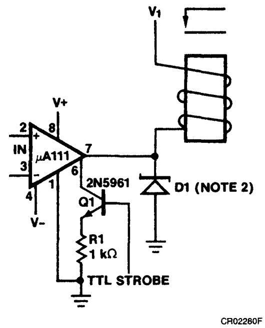
Strobing of Both Input And Output Stages (Note 1)



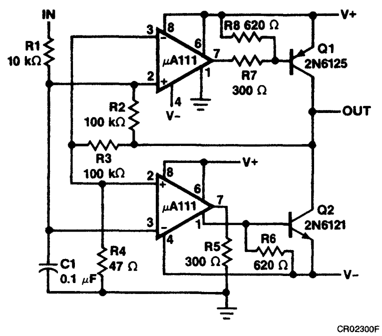
Precision Photodiode Comparator



Relay Driver with Strobe



Switching Power Amplifier



Notes

1. Typical input current is 50 pA with inputs strobed off.
2. Absorbs inductive kickback of relay and protects IC from severe voltage transients on V_I line.
3. R2 sets the comparison level. At comparison, the photodiode has less than 5.0 mV across it, decreasing leakages by an order of magnitude.

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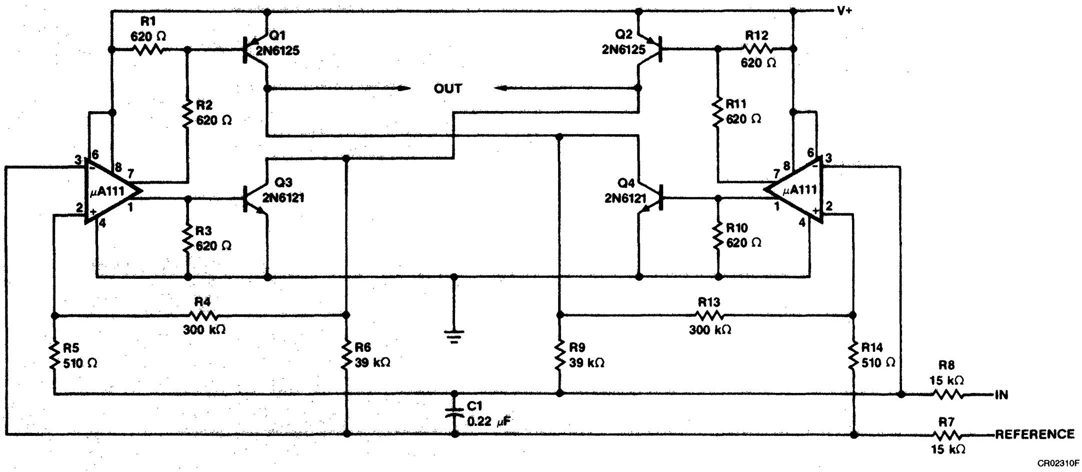
Switching Power Amplifier



FAIRCHILD

A Schlumberger Company

μA139 • μA239 • μA339
μA2901 • μA3302
Quad Comparators

Description

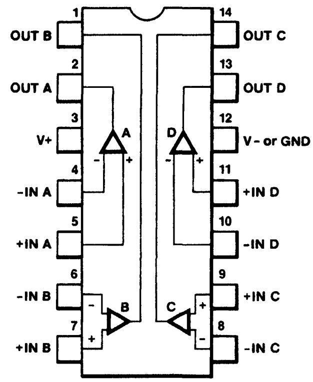
The μA139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stages allow the input common mode voltage to include ground.

- **Single Supply Operation +2.0 V To +36 V**
- **Dual Supply Operation ±1.0 V To ±18 V**
- **Allow Comparison Of Voltages Near Ground Potential**
- **Low Current Drain 800 μA Typ**
- **Compatible With All Forms Of Logic**
- **Low Input Bias Current 25 nA Typ**
- **Low Input Offset Current ±5.0 nA Typ**
- **Low Offset Voltage ±2.0 mV**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA139M)	-55°C to +125°C
Automotive (μA2901V, μA3302V)	-40°C to +85°C
Industrial (μA239V)	-25°C to +85°C
Commercial (μA339C)	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	
μA139 Series/μA2901	36 V or ±18 V
μA3302	28 V or ±14 V
Differential Input Voltage	
μA139 Series/μA2901	36 V
μA3302	28 V
Output Short Circuit to GND[3]	Indefinite
Input Current ($V_I < -0.3$ V)[4]	50 mA

Connection Diagram
14-Lead DIP and SO-14 Package
(Top View)



CD01021F

Order Information

Device Code	Package Code	Package Description
μA139DM	6A	Ceramic DIP
μA239DV	6A	Ceramic DIP
μA239PV	9A	Molded DIP
μA239SV	KD	Molded Surface Mount
μA339DC	6A	Ceramic DIP
μA339PC	9A	Molded DIP
μA339SC	KD	Molded Surface Mount
μA2901DV	6A	Ceramic DIP
μA2901PV	9A	Molded DIP
μA3302DV	6A	Ceramic DIP
μA3302PV	9A	Molded DIP
μA3302SV	KD	Molded Surface Mount

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V+.
4. This input current will exist only when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level or to ground for a large overdrive, for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3 V.

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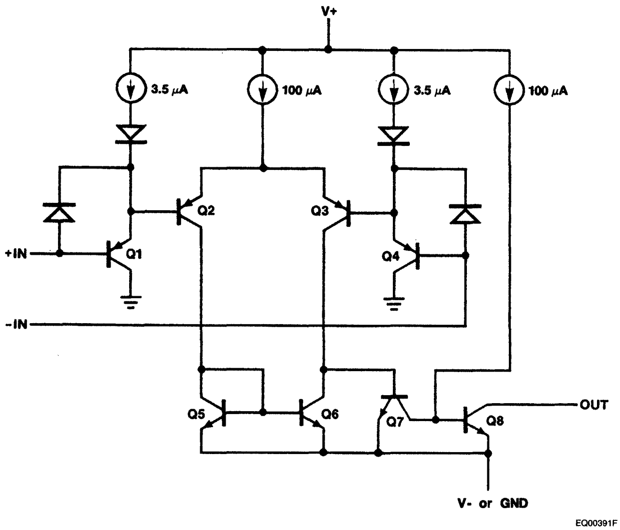
Equivalent Circuit



μA139, μA239, μA339
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, unless otherwise specified.

			μA139			μA239, μA339			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IO}	Input Offset Voltage[5]			±2.0	±5.0		±2.0	±5.0	mV
I_{IB}	Input Bias Current[1]	I_I+ or I_I– with Output in Linear Range		25	100		25	250	nA
I_{IO}	Input Offset Current	(I_I+) – (I_I–)		±5.0	±25		±5.0	±50	nA
V_{IR}	Input Common Mode Voltage Range[2]		0		(V+) – 1.5	0		(V+) – 1.5	V
I_{CC}	Supply Current	$R_L = \infty$ on all Comparators		0.8	2.0		0.8	2.0	mA
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 15$ kΩ, V+ = 15 V (To Support Large V_O Swing)		200			200		V/mV
t_{PD1}	Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ		300			300		ns
t_{PD2}	Response Time[3]	V_{RL} = 5.0 V, R_L = 5.1 kΩ		1.3			1.3		μs

μA139, μA239, μA339 (Cont.)
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, unless otherwise specified.

			μA139			μA239, μA339			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{OL}	Output Sink Current	$V_I- \geq 1.0$ V, $V_I+ = 0$ V, $V_O \leq 1.5$ V	6.0	16		6.0	16		mA
V_{SAT}	Saturation Voltage	$V_I- \geq 1.0$ V, $V_I+ = 0$ V, $I_{OL} \leq 4.0$ mA		250	400		250	400	mV
I_{CEX}	Output Leakage Current	$V_I+ \geq 1.0$ V, $V_I- = 0$ V, $V_O = 30$ V			200			200	nA
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for the μA139, $-25°C \leq T_A \leq +85°C$ for the μA239 and $0°C \leq T_A \leq +70°C$ for the μA339.									
V_{IO}	Input Offset Voltage[5]				9.0			9.0	mV
I_{IO}	Input Offset Current	$(I_I+) - (I_I-)$			±100			±150	nA
I_{IB}	Input Bias Current	I_I+ or I_I- with Output in Linear Range			300			400	nA
V_{IR}	Input Voltage Range		0		(V+) − 2.0	0		(V+) − 2.0	V
V_{SAT}	Saturation Voltage	$V_I- \geq 1.0$ V, $V_I+ = 0$ V, $I_{OL} \leq 4.0$ mA			700			700	mV
I_{CEX}	Output Leakage Current	$V_I+ \geq 1.0$ V, $V_I- = 0$ V, $V_O = 30$ V			1.0			1.0	μA
V_{ID}	Differential Input Voltage[4]	Keep all $V_{I's} \geq 0$ V (or V−, if used)			36			36	V

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μA2901, μA3302
Electrical Characteristics T_A = 25°C, V+ = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	μA2901			μA3302			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage[5]			±2.0	±7.0		±3.0	±2.0	mV
I_{IB}	Input Bias Current[1]	I_I+ or I_I– with Output in Linear Range		25	250		25	500	nA
I_{IO}	Input Offset Current	$(I_I+) - (I_I-)$		±5.0	±50		±5.0	±100	nA
V_{IR}	Input Common Mode Voltage Range[2]		0		(V+) – 1.5	0		(V+) – 1.5	V
I_{CC}	Supply Current	$R_L = \infty$ on all Comparators		0.8	2.0		0.8	2.0	mA
		$R_L = \infty$, V+ = 30 V		1.0	2.5				
A_{VS}	Large Signal Voltage Gain	$R_L \geqslant 15$ kΩ, V+ = 15 V (To Support Large V_O Swing)	25	100		2.0	30		V/mV
t_{PD1}	Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = 1.4 V, V_{RL} = 5.0 V, R_L = 5.1 kΩ		300			300		ns
t_{PD2}	Response Time[3]	V_{RL} = 5.0 V, R_L = 5.1 kΩ		1.3			1.3		μs
I_{OL}	Output Sink Current	$V_I- \geqslant 1.0$ V, $V_I+ = 0$ V, $V_O \leqslant 1.5$ V	6.0	16		2.0	16		mA
V_{SAT}	Saturation Voltage	$V_I- \geqslant 1.0$ V, $V_I+ = 0$ V, $I_{OL} \leqslant 4.0$ mA			400		250	500	mV
I_{CEX}	Output Leakage Current	$V_I+ \geqslant 1.0$ V, $V_I- = 0$ V, $V_O = 30$ V			200			200	nA

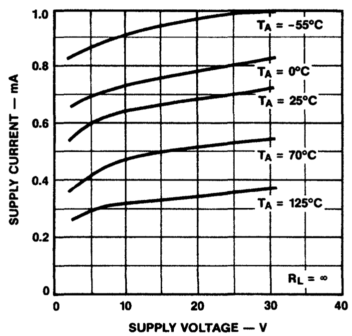
μA2901, μA3302 (Cont.)
Electrical Characteristics $-40°C \leq T_A \leq +85°C$, V+ = 5.0 V, unless otherwise specified.

			μA2901			μA3302			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{IO}	Input Offset Voltage[5]			9.0	15			40	mV
I_{IO}	Input Offset Current	$(I_I+) - (I_I-)$		50	200			300	nA
I_{IB}	Input Bias Current	I_I+ or I_I- with Output in Linear Range		200	500			1000	nA
V_{IR}	Input Voltage Range		0		(V+) − 2.0	0		(V+) − 2.0	V
V_{SAT}	Saturation Voltage	$V_I- \geq 1.0$ V, $V_I+ = 0$ V, $I_{OL} \leq 4.0$ mA		400	700			700	mV
I_{CEX}	Output Leakage Current	$V_I+ \geq 1.0$ V, $V_I- = 0$ V, $V_O = 30$ V			1.0			1.0	μA
V_{ID}	Differential Input Voltage[4]	Keep all $V_{I's} \geq 0$ V (or V−, if used)			V+			V+	V

Notes
1. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is (V+) − 1.5 V, but either or both inputs can go to +30 V without damage.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance curves segment.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
5. At output switch point, $V_O \simeq 1.4$ V, $R_S = 0\ \Omega$ with V+ from 5.0 V; and over the full input common mode range 0 V to V+ −1.5 V.
6. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5.0 V supply, V_I should be limited to 25 V maximum and a limiting resistor should be used on all inputs that might exceed the positive supply.

Typical Performance Curves for μA139, μA239, μ339

Supply Current



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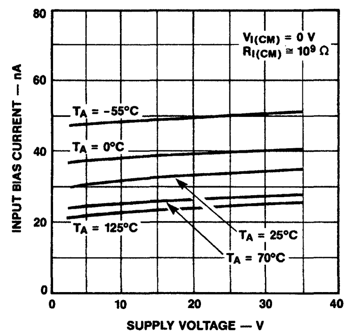
Input Bias Current



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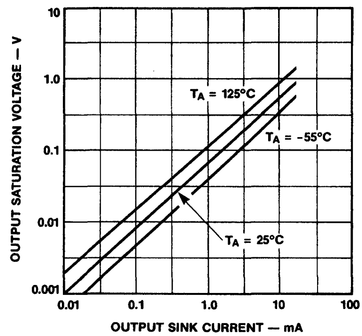
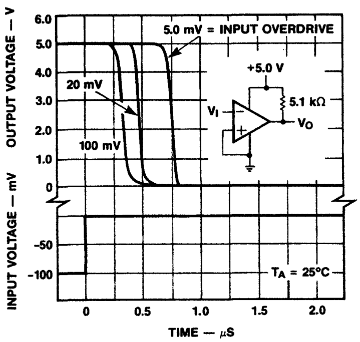
Output Saturation Voltage



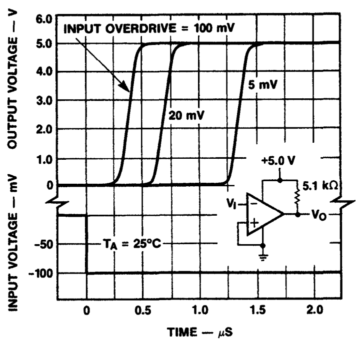
PC06970F

Response Time for Various Input Overdrives — Negative Transition



PC06930F

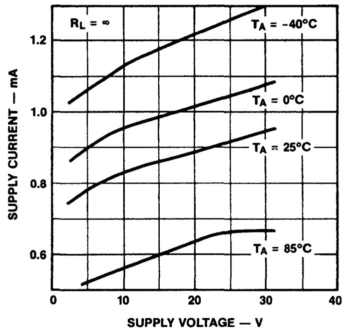
Response Time for Various Input Overdrives — Positive Transition



PC06940F

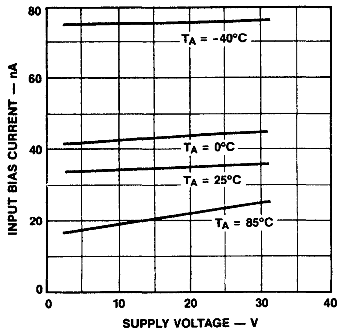
Typical Performance Curves for μA2901, μA3302

Supply Current



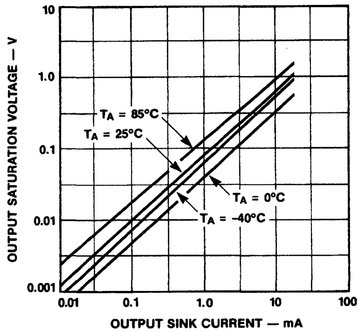
PC06950F

Input Bias Current



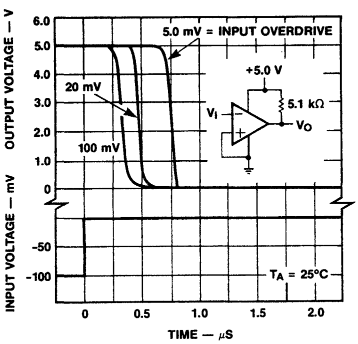
PC06960F

Output Saturation Voltage



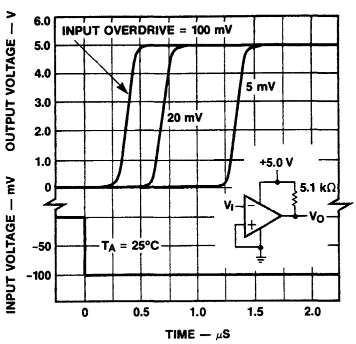
PC06921F

Response Time for Various Input Overdrives — Negative Transition



PC06930F

Response Time for Various Input Overdrives — Positive Transition



PC06940F

Application Information

The μA139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input/output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1.0 V to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the leads will cause input/output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All leads of any unused comparators should be grounded.

The bias network of the μA139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 2.0 V to 30 V.

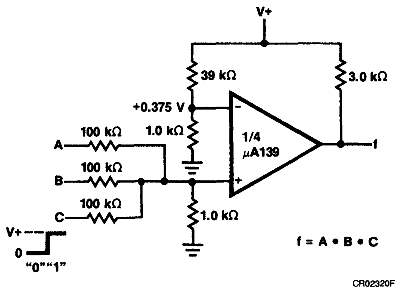
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going more negative than -0.3 V (at 25°C). An input clamp diode can be used as shown in the applications segment of this data sheet.

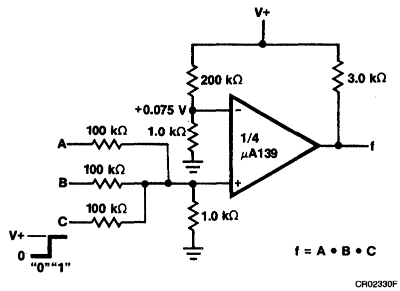
The output of the μA139 series is the uncommitted collector of grounded emitter NPN output transistor. Many collectors can be tied together to provide wired OR output function. An output pull-up resistor can be connected to any available power supply within the permitted supply voltage range. There is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the μA139 package. The output can also be used as a simple SP/ST switch to ground (when a pull up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications (V+ = 15 V)

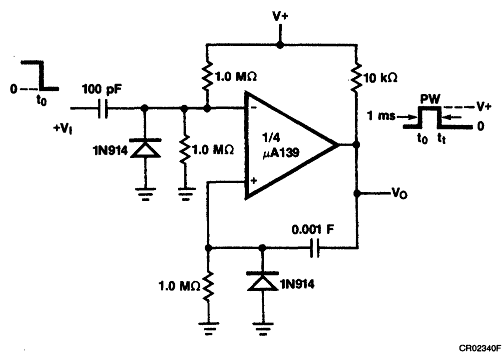
AND Gate



OR Gate

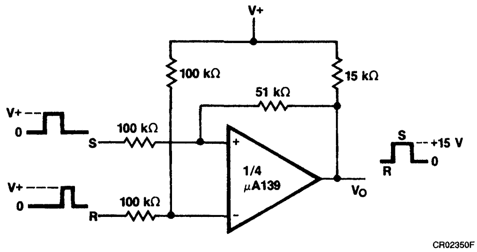


Monostable Multivibrator

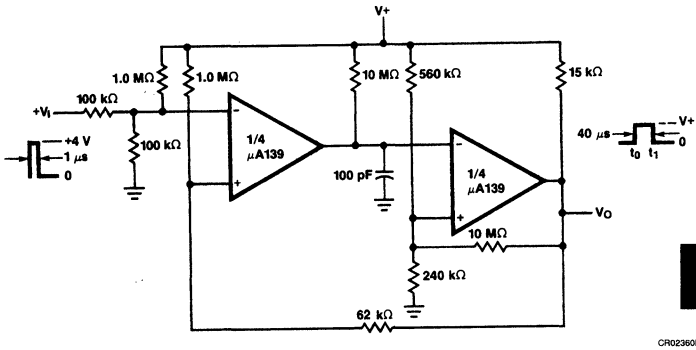


Typical Applications (V+ = 15 V) (Cont.)

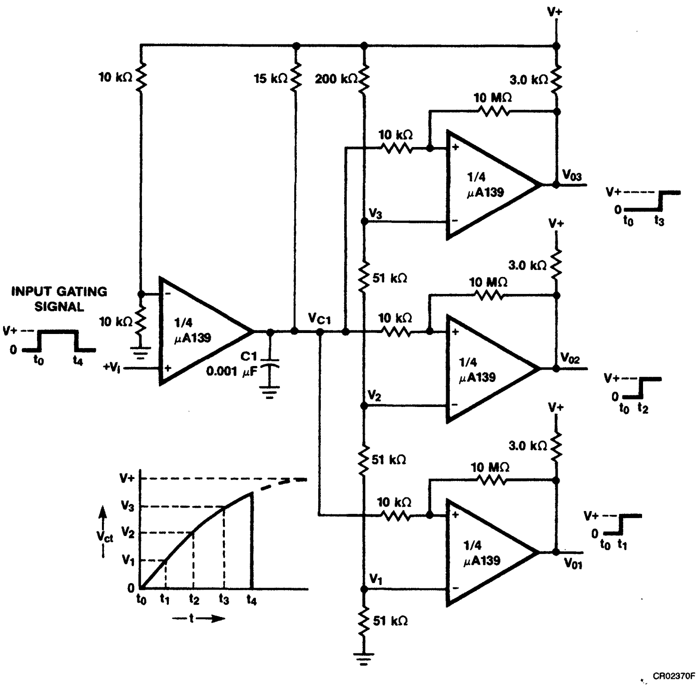
Bistable Multivibrator



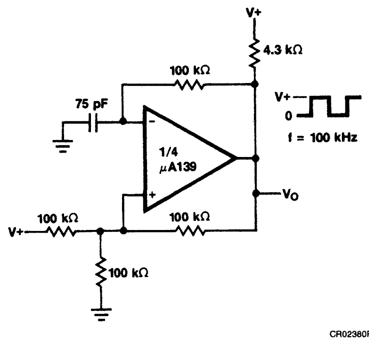
Monostable Multivibrator with Input Lock Out



Time Delay Generator



Squarewave Oscillator



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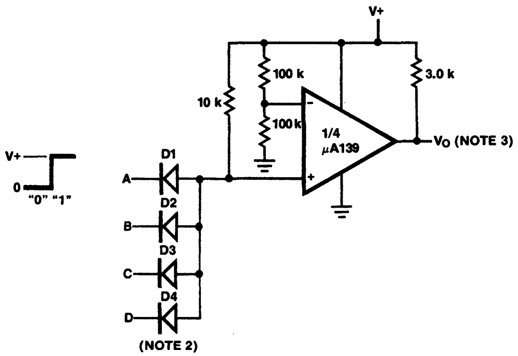
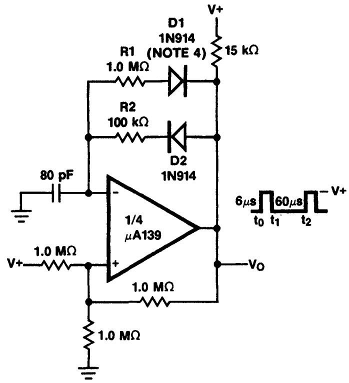
Typical Applications (V+ = 15 V) (Cont.)

Large Fan-In AND Gate (Note 1)



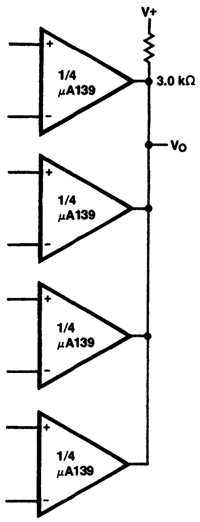
CR02400F

Pulse Generator



CR02410F

Wired-OR Outputs



CR02390F

Notes
1) All resistor values in ohms.
2) All diodes 1N914.
3) $V_O = A \cdot B \cdot C \cdot D$
4) For large ratios of R1/R2, D1 can be omitted.

FAIRCHILD

A Schlumberger Company

μA6685 Ultra Fast Single Latched Comparator

Linear Division Comparators

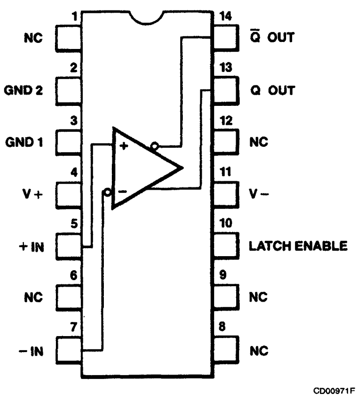
Description

The μA6685 is an ultra fast single voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (2.7 ns) with excellent matching characteristics. The comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50 Ω transmission lines. The low input offsets and short delays make this comparator especially suitable for high speed precision analog to digital processing.

The μA6685 is lead compatible with the AM6685 and functionally compatible with AD9685 and SP9685.

- **2.7 ns Typical Propagation Delay**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**
- **Built-In Latch**
- **Typical Output Skew 0.2 ns**
- **Propagation Delay Constant With Overdrive**

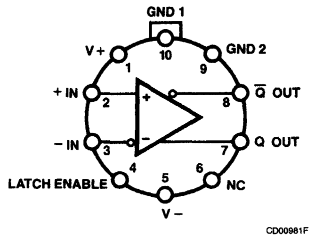
Connection Diagram SO-14 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA6685SV	KD	Molded Surface Mount

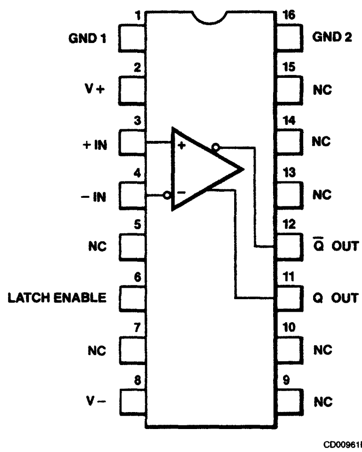
Connection Diagram 10-Lead Metal Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA6685HM	5X	Metal
μA6685HV	5X	Metal

Connection Diagram 16-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA6685DM	6B	Ceramic DIP
μA6685DV	6B	Ceramic DIP
μA6685PV	9B	Molded DIP

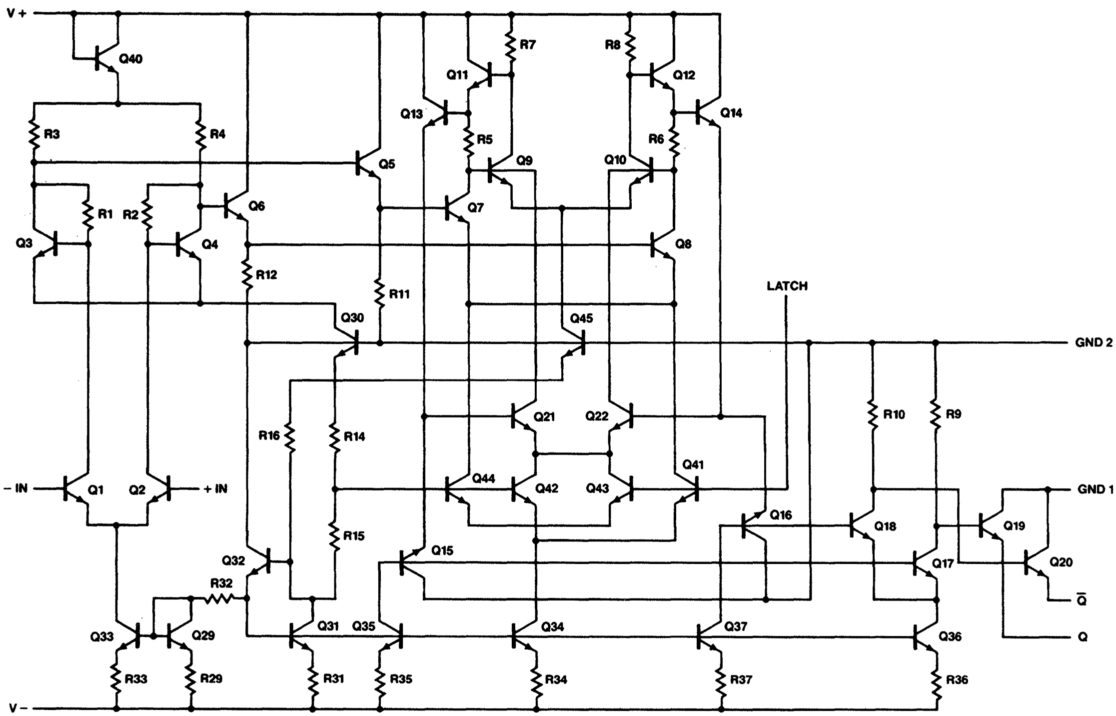
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA6685M)	-55°C to +125°C
Industrial (μA6685V)	-30°C to +85°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
SO-14	0.93
Positive Supply Voltage	+7.0 V
Negative Supply Voltage	-7.0 V
Input Voltage	±4.0 V
Differential Input Voltage	±6.0 V
Output Current	30 mA
Minimum Operating Voltage (V+ to V−)	9.7 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 16L-Ceramic DIP at 10 mW/°C, the 16L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Equivalent Circuit



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μA6685V, μA6685M

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]	μA6685V			μA6685M			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$R_S \leq 100\ \Omega$, $T_A = 25°C$	-3.0	0.3	+3.0	-2.0	0.3	+2.0	mV
		$R_S \leq 100\ \Omega$	-3.5		+3.5	-3.0		+3.0	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ \Omega$		4.0			4.0		μV/°C
I_{IO}	Input Offset Current[2]	$25°C \leq T_A \leq T_{A\ Max}$	-1.0	0.2	+1.0	-1.0	0.2	+1.0	μA
		$T_A = T_{A\ Min}$	-1.3	0.3	+1.3	-1.6	0.3	+1.6	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\ Max}$		4.0	10		4.0	10	μA
		$T_A = T_{A\ Min}$		7.0	13		8.0	16	
V_{CM}	Common Mode Voltage Range		-3.3		+3.3	-3.3		+3.3	V
CMR	Common Mode Rejection	$R_S \leq 100\ \Omega$, $-3.3\ V \leq V_{CM} \leq +3.3\ V$	80			80			dB
PSRR	Power Supply Rejection Ratio[2]	$R_S \leq 100\ \Omega$, $\Delta V_S = \pm 5\%$	70			70			dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	-0.960	-0.885	-0.810	-0.960	-0.885	-0.810	V
		$T_A = T_{A\ Min}$	-1.060	-0.975	-0.890	-1.100	-1.010	-0.920	
		$T_A = T_{A\ Max}$	-0.890	-0.795	-0.700	-0.850	-0.735	-0.620	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	-1.850	-1.750	-1.650	-1.850	-1.750	-1.650	V
		$T_A = T_{A\ Min}$	-1.890	-1.783	-1.675	-1.910	-1.800	-1.690	
		$T_A = T_{A\ Max}$	-1.825	-1.725	-1.625	-1.810	-1.693	-1.575	
I+	Positive Supply Current			15	22		15	22	mA
I–	Negative Supply Current			12	26		12	26	mA
P_c	Power Consumption[3]			180	300		180	300	mW

Switching Characteristics $V_{in} = 100$ mV, $V_{OD} = 10$ mV

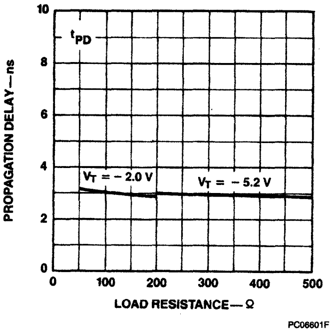
Symbol	Characteristic[2]	Condition[1]	μA6685V			μA6685M			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{PD}+$, $t_{PD}-$	Propagation Delay	$T_A = 25°C$		2.7	4.0		2.7	4.0	ns
$t_{PD}+(E)$, $t_{PD}-(E)$	Latch Enable to Output (HIGH or LOW) Delay	$T_A = 25°C$		2.0	2.5		2.0	2.5	ns
t_S	Min Latch Set up Time	$T_A = 25°C$		0.5	1.0		0.5	1.0	ns
t_h	Min Latch Hold Time	$T_A = 25°C$		0.5	1.0		0.5	1.0	ns

Notes

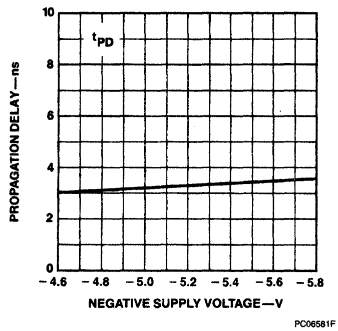
1. Unless otherwise specified V+ = 6.0 V, V– = –5.2 V, $V_T = -2.0$ V and $R_L = 50\ \Omega$, all switching characteristics are for a 100 mV input step with 10 mV overdrive. The specification given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, $t_{PD}+$, and $t_{PD}-$ apply for ± 5% supply voltages. The μA6685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
2. Guaranteed but not tested in production.
3. Refer to Internal Power Dissipation in Absolute Maximum Rating Table.

Typical Performance Curves $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 10$ mV, unless otherwise specified.

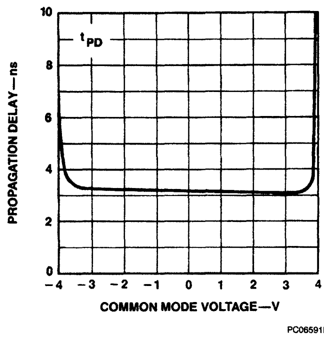
Propagation Delays vs Load Resistance



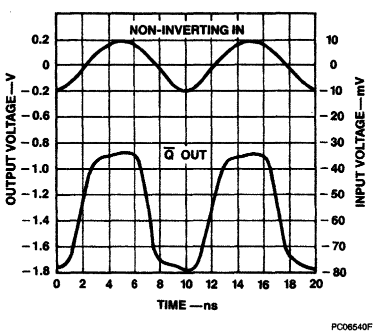
Propagation Delays vs Negative Supply Voltage



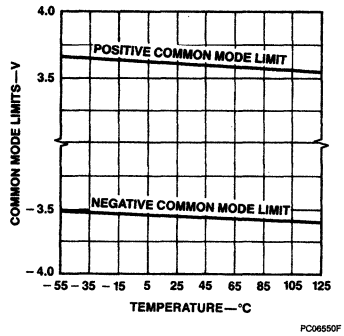
Propagation Delays vs Common Mode Voltage



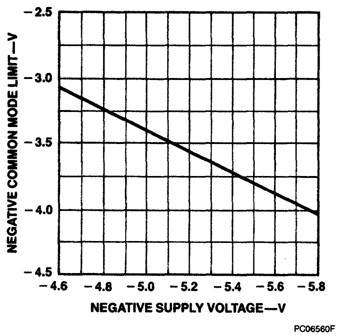
Response to 100 MHz Sine Wave



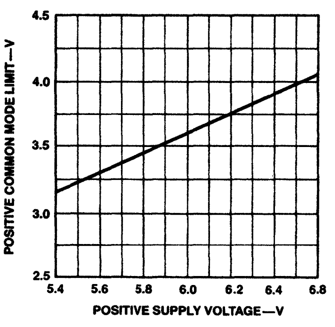
Common Mode Limits vs Temperature



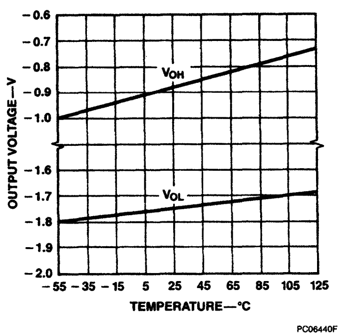
Negative Common Mode Limit vs Negative Supply Voltage



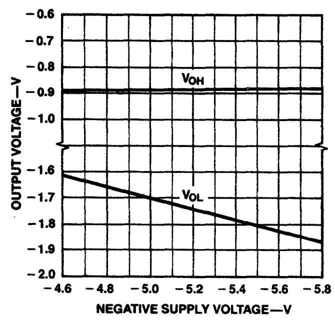
Positive Common Mode Limit vs Positive Supply Voltage



Output Levels vs Temperature

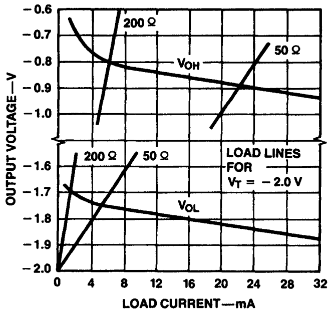


Output Levels vs Negative Supply Voltage



Typical Performance Curves (Cont.) $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 10$ mV, unless otherwise specified.

Output Levels vs DC Loading



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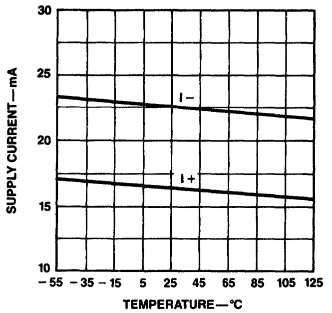
Supply Currents vs Temperature



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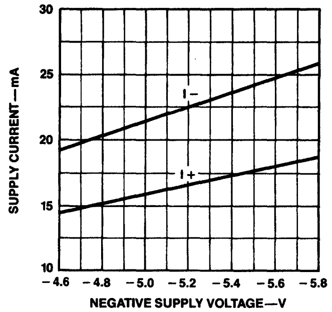
Supply Currents vs Negative Supply Voltage



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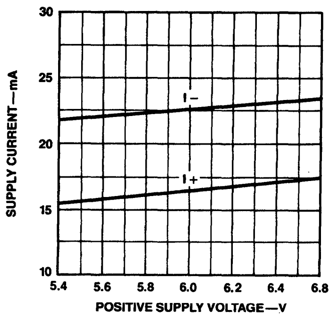
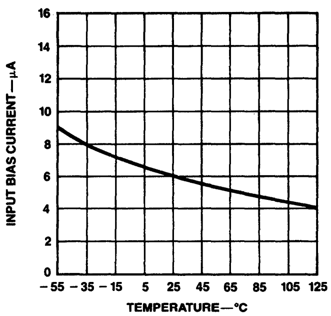
Supply Currents vs Positive Supply Voltage



PC06490F

Input Bias Current vs Temperature



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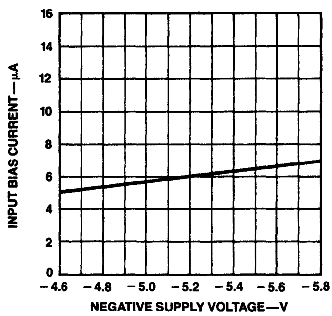
Input Bias Current vs Negative Supply Voltage



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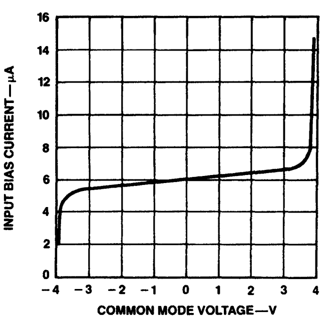
Input Bias Current vs Common Mode Voltage



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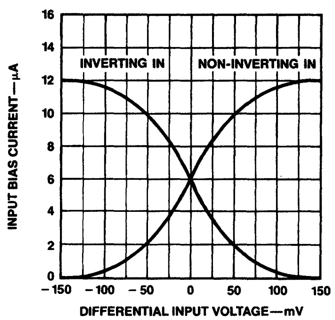
Input Current vs Differential Input Voltage



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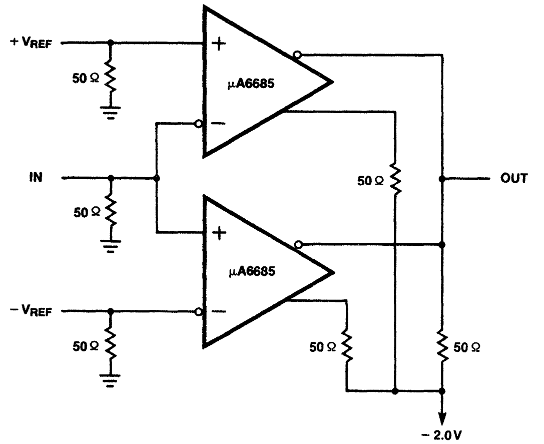
Typical Applications (T_A = 25°C)

High Speed Window Detector



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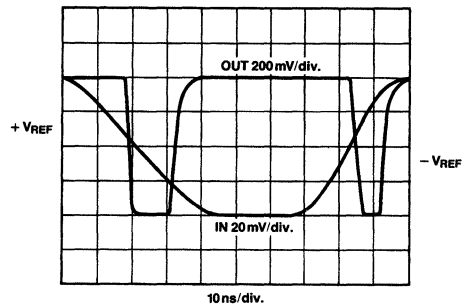
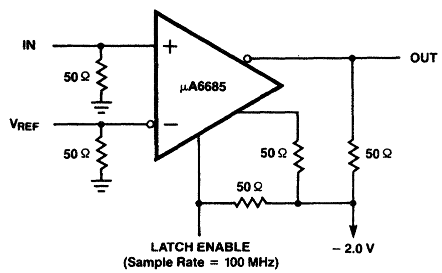


CR02100F

High Speed Sampling



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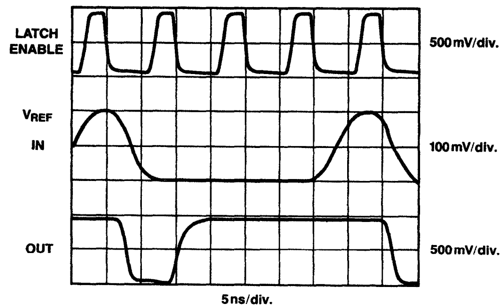

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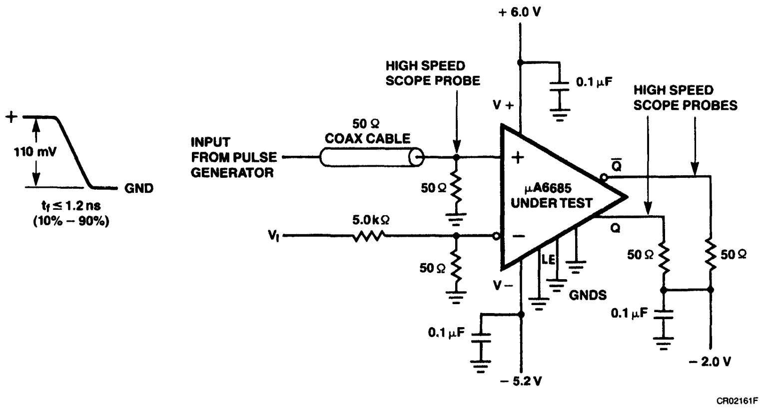
Measurement Of Propagation Delay



Propagation delays $t_{PD}+$ (Q̄ output) and $t_{PD}-$ (Q output) are measured with input signal conditions of a 100 mV step with an overdrive of 10 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting V_I until outputs are in the linear region while the Pulse Generator is disconnected. V_I is then increased in the positive direction so inverting input changes by 10 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +110 mV to 0 V swing, with a $t_{PD}+$ or $t_{PD}-$ reading taken between the +10 mV level of the input pulse and the 50% point of the outputs.

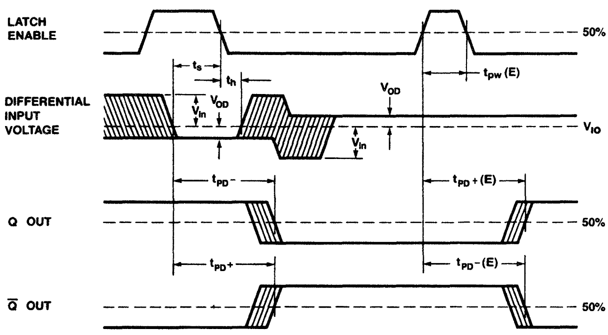
Thermal Considerations

To achieve the high speed of the μA6685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the μA6685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the μA6685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

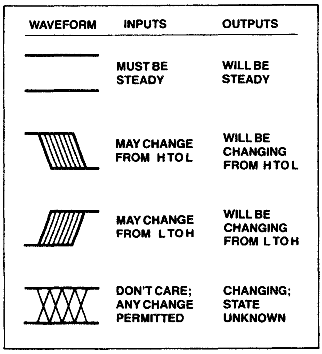
Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The μA6685 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0 V, but a Thevenin equivalent to V− can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

Timing Diagram



Key To Timing Diagram



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Note
The set up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_h will not be detected. Changes between t_S and t_h may or may not be detected.

Definition Of Terms

V_{IO} **Input Offset Voltage** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{IO}/\Delta T$ **Average Temperature Coefficient Of Input Offset Voltage** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{IO} **Input Offset Current** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_{IB} **Input Bias Current** — The average of the two input currents.

R_I **Input Resistance** — The resistance looking into either input terminal with the other grounded.

C_I **Input Capacitance** — The capacitance looking into either input terminal with the other grounded.

V_{CM} **Common Mode Voltage Range** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMR **Common Mode Rejection** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

PSRR **Power Supply Rejection Ratio** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **Output Voltage HIGH** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **Output Voltage LOW** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I+ **Positive Supply Current** — The current required from the positive supply to operate the comparator.

I– **Negative Supply Current** — The current required from the negative supply to operate the comparator.

P_c **Power Consumption** — The power dissipated by the comparator with both outputs terminated in 50 Ω to −2.0 V.

Switching Terms (see Timing Diagram)

t_{PD+} **Input To Output HIGH Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{PD-} **Input To Output LOW Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{PD+(E)}$ **Latch Enable To Output HIGH Delay** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{PD-(E)}$ **Latch Enable To Output LOW Delay** — The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_S **Minimum Set up Time** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **Minimum Latch Enable Pulse Width** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A	Ambient temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_{CC}	Supply voltages	V_{in}	Input pulse amplitude
V+	Positive supply voltage	V_{OD}	Input overdrive
V−	Negative supply voltage	f	Frequency

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μA6687 Ultra Fast Voltage Comparators

Linear Division Comparators

Description

The μA6687 is an ultra fast dual voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (2.7 ns) with excellent matching characteristics. These comparators have differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50 Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high speed precision analog-to-digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample and hold mode. The latch function inputs are designed to be driven from the complementary outputs of a standard ECL gate. If latch enable is HIGH and $\overline{\text{latch enable}}$ is LOW, the comparator functions normally. When latch enable is driven LOW and $\overline{\text{latch enable}}$ is driven HIGH, the comparator outputs are locked in their existing logical states. Should the latch function not be used, latch enable must be connected to ground.

The μA6687 is lead compatible with the AM6687 and with the AD9687 and SP9687.

- **2.7 ns Typical Propagation Delay At 10 mV Overdrive**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**
- **1.0 ns Latch Set up Time**

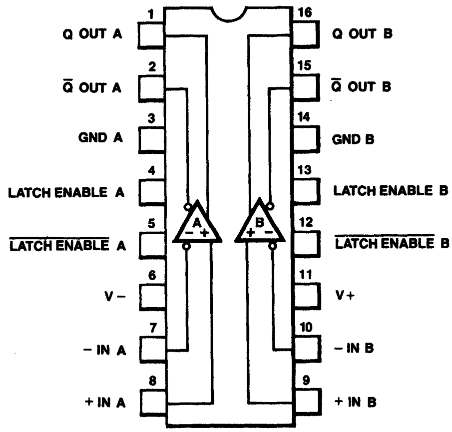
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA6687M)	-55°C to +125°C
Industrial (μA6687V)	-30°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Positive Supply Voltage	+7.0 V
Negative Supply Voltage	-7.0 V
Input Voltage	±4.0 V
Differential Input Voltage	±6.0 V
Output Current	30 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



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Order Information

Device Code	Package Code	Package Description
μA6687DM	6B	Ceramic DIP
μA6687DV	6B	Ceramic DIP
μA6687PV	9B	Molded DIP

Electrical Characteristics Over the recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]	μA6687V Min.	μA6687V Max.	μA6687M Min.	μA6687M Max.	Units
V_{IO}	Input Offset Voltage	$R_S \leq 100\ \Omega$, $T_A = 25°C$	-2.0	+2.0	-2.0	+2.0	mV
		$R_S \leq 100\ \Omega$	-3.0	+3.0	-3.0	+3.0	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage[2]	$R_S \leq 100\ \Omega$	-10	+10	-10	+10	μV/°C
I_{IO}	Input Offset Current[2]	$25°C \leq T_A \leq T_{A\ Max}$	-1.0	+1.0	-1.0	+1.0	μA
		$T_A = T_{A\ Min}$	-1.3	+1.3	-1.6	+1.6	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\ Max}$		10		10	μA
		$T_A = T_{A\ Min}$		13		16	
V_{CM}	Input Common Mode Range		-3.3	+2.7	-3.3	+2.7	V
CMR	Common Mode Rejection	$R_S \leq 100\ \Omega$, $-3.3\ V \leq V_{CM} \leq +2.7\ V$	80		80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\ \Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	-0.960	-0.810	-0.960	-0.810	V
		$T_A = T_{A\ Min}$	-1.060	-0.890	-1.100	-0.920	
		$T_A = T_{A\ Max}$	-0.890	-0.700	-0.850	-0.620	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	-1.850	-1.650	-1.850	-1.650	V
		$T_A = T_{A\ Min}$	-1.890	-1.675	-1.910	-1.690	
		$T_A = T_{A\ Max}$	-1.825	-1.625	-1.810	-1.575	
I+	Positive Supply Current			32		32	mA
I-	Negative Supply Current			44		44	mA
P_C	Power Consumption			450		450	mW

Switching Characteristics ($V_{in} = 100$ mV, $V_{OD} = 10$ mV)

Symbol	Characteristic	Condition[1]	μA6687V Min.	μA6687V Max.	μA6687M Min.	μA6687M Max.	Units
t_{PD+}, t_{PD-}	Propagation Delay[2]	$T_A = 25°C$		4.0		4.0	ns
t_S	Minimum Latch Set Up Time[2]	$T_A = 25°C$		1.0		1.0	ns

Notes

1. Unless otherwise specified V+ = +5.0 V, V− = −5.2 V, $V_T = -2.0$ V, and $R_L = 50\ \Omega$; all switching characteristics are for a 100 mV input step with 10 mV overdrive. The specifications given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, t_{PD+} and t_{PD-} apply over the full V_{CM} range and for ±5% supply voltages.
2. Guaranteed, but not tested in production.

FAIRCHILD

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μA685
High Speed
Single Latched Comparator

Linear Division Comparators

Description

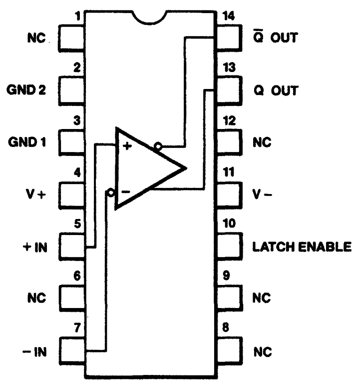
The μA685 is a fast voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays without sacrificing the excellent matching characteristics formerly associated only with slow, high performance linear ICs. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50 Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high speed precision analog to digital processing.

A latch function is provided to allow the comparator to be used in a sample and hold mode. If the latch enable is HIGH, the comparator functions normally. When the latch enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the latch enable must be connected to ground.

The μA685 is lead compatible with the AM685.

- **6.5 ns Maximum Propagation Delay At 5.0 mV Overdrive**
- **3.0 ns Latch Set up Time**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**
- **Typical Output Skew 0.2 ns**
- **Constant Propagation Delay With Overdrive**

Connection Diagram
SO-14 Package
(Top View)



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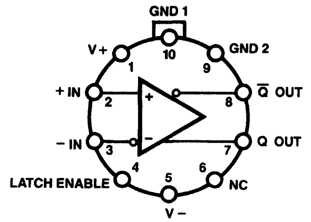
Order Information

Device Code	Package Code	Package Description
μA685SV	KD	Molded Surface Mount

Connection Diagram
10-Lead Metal Package
(Top View)

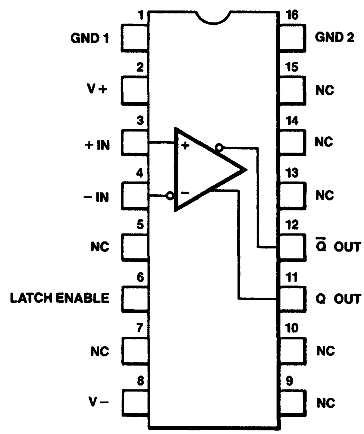


CD00981F

Order Information

Device Code	Package Code	Package Description
μA685HM	5X	Metal
μA685HV	5X	Metal

Connection Diagram
16-Lead DIP
(Top View)



CD00961F

Order Information

Device Code	Package Code	Package Description
μA685DM	6B	Ceramic DIP
μA685DV	6B	Ceramic DIP
μA685PV	9B	Molded DIP

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Extended (μA685M)	−55°C to +125°C
Industrial (μA685V)	−30°C to +85°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C

Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
SO-14	0.93 W
Positive Supply Voltage	+7.0 V
Negative Supply Voltage	−7.0 V
Input Voltage	±4.0 V
Differential Input Voltage	±6.0 V
Output Current	30 mA
Minimum Operating Voltage (V+ to V−)	9.7 V

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 16L-Ceramic DIP at 10 mW/°C, the 16L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

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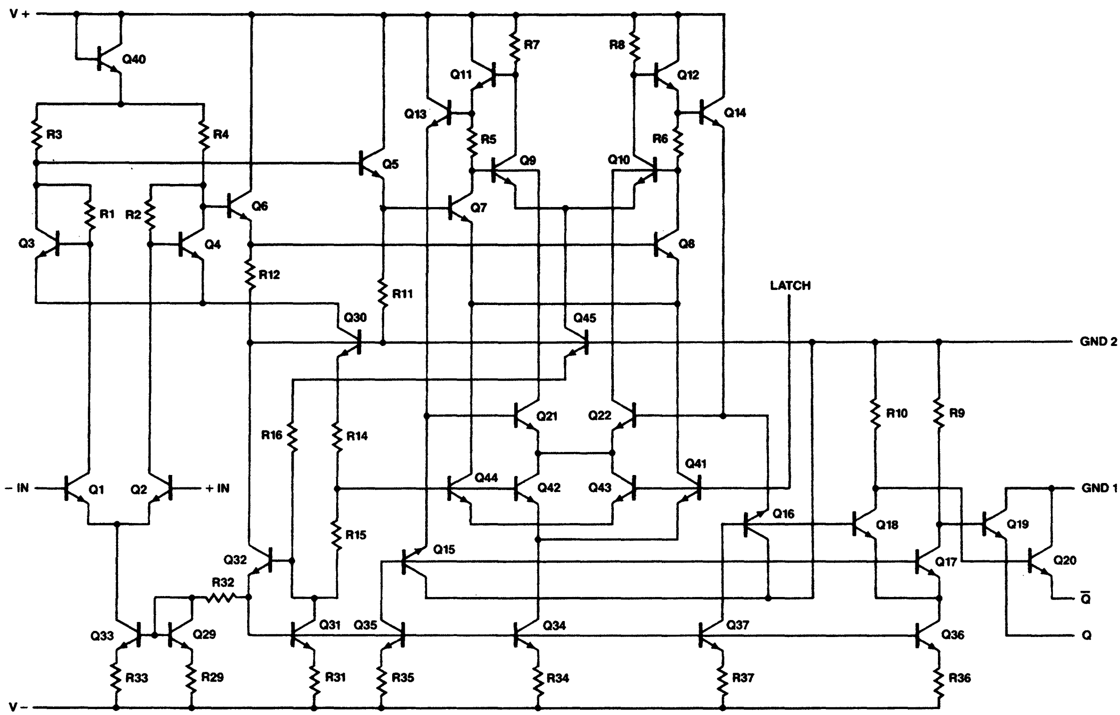
Equivalent Circuit



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μA685

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[2]	μA685V		μA685M		Units
			Min.	Max.	Min.	Max.	
V_{IO}	Input Offset Voltage	$R_S \leqslant 100\ \Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leqslant 100\ \Omega$	−2.5	+2.5	−3.0	+3.0	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage[3]	$R_S \leqslant 100\ \Omega$	−10	+10	−10	+10	μV/°C
I_{IO}	Input Offset Current[3]	$25°C \leqslant T_A \leqslant T_{A\ Max}$	−1.0	+1.0	−1.0	+1.0	μA
		$T_A = T_{A\ Min}$	−1.3	+1.3	−1.6	+1.6	
I_{IB}	Input Bias Current	$25°C \leqslant T_A \leqslant T_{A\ Max}$		10		10	μA
		$T_A = T_{A\ Min}$		13		16	
R_I	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_I	Input Capacitance[1]	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Common Mode Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMR	Common Mode Rejection	$R_S \leqslant 100\ \Omega$, $-3.3 \leqslant V_{CM} \leqslant +3.3V$	80		80		dB
PSRR	Power Supply Rejection Ratio[3]	$R_S \leqslant 100\ \Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A\ Min}$	−1.060	−0.890	−1.100	−0.920	
		$T_A = T_{A\ Max}$	−0.890	−0.700	−0.850	−0.620	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A\ Min}$	−1.890	−1.675	−1.910	−1.690	
		$T_A = T_{A\ Max}$	−1.825	−1.625	−1.810	−1.575	
I+	Positive Supply Current			22		22	mA
I−	Negative Supply Current			26		26	mA
P_c	Power Consumption[4]			300		300	mW

Switching Characteristics $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV

Symbol	Characteristic	Condition[2]	μA685V		μA685M		Units
			Min.	Max.	Min.	Max.	
t_{PD+}	Input to Output HIGH[3]	$T_{A\ Min} \leqslant T_A \leqslant 25°C$		6.5		6.5	ns
		$T_A = T_{A\ Max}$		9.5		12	
t_{PD-}	Input to Output LOW[3]	$T_{A\ Min} \leqslant T_A \leqslant 25°C$		6.5		6.5	ns
		$T_A = T_{A\ Max}$		9.5		12	

μ**A685** (Cont.)
Electrical Characteristics

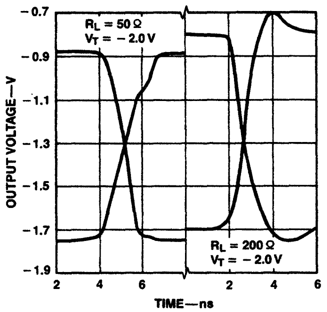
Switching Characteristics $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV

Symbol	Characteristic	Condition[2]	μA685V Min.	μA685V Max.	μA685M Min.	μA685M Max.	Units
t_{PD+}(E)	Latch Enable to Output HIGH Delay[3]	$T_{A\ Min} \leq T_A \leq 25°C$		6.5		6.5	ns
		$T_A = T_{A\ Max}$		9.5		12	
t_{PD-}(E)	Latch Enable to Output LOW Delay[3]	$T_{A\ Min} \leq T_A \leq 25°C$		6.5		6.5	ns
		$T_A = T_{A\ Max}$		9.5		12	
t_S	Minimum Set up Time[3]	$T_{A\ Min} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A\ Max}$		4.0		6.0	
t_h	Minimum Hold Time[3]	$T_{A\ Min} \leq T_A \leq T_{A\ Max}$		1.0		1.0	ns
t_{pw}(E)	Minimum Latch Enable Pulse Width[3]	$T_{A\ Min} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A\ Max}$		4.0		5.0	

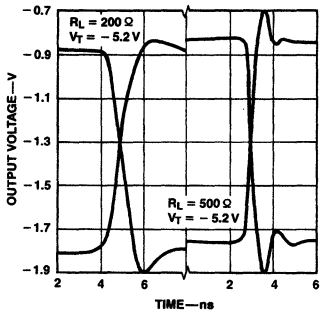
Notes
1. For TO-99 only; CERDIP = 7.0 pF.
2. Unless otherwise specified V+ = 6.0 V, V− = −5.2 V, $V_T = -2.0$ V, and $R_L = 50\ \Omega$; all switching characteristics are for a 100 mV input step with 5.0 mV overdrive. The specifications given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, t_{PD+} and t_{PD-} apply over the full V_{CM} range and for ±5% supply voltages. The μA685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
3. Guaranteed, but not tested in production.
4. Refer to Internal Power Dissipation in Absolute Maximum Rating Table.

Typical Performance Curves $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

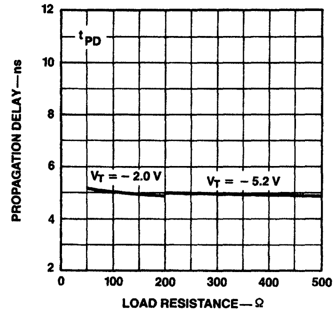
Response for Various Load Resistances



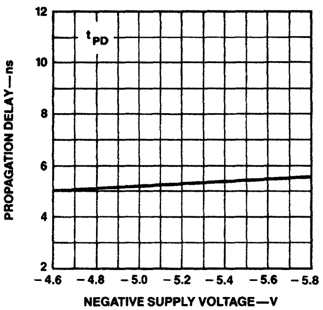
Response for Various Load Resistances



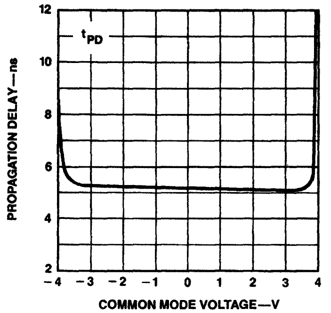
Propagation Delay vs Load Resistance



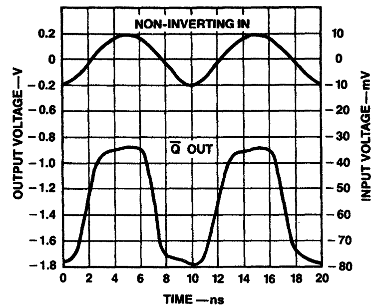
Propagation Delay vs Negative Supply Voltage



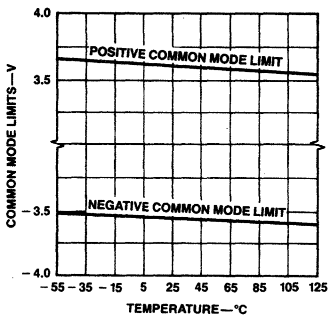
Propagation Delay vs Common Mode Voltage



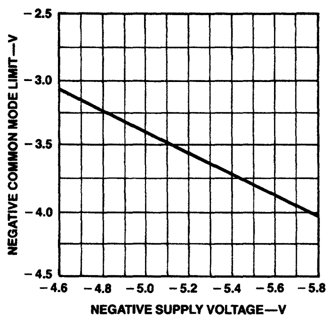
Response to 100 MHz Sine Wave



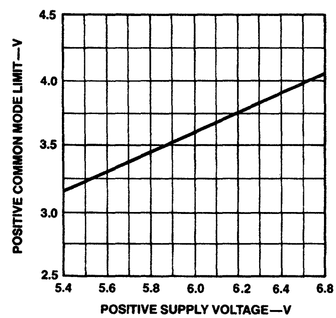
Common Mode Limits vs Temperature



Negative Common Mode Limit vs Negative Supply Voltage

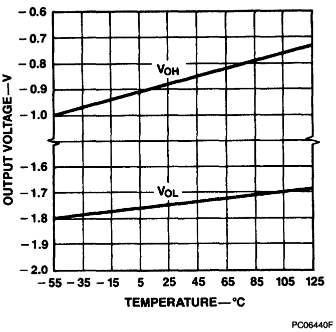


Positive Common Mode Limit vs Positive Supply Voltage

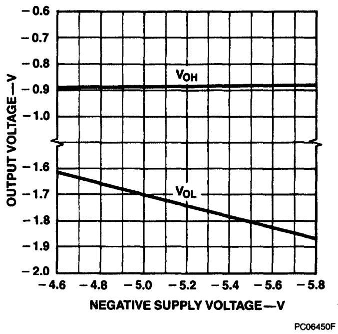


Typical Performance Curves (Cont.) $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

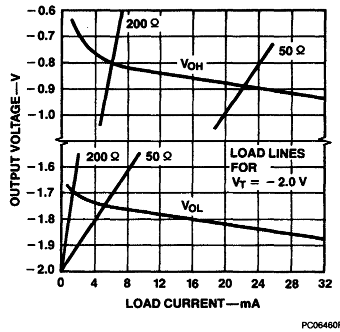
Output Levels vs Temperature



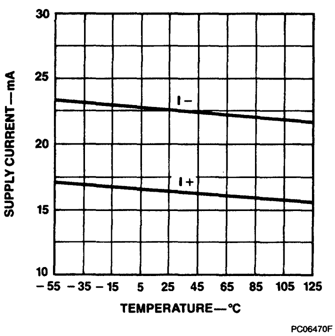
Output Levels vs Negative Supply Voltage



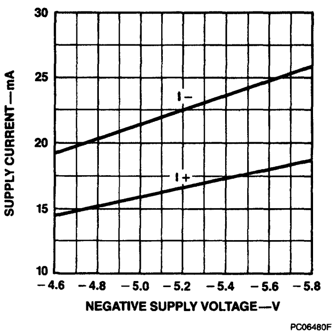
Output Levels vs DC Loading



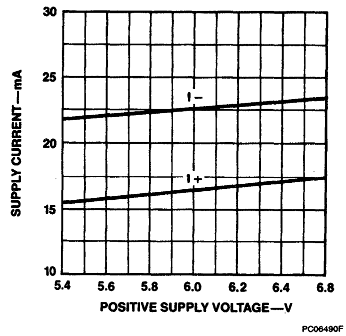
Supply Currents vs Temperature



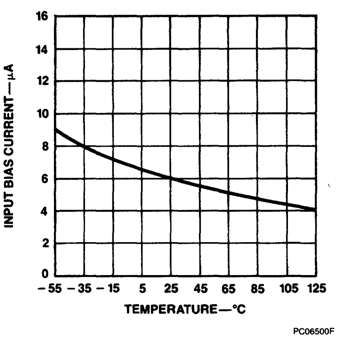
Supply Currents vs Negative Supply Voltage



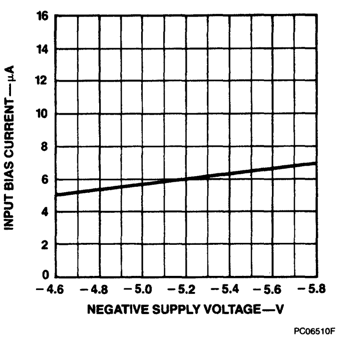
Supply Currents vs Positive Supply Voltage



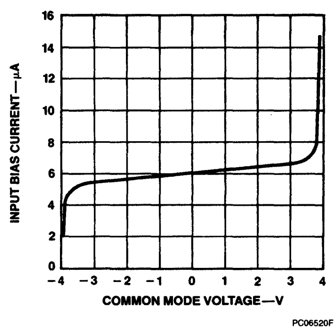
Input Bias Current vs Temperature



Input Bias Current vs Negative Supply Voltage

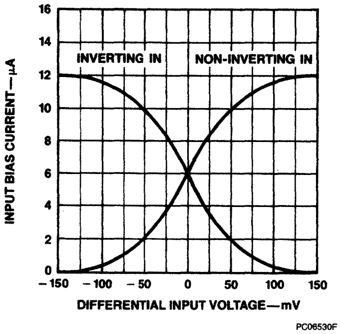


Input Bias Current vs Common Mode Voltage



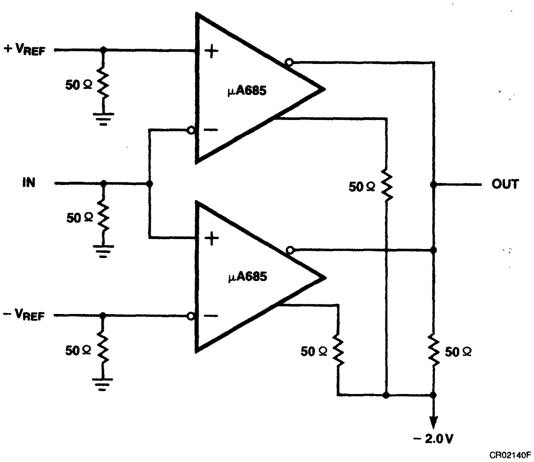
Typical Performance Curves (Cont.) $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

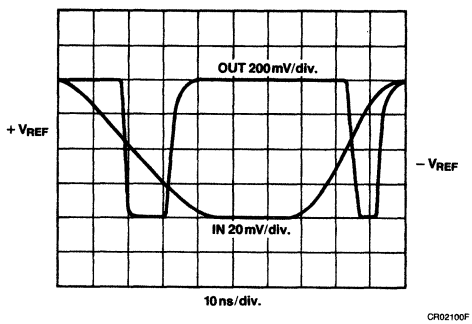
Input Current vs Differential Input Voltage



Typical Applications ($T_A = 25°C$)

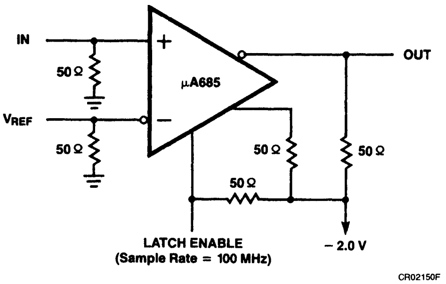
High Speed Window Detector

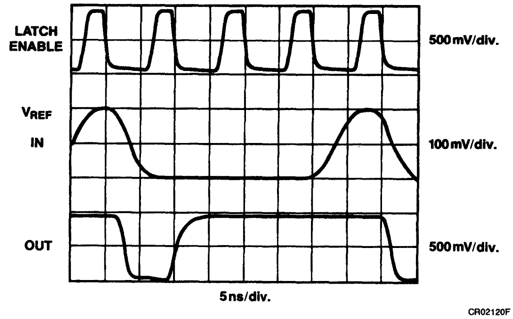




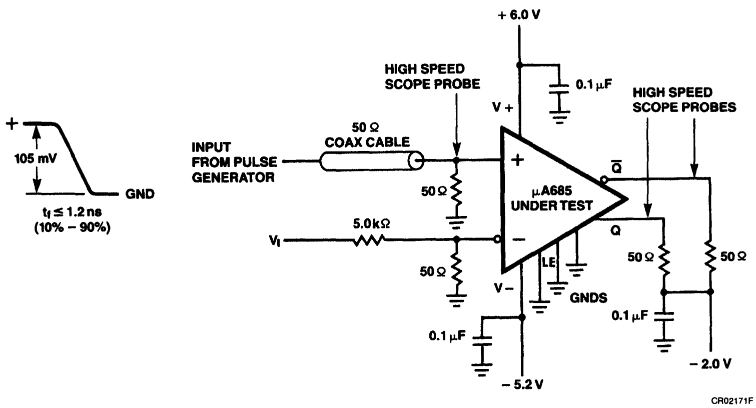
Typical Applications (Cont.)

High Speed Sampling





Measurement Of Propagation Delay



Propagation delays $t_{PD}+$ ($\overline{Q}$ output) and $t_{PD}-$ (Q output) are measured with input signal conditions of a 100 mV step with an overdrive of 5.0 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting V_I until outputs are in the linear region while the Pulse Generator is disconnected. V_I is then increased in the positive direction so inverting input changes by 5.0 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +105 mV to 0 V swing, with a $t_{PD}+$ or $t_{PD}-$ reading taken between the +5.0 mV level of the input pulse and the 50% point of the outputs.

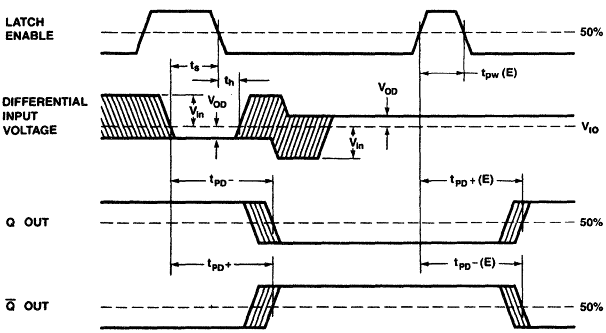
Thermal Considerations

To achieve the high speed of the μA685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the μA685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the μA685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

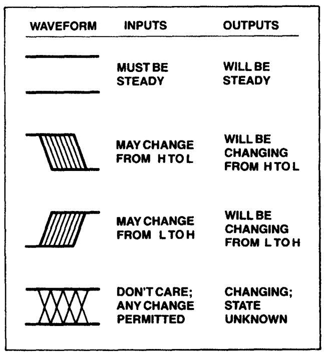
Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The μA685 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0 V, but a Thevenin equivalent to V− can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

Timing Diagram



Key To Timing Diagram



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Note

The set up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_h will not be detected. Changes between t_S and t_h may or may not be detected.

Definition Of Terms

V_{IO} **Input Offset Voltage** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{IO}/\Delta T$ **Average Temperature Coefficient Of Input Offset Voltage** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{IO} **Input Offset Current** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_{IB} **Input Bias Current** — The average of the two input currents.

R_I **Input Resistance** — The resistance looking into either input terminal with the other grounded.

C_I **Input Capacitance** — The capacitance looking into either input terminal with the other grounded.

V_{CM} **Common Mode Voltage Range** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMR **Common Mode Rejection** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

PSRR **Power Supply Rejection Ratio** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **Output Voltage HIGH** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **Output Voltage LOW** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I+ **Positive Supply Current** — The current required from the positive supply to operate the comparator.

I– **Negative Supply Current** — The current required from the negative supply to operate the comparator.

P_c **Power Consumption** — The power dissipated by the comparator with both outputs terminated in 50 Ω to −2.0 V.

Switching Terms (see Timing Diagram)

t_{PD+} **Input To Output HIGH Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{PD-} **Input To Output LOW Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{PD+(E)}$ **Latch Enable To Output HIGH Delay** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{PD-(E)}$ **Latch Enable To Output LOW Delay** — The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_S **Minimum Set up Time** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **Minimum Latch Enable Pulse Width** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A	Ambient temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_{CC}	Supply voltages	V_{in}	Input pulse amplitude
V+	Positive supply voltage	V_{OD}	Input overdrive
V–	Negative supply voltage	f	Frequency

FAIRCHILD

A Schlumberger Company

μA687 • μA687A Dual Voltage Comparators

Description

The μA687 and μA687A are fast dual voltage comparators manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (8.0 ns) with excellent matching characteristics. These comparators have differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capabilities are adequate for driving terminated 50 Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high speed precision analog to digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample and hold mode. The latch function inputs are designed to be driven from the complementary outputs of a standard ECL gate. If latch enable is HIGH and $\overline{\text{latch enable}}$ is LOW, the comparator functions normally. When latch enable is driven LOW and $\overline{\text{latch enable}}$ is driven HIGH, the comparator outputs are locked in their existing logical states. Should the latch function not be used, latch enable must be connected to ground.

The μA687 and μA687A are lead compatible with the AM687.

- **8.0 ns Maximum Propagation Delay At 5 mV Overdrive**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**

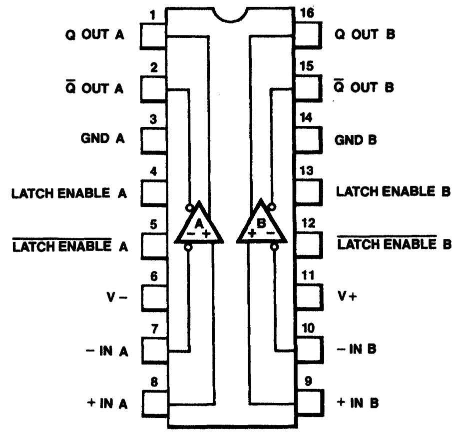
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA687M/AM)	-55°C to +125°C
Industrial (μA687V/AV)	-30°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Positive Supply Voltage	+7.0 V
Negative Supply Voltage	-7.0 V
Input Voltage	±4.0 V
Differential Input Voltage	±6.0 V
Output Current	30 mA
Minimum Operating Voltage (V+ to V–)	9.7 V

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



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Order Information

Device Code	Package Code	Package Description
μA687DM	6B	Ceramic DIP
μA687DV	6B	Ceramic DIP
μA687PV	9B	Molded DIP
μA687ADM	6B	Ceramic DIP
μA687ADV	6B	Ceramic DIP
μA687APV	9B	Molded DIP

μA687/AV, μA687AM
Electrical Characteristics Over the recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]	μA687/AV		μA687/AM		Units
			Min.	Max.	Min.	Max.	
V_{IO}	Input Offset Voltage	$R_S \leq 100\ \Omega$, $T_A = 25°C$	-3.0	+3.0	-2.0	+2.0	mV
		$R_S \leq 100\ \Omega$	-3.5	+3.5	-3.0	+3.0	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage[2]	$R_S \leq 100\ \Omega$	-10	+10	-10	+10	μV/°C
I_{IO}	Input Offset Current[2]	$25°C \leq T_A \leq T_{A\ Max}$	-1.0	+1.0	-1.0	+1.0	μA
		$T_A = T_{A\ Min}$	-1.3	+1.3	-1.6	+1.6	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\ Max}$		10		10	μA
		$T_A = T_{A\ Min}$		13		16	
V_{CM}	Common Mode Voltage Range		-3.3	+2.7	-3.3	+2.7	V
CMR	Common Mode Rejection	$R_S \leq 100\ \Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\ \Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	-0.960	-0.810	-0.960	-0.810	V
		$T_A = T_{A\ Min}$	-1.060	-0.890	-1.100	-0.920	
		$T_A = T_{A\ Max}$	-0.890	-0.700	-0.850	-0.620	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	-1.850	-1.650	-1.850	-1.650	V
		$T_A = T_{A\ Min}$	-1.890	-1.675	-1.910	-1.690	
		$T_A = T_{A\ Max}$	-1.825	-1.625	-1.810	-1.575	
I+	Positive Supply Current			35		32	mA
I−	Negative Supply Current			48		44	mA
P_C	Power Consumption			485		450	mW

Switching Characteristics $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV

Symbol	Characteristic	Condition[1]	μA687/AV		μA687/AM		Units
			Min.	Max.	Min.	Max.	
t_{PD}	Propagation Delay (μA687A)[2]	$T_{A\ Min} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A\ Max}$		10		12.5	
t_{PD}	Propagation Delay (μA687)[2]	$T_{A\ Min} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A\ Max}$		14		20	
t_S	Minimum Latch Set Up Time[2]	$T_A = 25°C$		4.0		4.0	ns

Notes

1. Unless otherwise specified V+ = +5.0 V, V− = −5.2 V, $V_T = -2.0$ V, and $R_L = 50\ \Omega$; all switching characteristics are for a 100 mV input step with 5.0 mV overdrive. The specifications given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, t_{PD+} and t_{PD-} apply over the full V_{CM} range and for ±5% supply voltages. The μA687 and μA687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
2. Guaranteed, but not tested in production.

8

FAIRCHILD

A Schlumberger Company

μA710 High Speed Differential Comparator

Linear Division Comparators

Description

The μA710 is a high speed differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar Epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

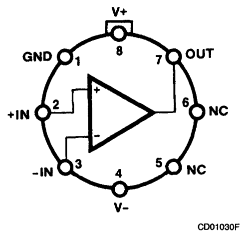
- **5.0 mV Maximum Offset Voltage**
- **5.0 μA Maximum Offset Current**
- **1000 Minimum Voltage Gain**
- **20 μV/°C Maximum Offset Voltage Drift**

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA710M)	-55°C to +125°C
Commercial (μA710C)	0°C to 70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, and the 14L-Molded DIP at 8.3 mW/°C.

Connection Diagram 8-Lead Metal Package (Top View)

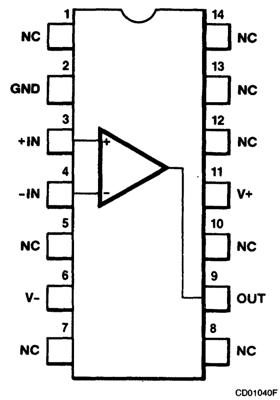


Lead 4 connected to case

Order Information

Device Code	Package Code	Package Description
μA710HM	5W	Metal
μA710HC	5W	Metal

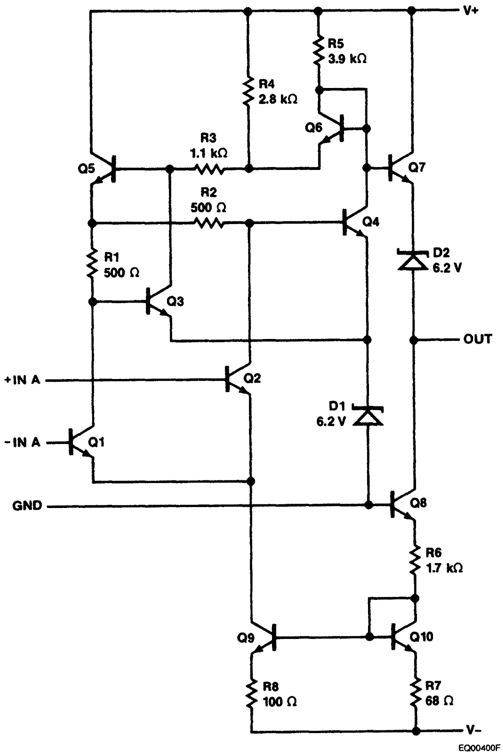
Connection Diagram 14-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA710DM	6A	Ceramic DIP
μA710DC	6A	Ceramic DIP
μA710PC	9A	Molded DIP

Equivalent Circuit



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μA710
Electrical Characteristics $T_A = 25°C$, V+ = 12 V, V− = −6.0 V, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
I_{IO}	Input Offset Current			0.75	3.0	μA
I_{IB}	Input Bias Current			13	20	μA
A_{VS}	Large Signal Voltage Gain		1250	1700		V/V
R_O	Output Resistance			200		Ω
I_{OL}	Output Sink Current	$\Delta V_I \geq 5.0$ mV, $V_O = 0$ V	2.0	2.5		mA
t_{PD}	Response Time[2]			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$						
V_{IO}	Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to 125°C		3.5	10	μV/°C
		$R_S = 50\ \Omega$, $T_A = +25°C$ to −55°C		2.7	10	
I_{IO}	Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
		$T_A = -55°C$		1.8	7.0	
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to 125°C		5.0	25	nA/°C
		$T_A = +25°C$ to −55°C		15	75	
I_{IB}	Input Bias Current	$T_A = -55°C$		27	45	μA
V_{IR}	Input Voltage Range	V− = −7.0 V	±5.0			V
CMR	Common Mode Rejection	$R_S \leq 200\ \Omega$	80	100		dB
V_{IDR}	Differential Input Voltage Range		±5.0			V
A_{VS}	Large Signal Voltage Gain		1000			V/V
V_{OH}	Output Voltage HIGH	$\Delta V_I \geq 5.0$ mV, 0 mA $\leq I_{OH} \leq 5.0$ mA	2.5	3.2	4.0	V
V_{OL}	Output Voltage LOW	$\Delta V_I \geq 5.0$ mV	−1.0	−0.5	0	V
I_{OL}	Output Sink Current	$T_A = +125°C$, $\Delta V_I \geq 5.0$ mV, V_O = GND	0.5	1.7		mA
		$T_A = -55°C$, $\Delta V_I \geq 5.0$ mV, V_O = GND	1.0	2.3		
I+	Positive Supply Current	V_O = GND		5.2	9.0	mA
I−	Negative Supply Current	V_O = GND, Inverting Input = 5.0 mV		4.6	7.0	mA
P_c	Power Consumption	V_O = GND, Inverting Input = 10 mV		90	150	mW

μA710C

Electrical Characteristics $T_A = 25°C$, $V+ = 12$ V, $V- = -6.0$ V, unless otherwise specified.

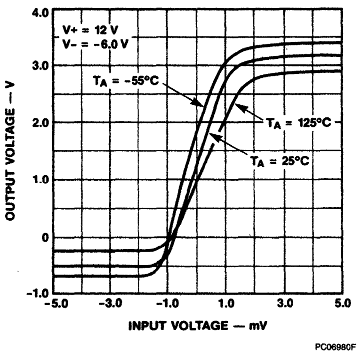
Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
I_{IO}	Input Offset Current			1.8	5.0	μA
I_{IB}	Input Bias Current			16	25	μA
A_{VS}	Large Signal Voltage Gain		1000	1500		V/V
R_O	Output Resistance			200		Ω
I_{OL}	Output Sink Current	$\Delta V_I \geq 5.0$ mV, $V_O = 0$ V	1.6	2.5		mA
t_{PD}	Response Time[2]			40		ns
The following specifications apply for $0°C \leq T_A \leq 70°C$						
V_{IO}	Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $70°C$		5.0	20	μV/°C
I_{IO}	Input Offset Current				7.5	μA
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $70°C$		15	50	nA/°C
		$T_A = 25°C$ to $0°C$		24	100	
I_{IB}	Input Bias Current	$T_A = 0°C$		25	40	μA
V_{IR}	Input Voltage Range	$V- = -7.0$ V	±5.0			V
CMR	Common Mode Rejection	$R_S \leq 200\ \Omega$	70	98		dB
V_{IDR}	Differential Input Voltage Range		±5.0			V
A_{VS}	Large Signal Voltage Gain		800			V/V
V_{OH}	Output Voltage HIGH	$\Delta V_I \geq 5.0$ mV, $0\ mA \leq I_{OH} \leq 5.0$ mA	2.5	3.2	4.0	V
V_{OL}	Output Voltage LOW	$\Delta V_I \geq 5.0$ mV	−1.0	−0.5	0	V
I_{OL}	Output Sink Current	$\Delta V_I \geq 5.0$ mV, $V_O =$ GND	0.5			mA
I+	Positive Supply Current	$V_O =$ GND		5.2	9.0	mA
I−	Negative Supply Current	$V_O =$ GND, Inverting Input = 5.0 mV		4.6	7.0	mA
P_c	Power Consumption	$V_O =$ GND, Inverting Input = 10 mV		90	150	mW

Notes

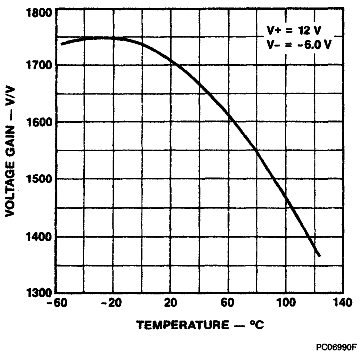
1. The input offset voltage and input offset current are specified for a logic threshold voltage as follows: For μA710, 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C. For μA710C, 1.5 V at 0°C, 1.4 V at 25°C, and 1.2 V at 70°C.
2. The response time specified is for a 100 mV input step with 5.0 mV overdrive.

Typical Performance Curves for μA710

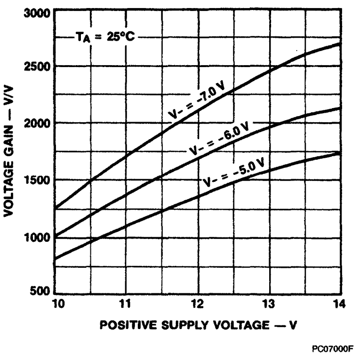
Voltage Transfer Characteristic



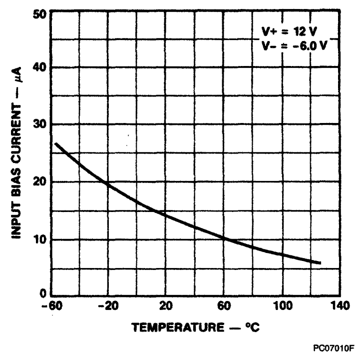
Voltage Gain vs Temperature



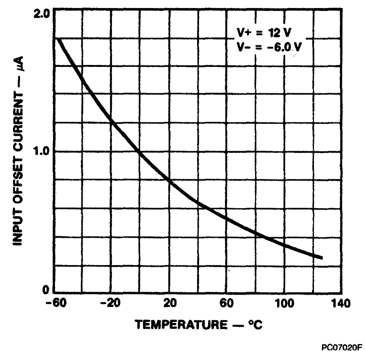
Voltage Gain vs Supply Voltages



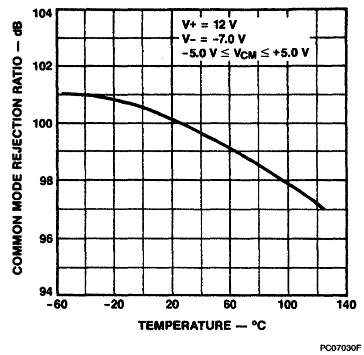
Input Bias Current vs Temperature



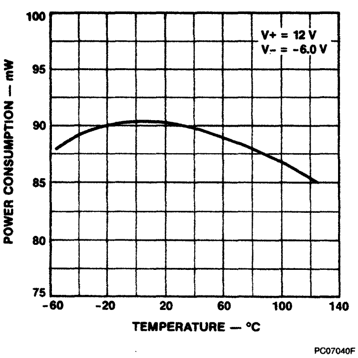
Input Offset Current vs Temperature



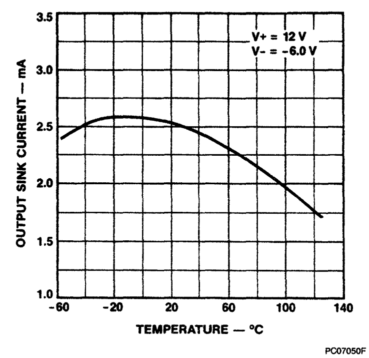
Common Mode Rejection Ratio vs Temperature



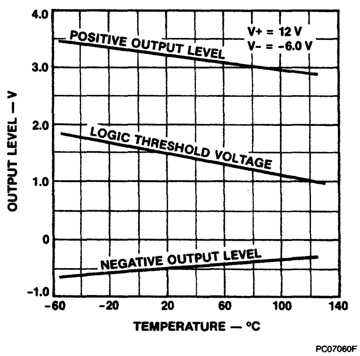
Power Consumption vs Temperature



Output Sink Current vs Temperature

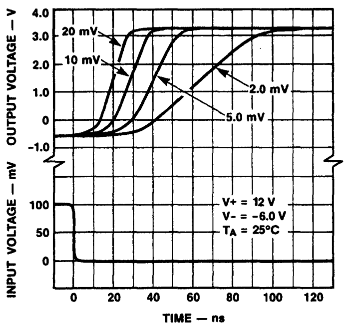


Output Voltage Levels vs Temperature



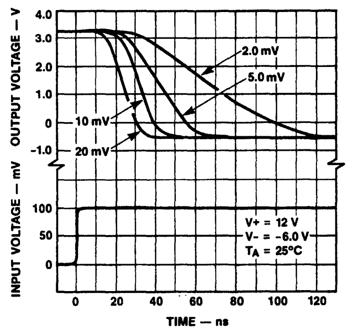
Typical Performance Curves for μA710 (Cont.)

Response Time for Various Input Overdrives



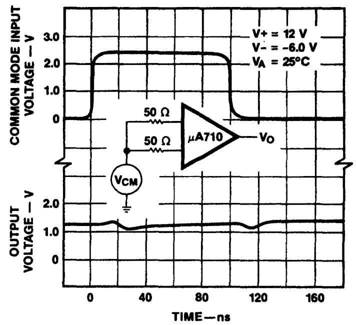
PC07070F

Response Time for Various Input Overdrives



PC07081F

Common Mode Pulse Response

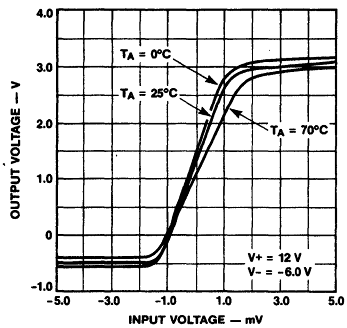


PC07090F

8

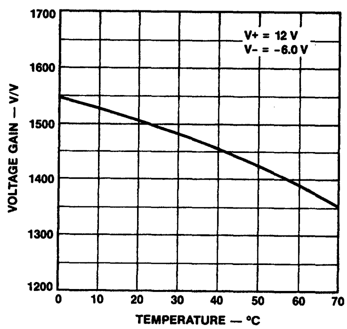
Typical Performance Curves for μA710C

Voltage Transfer Characteristic



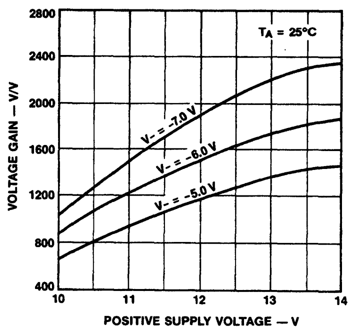
PC07100F

Voltage Gain vs Ambient Temperature



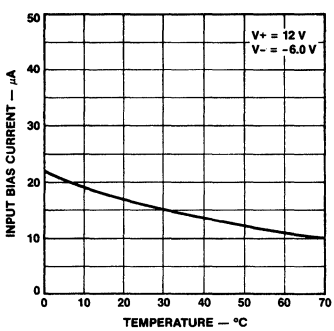
PC07120F

Voltage Gain vs Supply Voltages



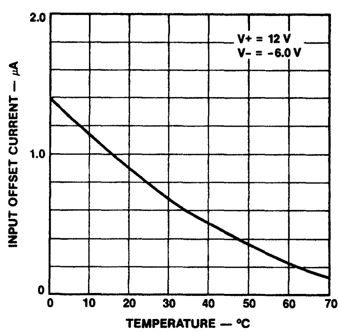
PC07130F

Input Bias Current vs Temperature



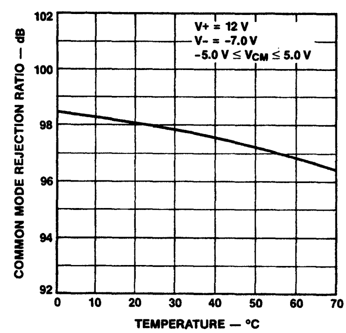
PC07140F

Input Offset Current vs Temperature



PC07150F

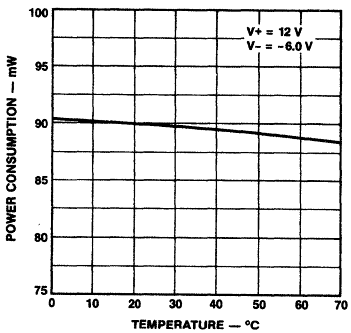
Common Mode Rejection Ratio vs Temperature



PC07160F

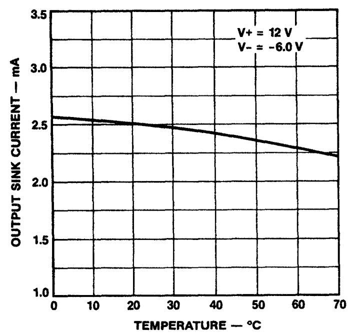
Typical Performance Curves for μA710C (Cont.)

Power Consumption vs Temperature



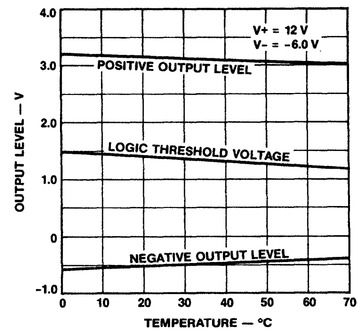
PC07170F

Output Sink Current vs Temperature



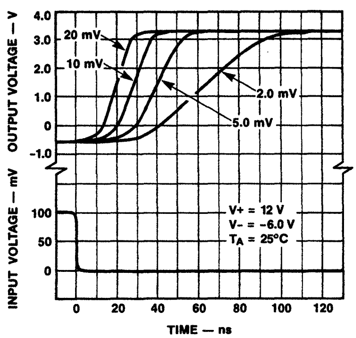
PC07180F

Output Voltage Levels vs Temperature



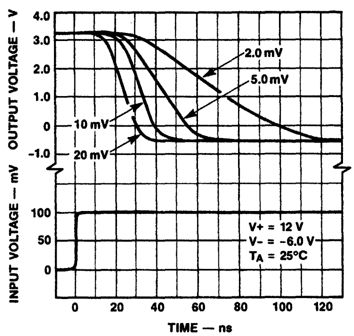
PC07190F

Response Time for Various Input Overdrives



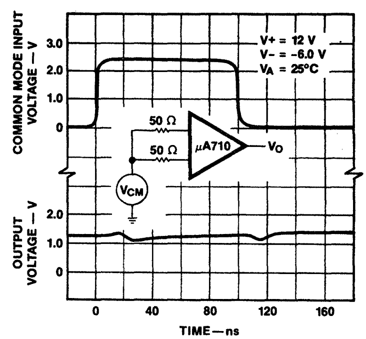
PC07070F

Response Time for Various Input Overdrives



PC07081F

Common Mode Pulse Response



PC07090F

FAIRCHILD

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μA711
Dual High Speed Differential Comparator

Description

The μA711 is a dual high speed differential comparator featuring high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double ended limit detector for automatic Go/No-Go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar Epitaxial process.

- **Fast Response Time — 40 ns Typical**
- **5.0 mV Maximum Offset Voltage**
- **10 μA Maximum Offset Current**
- **Independent Comparator Strobing**

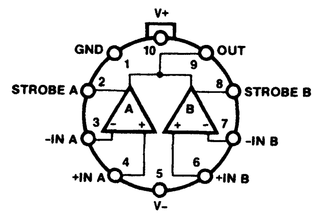
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA711M)	−55°C to +125°C
Commercial (μA711C)	0°C to 70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 V to +6.0 V

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW°C, the 14L-Ceramic DIP at 9.1 mW°C, and the 14L-Molded DIP at 8.3 mW°C.

Connection Diagram
10-Lead Metal Package
(Top View)



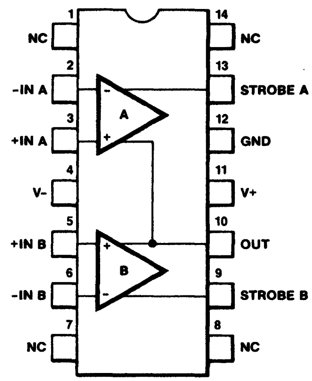
CD01050F

Lead 5 connected to case

Order Information

Device Code	Package Code	Package Description
μA711HM	5X	Metal
μA711HC	5X	Metal

Connection Diagram
14-Lead DIP
(Top View)

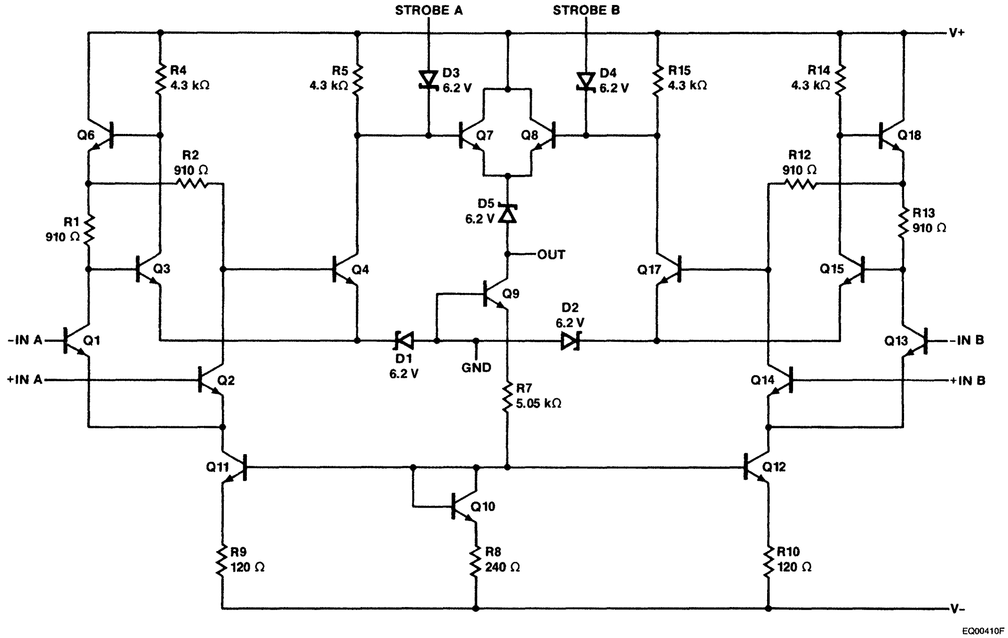


CD01061F

Order Information

Device Code	Package Code	Package Description
μA711DM	6A	Ceramic DIP
μA711DC	6A	Ceramic DIP
μA711PC	9A	Molded DIP

Equivalent Circuit



μA711
Electrical Characteristics T_A = 25°C, V+ = 12 V, V− = −6.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	V_O = 1.4 V, $R_S \leq$ 200 Ω, V_{CM} = 0 V		1.0	3.5	mV
		V_O = 1.4 V, $R_S \leq$ 200 Ω		1.0	5.0	
I_{IO}	Input Offset Current	V_O = 1.4 V		0.5	10.0	μA
I_{IB}	Input Bias Current			25	75	μA
A_{VS}	Large Signal Voltage Gain		750	1500		V/V
t_{PD}	Response Time[1]			40		ns
t_{STRL}	Strobe Release Time			12		ns
V_{IR}	Input Voltage Range	V− = −7.0 V	±5.0			V
V_{IDR}	Differential Input Voltage Range		±5.0			V
R_O	Output Resistance			200		Ω
V_{OH}	Output Voltage HIGH	$V_I \geq$ 10 mV		4.5	5.0	V
V_{OH}	Loaded Output Voltage HIGH	$V_I \geq$ 10 mV, I_{OH} = 5.0 mA	2.5	3.5		V
V_{OL}	Output Voltage LOW	$V_I \geq$ 10 mV	−1.0	−0.5	0	V
$V_{O(ST)}$	Strobed Output Level	$V_{ST} \leq$ 0.3 V	−1.0		0	V

μA711 (Cont.)

Electrical Characteristics $T_A = 25°C$, V+ = 12 V, V− = −6.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{OL}	Output Sink Current	$V_I \geqslant 10$ mV, $V_O \geqslant 0$ V	0.5	0.8		mA
$I_{O(ST)}$	Strobe Current	$V_{ST} = 100$ mV		1.2	2.5	mA
I+	Positive Supply Current	V_O = GND, Inverting Input = 5.0 mV		8.6		mA
I−	Negative Supply Current	V_O = GND, Inverting Input = 5.0 mV		3.9		mA
P_c	Power Consumption			130	200	mW
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$						
V_{IO}	Input Offset Voltage[2]	$R_S \leqslant 200\ \Omega$, $V_{CM} = 0$ V			4.5	mV
		$R_S \leqslant 200\ \Omega$			6.0	mV
I_{IO}	Input Offset Current				20	μA
I_{IB}	Input Bias Current				150	μA
$\Delta V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
A_{VS}	Large Signal Voltage Gain		500			V/V

μA711C

Electrical Characteristics $T_A = 25°C$, V+ = 12 V, V− = −6.0 V, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$V_O = +1.4$ V, $R_S \leqslant 200\ \Omega$, $V_{CM} = 0$ V		1.0	5.0	mV
		$V_O = +1.4$ V, $R_S \leqslant 200\ \Omega$		1.0	7.5	mV
I_{IO}	Input Offset Current	$V_O = +1.4$ V		0.5	15	μA
I_{IB}	Input Bias Current			25	100	μA
A_{VS}	Large Signal Voltage Gain		700	1500		V/V
t_{PD}	Response Time[1]			40		ns
t_{STRL}	Strobe Release Time			12		ns
V_{IR}	Input Voltage Range	V− = −7.0 V	±5.0			V
V_{IDR}	Differential Input Voltage Range		±5.0			V
R_O	Output Resistance			200		Ω
V_{OH}	Output Voltage HIGH	$V_I \geqslant 10$ mV		4.5	5.0	V
V_{OH}	Loaded Output Voltage HIGH	$V_I \geqslant 10$ mV, $I_{OH} = 5.0$ mA	2.5	3.5		V
V_{OL}	Output Voltage LOW	$V_I \geqslant 10$ mV	−1.0	−0.5	0	V
$V_{O(ST)}$	Strobed Output Level	$V_{ST} \leqslant 0.3$ V	−1.0		0	V
I_{OL}	Output Sink Current	$V_I \geqslant 10$ mV, $V_O \geqslant$ GND	0.5	0.8		mA
$I_{O(ST)}$	Strobe Current	$V_{ST} = 100$ mV		1.2	2.5	mA
I+	Positive Supply Current	V_O = GND, Inverting Input = 10 mV		8.6		mA

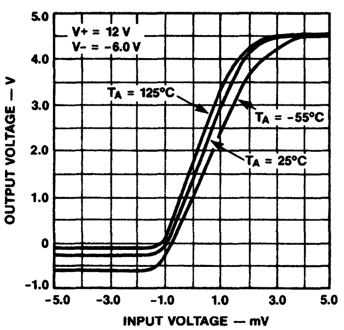
μA711C (Cont.)
Electrical Characteristics $T_A = 25°C$, V+ = 12 V, V− = −6.0 V, unless otherwise specified.

Symbol	Characteristic	Condition[1]	Min	Typ	Max	Unit
I−	Negative Supply Current	V_O = GND, Inverting Input = 10 mV		3.9		mA
P_c	Power Consumption			130	230	mW
The following specifications apply for $0°C \leq T_A \leq 70°C$						
V_{IO}	Input Offset Voltage[2]	$R_S \leq 200\ \Omega$, $V_{CM} = 0$ V			6.0	mV
		$R_S \leq 200\ \Omega$			10	mV
I_{IO}	Input Offset Current				25	μA
I_{IB}	Input Bias Current				150	μA
$\Delta V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
A_{VS}	Large Signal Voltage Gain		500			V/V

Notes
1. The response time specified is for a 100 mV step input with 5.0 mV overdrive.
2. The input offset voltage is specified for a logic threshold as follows:
μA711: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C
μA711C: 1.5 V at 0°C, 1.4 V at 25°C, 1.2 V at 70°C

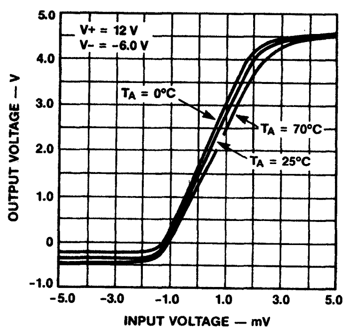
Typical Performance Curves

Voltage Transfer Characteristic μA711



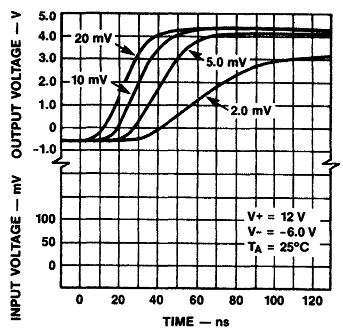
PC07200F

Voltage Transfer Characteristic μA711C



PC07210F

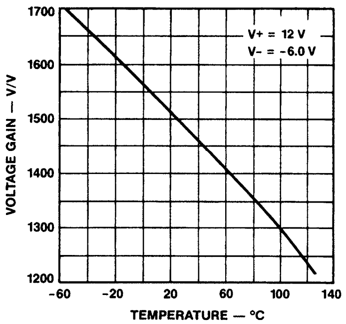
Response Time for Various Input Overdrives



PC07220F

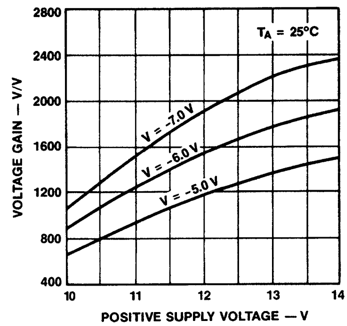
Typical Performance Curves (Cont.)

Voltage Gain vs Temperature



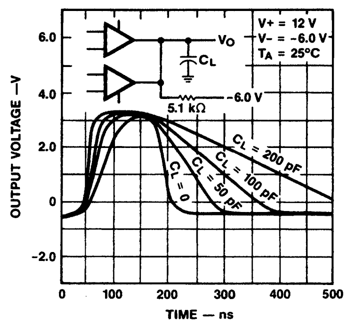
P07230F

Voltage Gain vs Supply Voltages



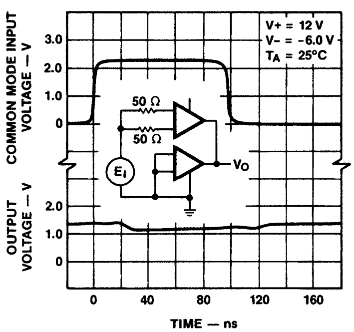
PC07240F

Output Pulse Stretching With Capacitive Loading



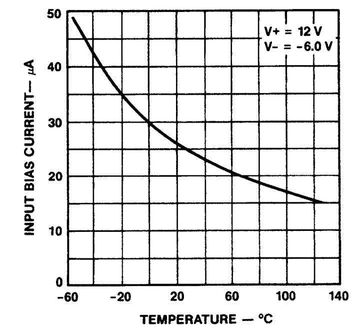
PC07250F

Common Mode Pulse Response



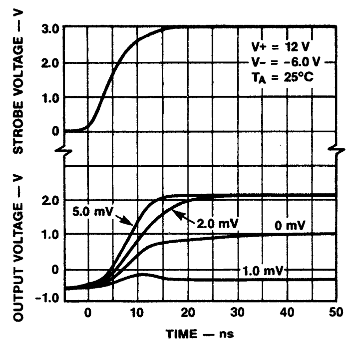
PC07260F

Input Bias Current vs Temperature



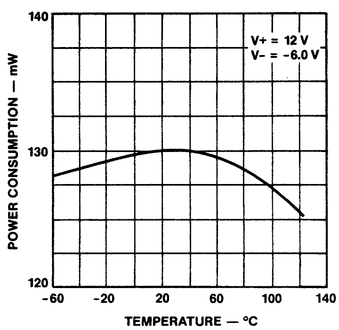
PC07270F

Strobe Release Time for Various Input Overdrives



PC07280F

Power Consumption vs Temperature



PC07290F

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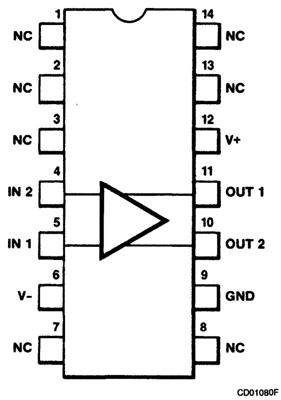
μA760 High Speed Differential Comparator

Description

The μA760 is a differential voltage comparator offering considerable speed improvement over the μA710 family and operates from symmetric supplies of ±4.5 V to ±6.5 V. The μA760 can be used in high speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

- **Guaranteed High Speed — 25 ns Max**
- **Guaranteed Delay Matching On Both Outputs**
- **Complementary TTL Compatible Outputs**
- **High Sensitivity**
- **Standard Supply Voltages**

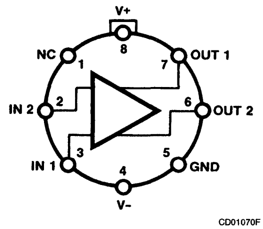
Connection Diagram 14-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA760DM	6A	Ceramic DIP
μA760DC	6A	Ceramic DIP

Connection Diagram 8-Lead Metal Package (Top View)

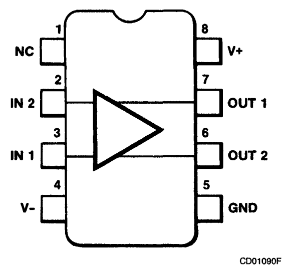


Lead 4 connected to case

Order Information

Device Code	Package Code	Package Description
μA760HM	5W	Metal
μA760HC	5W	Metal

Connection Diagram 8-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA760RM	6T	Ceramic DIP
μA760RC	6T	Ceramic DIP

Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA760M)	-55°C to +125°C
Commercial (μA760C)	0°C to 70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C

Internal Power Dissipation[1, 2]	
8L-Metal Can	1.00 W
14L-Ceramic DIP	1.36 W
8L-Ceramic DIP	1.30 W
Positive Supply Voltage	+8.0 V
Negative Supply Voltage	-8.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	$V+ \geqslant V_I \geqslant V-$

Notes

1. $T_{J\ Max} = 175°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, and the 8L-Ceramic DIP at 8.7 mW/°C.

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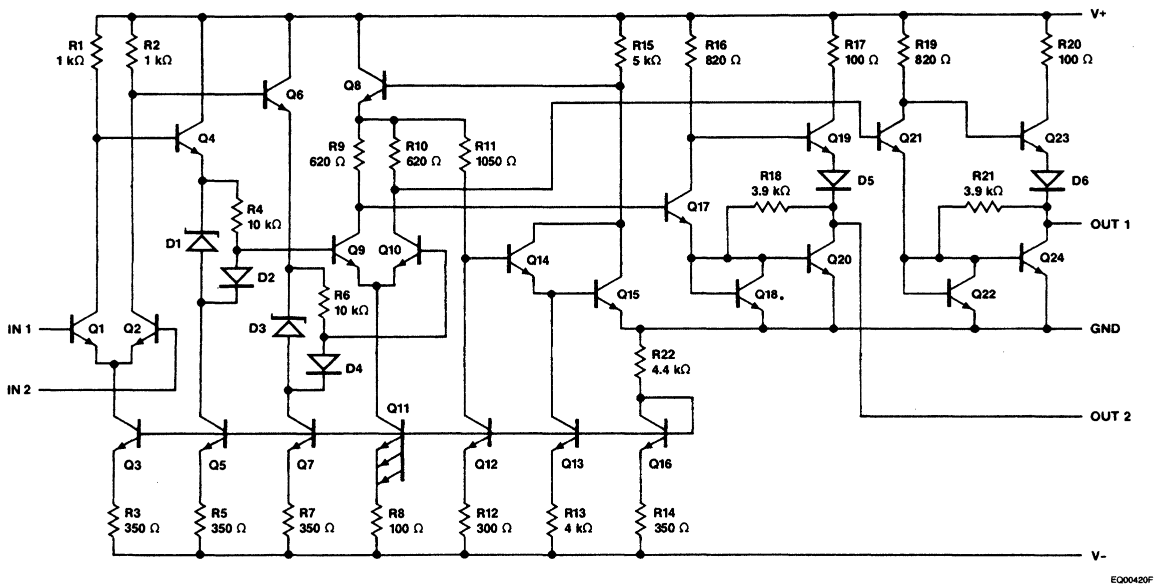
Equivalent Circuit



μA760

Electrical Characteristics $V_{CC} = \pm 4.5$ V to ± 6.5 V, $T_A = -55°C$ to $+125°C$, $T_A = 25°C$ for typical figures, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leqslant 200\ \Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (either output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	$T_A = 25°C$[1]		18	30	ns
		$T_A = 25°C$[2]			25	
		(Note 3)		16		
Δt_{PD}	Response Time Difference between Outputs[1] (t_{PD} of $+V_{I1}$) − (t_{PD} of $-V_{I2}$)	$T_A = 25°C$			5.0	ns
	(t_{PD} of $+V_{I2}$) − (t_{PD} of $-V_{I1}$)	$T_A = 25°C$			5.0	
	(t_{PD} of $+V_{I1}$) − (t_{PD} of $+V_{I2}$)	$T_A = 25°C$			7.5	
	(t_{PD} of $-V_{I1}$) − (t_{PD} of $-V_{I2}$)	$T_A = 25°C$			7.5	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = -55°C$ to $+125°C$		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $125°C$		2.0		nA/°C
		$T_A = +25°C$ to $-55°C$		7.0		
V_{IR}	Input Voltage Range	$V_{CC} = \pm 6.5$ V	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (either output)	0 mA $\leqslant I_{OH} \leqslant$ 5.0 mA $V_{CC} = +5.0$ V	2.4	3.2		V
		$I_{OH} = 80$ μA, $V_{CC} = \pm 4.5$ V	2.4	3.0		
V_{OL}	Output Voltage LOW (either output)	$I_{OL} = 3.2$ mA		0.25	0.4	V
I+	Positive Supply Current	$V_{CC} = \pm 6.5$ V		18	32	mA
I−	Negative Supply Current	$V_{CC} = \pm 6.5$ V		9.0	16	mA

Notes

1. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
2. Response time measured from the 50% point of a 2.0 V p-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the start of a 100 mV input step with 5.0 mV overdrive to the time when the output crosses the logic threshold.

μA760C

Electrical Characteristics V_{CC} = ±4.5 V to ±6.5 V, T_A = 0°C to 70°C, T_A = 25°C for typical figures, unless otherwise specified.

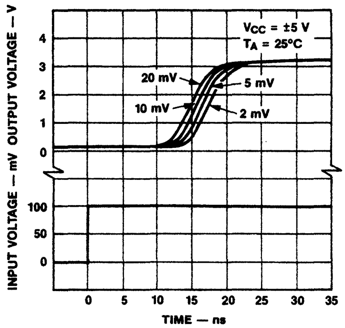
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (either output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	T_A = 25°C[1]		18	30	ns
		T_A = 25°C[2]			25	
		(Note 3)		16		
Δt_{PD}	Response Time Difference between Outputs[1]					ns
	(t_{PD} of $+V_{I1}$) – (t_{PD} of $-V_{I2}$)	T_A = 25°C			5.0	
	(t_{PD} of $+V_{I2}$) – (t_{PD} of $-V_{I1}$)	T_A = 25°C			5.0	
	(t_{PD} of $+V_{I1}$) – (t_{PD} of $+V_{I2}$)	T_A = 25°C			10	
	(t_{PD} of $-V_{I1}$) – (t_{PD} of $-V_{I2}$)	T_A = 25°C			10	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω, T_A = 0°C to 70°C		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	T_A = 25°C to 70°C		5.0		nA/°C
		T_A = 25°C to 0°C		10		
V_{IR}	Input Voltage Range	V_{CC} = ±6.5 V	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (either output)	0 mA ≤ I_{OH} ≤ 5.0 mA V_{CC} = +5.0 V	2.4	3.2		V
		I_{OH} = 80 μA, V_{CC} = ±4.5 V	2.5	3.0		
V_{OL}	Output Voltage LOW (either output)	I_{OL} = 3.2 mA		0.25	0.4	V
I+	Positive Supply Current	V_{CC} = ±6.5 V		18	34	mA
I–	Negative Supply Current	V_{CC} = ±6.5 V		9.0	16	mA

Notes
1. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
2. Response time measured from the 50% point of a 2.0 V p-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the start of a 100 mV input step with 5.0 mV overdrive to the time when the output crosses the logic threshold.

8

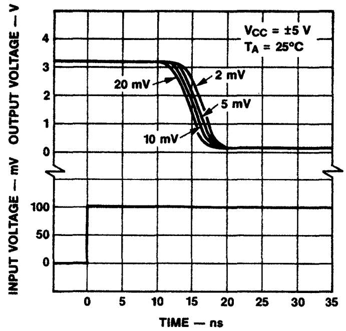
Typical Performance Curves

Response Time for Various Input Overdrives



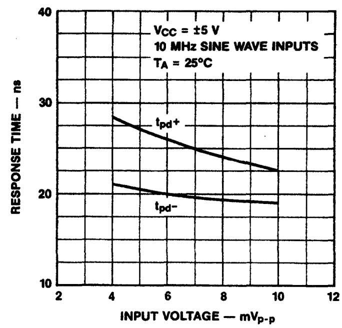
PC07300F

Response Time for Various Input Overdrives



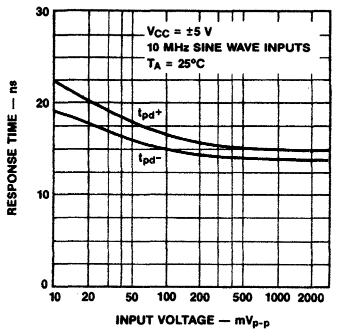
PC07310F

Response Time vs Input Voltage



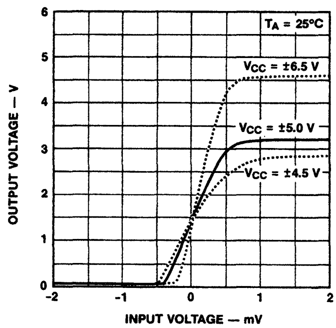
PC07320F

Response Time vs Input Voltage



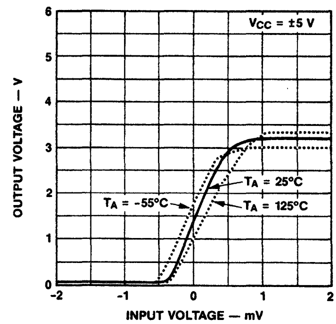
PC07330F

Voltage Transfer Characteristic



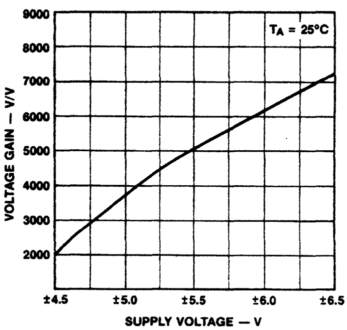
PC07340F

Voltage Transfer Characteristic



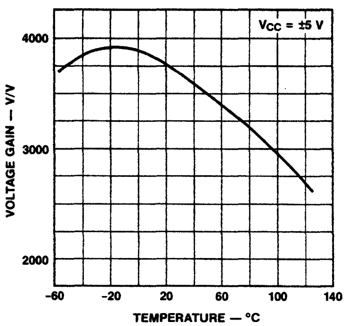
PC07350F

Voltage Gain vs Supply Voltage



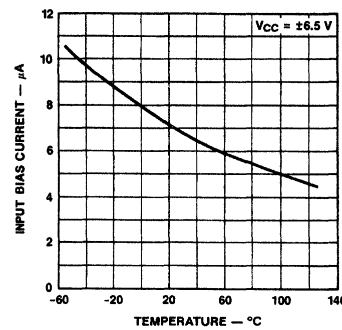
PC07361F

Voltage Gain vs Temperature



PC07370F

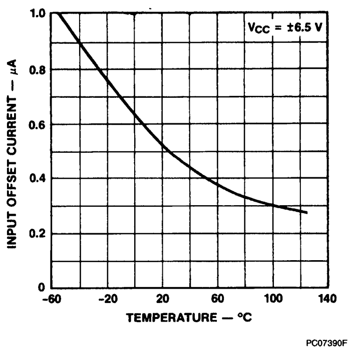
Input Bias Current vs Temperature



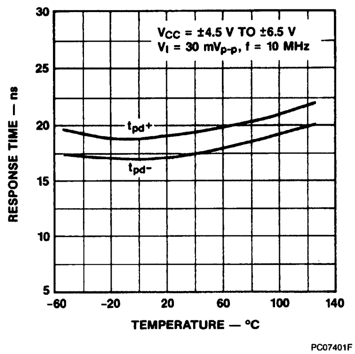
PC07380F

Typical Performance Curves (Cont.)

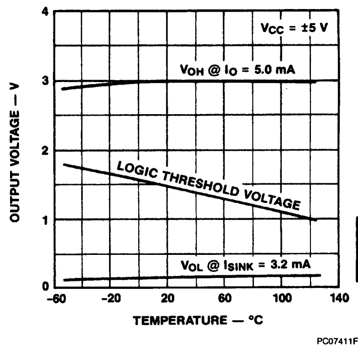
Input Offset Current vs Temperature



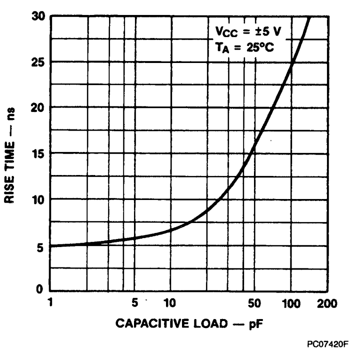
Response Time vs Temperature



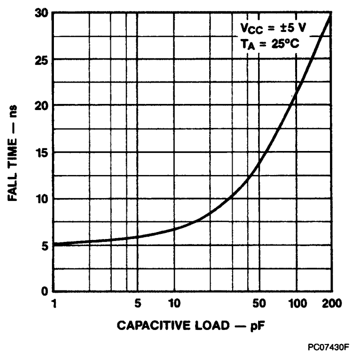
Output Voltage Levels vs Temperature



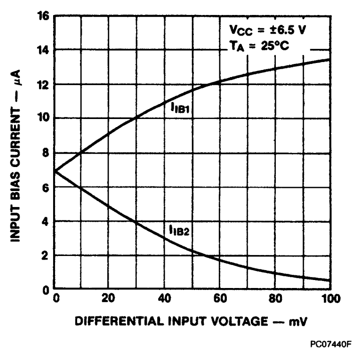
Rise Time vs Capacitive Load



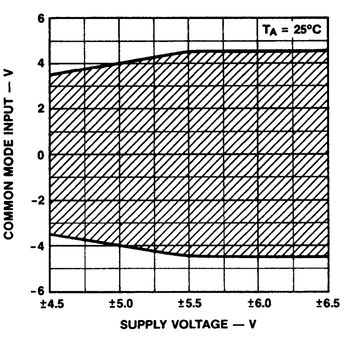
Fall Time vs Capacitive Load



Input Bias Current vs Differential Input Voltage

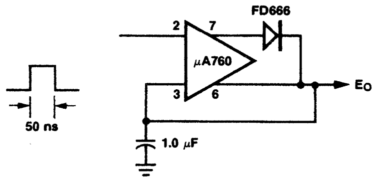


Common Mode Range vs Supply Voltage



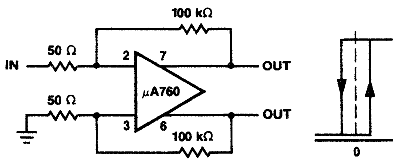
Typical Applications (Note 1)

Fast Positive Peak Detector



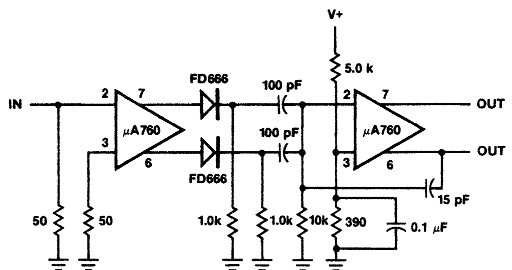
CR02420F

Level Detector with Hysteresis



CR02440F

Zero Crossing Detector (Note 2)

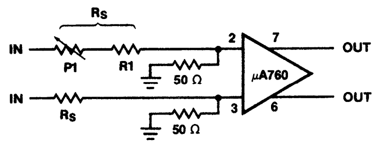


Total delay = 30 ns
Input frequency = 300 Hz to 3.0 MHz
Minimum input voltage = 20 mV_{p-p}

CR02450F

Notes
1. Lead numbers shown are for Metal Package only.
2. All resistor values in ohms.

Line Receiver With High Common Mode Range



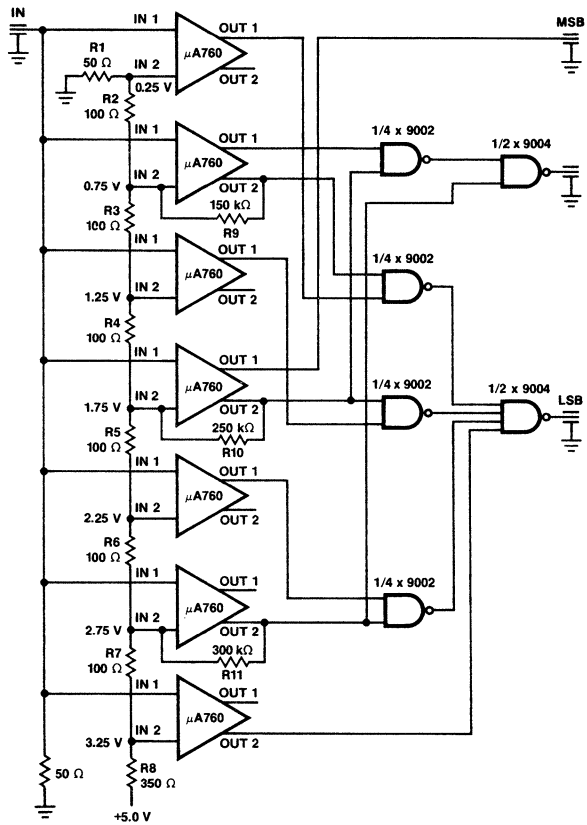
Common mode range = $\pm 4 \times \frac{RS}{50}$ V

Differential input sensitivity = $5 \times \frac{RS}{50}$ mV

P_1 must be adjusted for optimum common mode rejection.
For R_S = 200 Ω
Common mode range = ±16 V
Sensitivity = 20 mV

CR02430F

High Speed 3-Bit A/D Converter



Input voltage range = 3.5 V
Typical conversion speed = 30 ns

CR02460F

FAIRCHILD

A Schlumberger Company

μA1488
RS-232C
Quad Line Driver

Linear Division Interface Products

Description

The μA1488 is an EIA RS-232C specified quad line driver. This device is used to interface data terminals with data communications equipment. The μA1488 is a lead-for-lead replacement of the MC1488.

- **Current Limited Output — ± 10 mA Typical**
- **Power-Off Source Impedance 300 Ω Minimum**
- **Simple Slew Rate Control With External Capacitor**
- **Flexible Operating Supply Range**

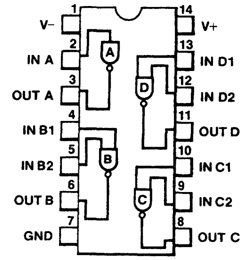
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	±15 V
Input Voltage Range	−15 V to +7.0 V
Output Signal Voltage	±15 V

Note

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



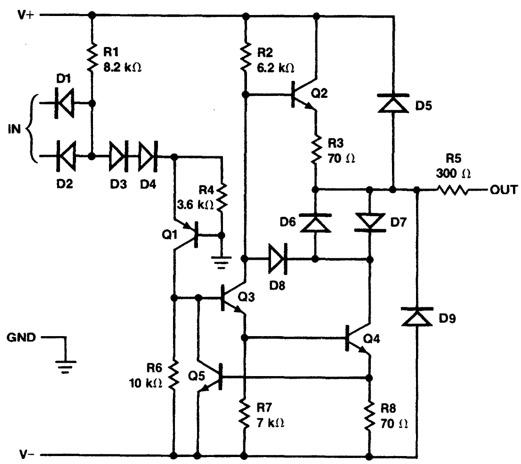
CD00331F

Order Information

Device Code	Package Code	Package Description
μA1488DC	6A	Ceramic DIP
μA1488PC	9A	Molded DIP
μA1488SC	KD	Molded Surface Mount

9

Equivalent Circuit (1/4 of Circuit)



BD00201F

μA1488
Electrical Characteristics

DC Characteristics $V_{CC} = \pm 9.0$ V $\pm 1\%$, $T_A = 0°C$ to 70°C, unless otherwise specified.

Symbol	Characteristic	Condition	Figure	Min	Typ	Max	Unit
I_{IL}	Input Current LOW	$V_{IL} = 0$ V	1		1.0	1.6	mA
I_{IH}	Input Current HIGH	$V_{IH} = 5.0$ V	1			10	μA
V_{OH}	Output Voltage HIGH	$V_{IL} = 0.8$ V, $R_L = 3.0$ kΩ $V_{CC} = \pm 9.0$ V	2	6.0	7.0		V
		$V_{IL} = 0.8$ V, $R_L = 3.0$ kΩ $V_{CC} = \pm 13.2$ V		9.0	10.5		
V_{OL}	Output Voltage LOW	$V_{IH} = 1.9$ V, $R_L = 3.0$ kΩ $V_{CC} = \pm 9.0$ V	2	-6.0	-7.0		V
		$V_{IH} = 1.9$ V, $R_L = 3.0$ kΩ $V_{CC} = \pm 13.2$ V		-9.0	-10.5		
I_{OS+}	Positive Output Short Circuit Current[1]	$V_{IL} = 0.8$ V	3	-6.0	-10	-12	mA
I_{OS-}	Negative Output Short Circuit Current[1]	$V_{IH} = 1.9$ V	3	+6.0	+10	+12	mA
R_O	Output Resistance	$V_{CC} = 0$ V, $V_O = \pm 2.0$ V	4	300			Ω
I+	Positive Supply Current	$R_L = \infty$ $V_{IH} = 1.9$ V, V+ = 9.0 V	5		15	20	mA
		$V_{IL} = 0.8$ V, V+ = 9.0 V			4.5	6.0	
		$V_{IH} = 1.9$ V, V+ = 12 V			19	25	
		$V_{IL} = 0.8$ V, V+ = 12 V			5.5	7.0	
		$V_{IH} = 1.9$ V, V+ = 15 V				34	
		$V_{IL} = 0.8$ V, V+ = 15 V				12	
I−	Negative Supply Current	$R_L = \infty$ $V_{IH} = 1.9$ V, V− = −9.0 V	5		-13	-17	mA
		$V_{IL} = 0.8$ V, V− = −9.0 V				-15	μA
		$V_{IH} = 1.9$ V, V− = −12 V			-18	-23	mA
		$V_{IL} = 0.8$ V, V− = −12 V				-15	μA
		$V_{IH} = 1.9$ V, V− = −15 V				-34	mA
		$V_{IL} = 0.8$ V, V− = −15 V				-2.5	mA
P_C	Power Consumption	$V_{CC} = \pm 9.0$ V				333	mW
		$V_{CC} = \pm 12$ V				576	

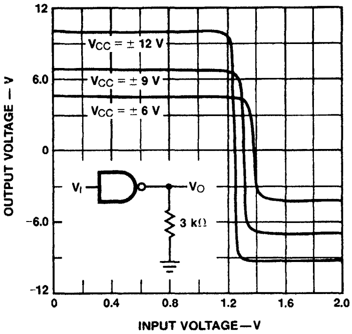
AC Characteristics $V_{CC} = \pm 9.0$ V $\pm 1\%$, $T_A = 25°C$

Symbol	Characteristic	Condition	Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time	$R_L = 3.0$ kΩ, $C_L = 15$ pF	6		220	350	ns
t_{PHL}					70	175	ns
t_f	Fall Time	$R_L = 3.0$ kΩ, $C_L = 15$ pF	6		70	75	ns
t_r	Rise Time				55	100	ns

Note
1. Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously.

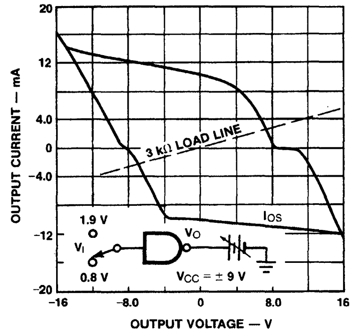
Typical Performance Curves

Transfer Characteristics vs Supply Voltage



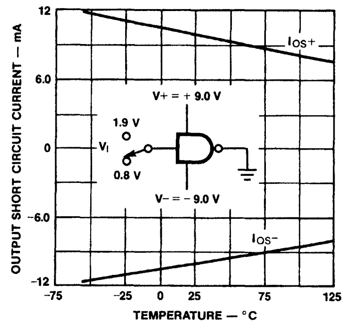
PC02342F

Output Voltage and Current Limiting Characteristics



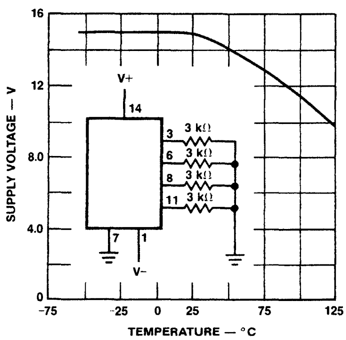
PC02352F

Short Circuit Output Current vs Temperature



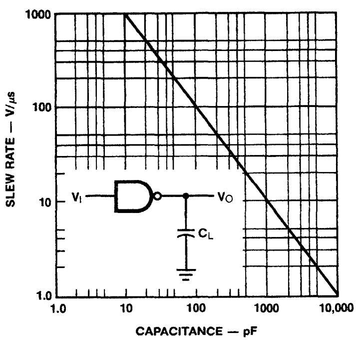
PC02362F

Supply Voltage vs Maximum Operating Temperature



PC02372F

Output Slew Rate vs Load Capacitance



PC02382F

DC Test Circuits

Figure 1 Input Current

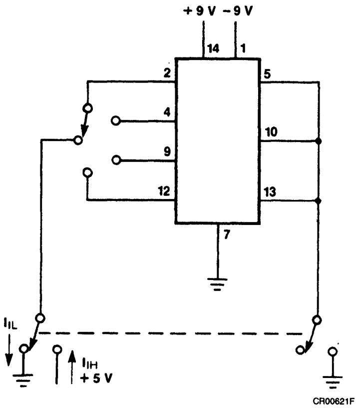


Figure 2 Output Voltage

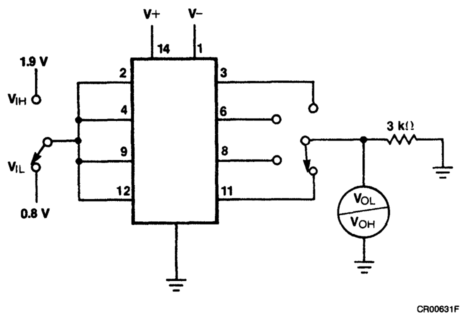


Figure 3 Output Short Circuit Current

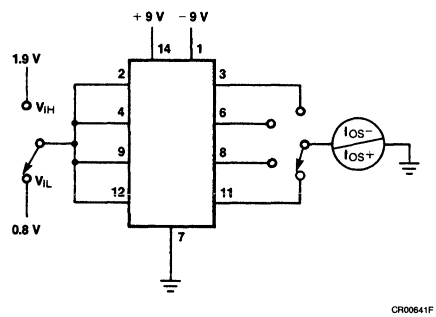


Figure 4 Output Resistance (Power-off)

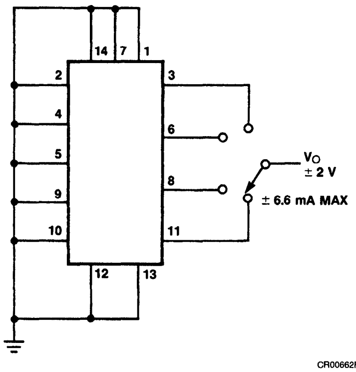


Figure 5 Supply Currents

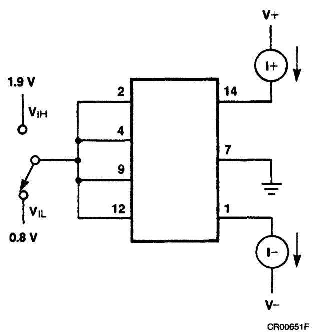
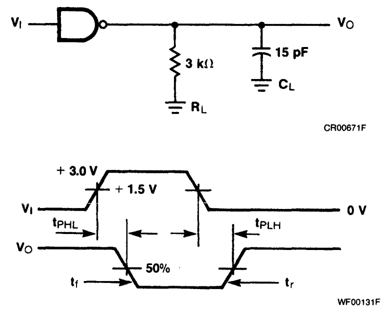


Figure 6 AC Test Circuit and Voltage Waveforms



t_r and t_f are measured 10% to 90%

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μA1489 • μA1489A RS-232C Quad Line Receivers

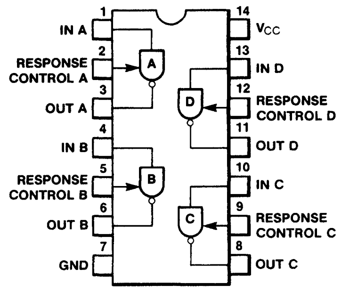
Linear Division Interface Products

Description

The μA1489 and the μA1489A are EIA RS-232C specified quad line receivers. These devices are used to interface data terminals with data communications equipment. The μA1489 and μA1489A are lead-for-lead replacements of the MC1489 and MC1489A respectively.

- **Input Resistance 3.0 kΩ To 7.0 kΩ**
- **Input Signal Range ±30 V**
- **Input Threshold Hysteresis Built-In**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**

Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	10 V
Input Voltage Range	±30 V
Output Load Current	20 mA

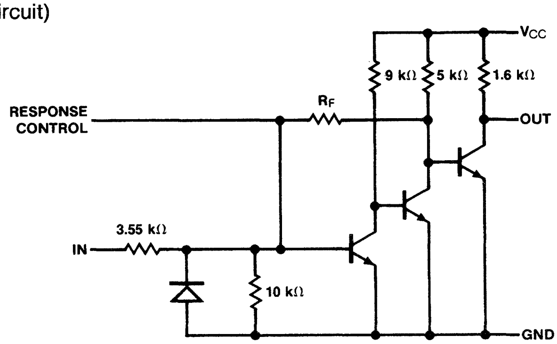
Note

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Order Information

Device Code	Package Code	Package Description
μA1489DC	6A	Ceramic DIP
μA1489PC	9A	Molded DIP
μA1489SC	KD	Molded Surface Mount
μA1489ADC	6A	Ceramic DIP
μA1489APC	9A	Molded DIP

Equivalent Circuit (1/4 of circuit)



	μA1489	μA1489A
R_F	10 kΩ	2 kΩ

EQ00210F

9

μA1489, μA1489A
Electrical Characteristics

DC Characteristics V_{CC} = 5.0 V ± 1.0%, response control lead is open, T_A = 0°C to 70°C, unless otherwise specified.

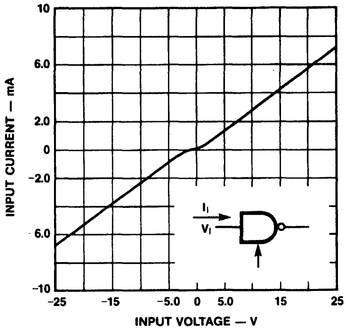
Symbol	Characteristic	Condition		Figure	Min	Typ	Max	Unit
I_{IH}	Input Current HIGH	V_{IH} = 25 V		1	3.6		8.3	mA
		V_{IH} = 3.0 V			0.43			
I_{IL}	Input Current LOW	V_{IL} = −25 V		1	−3.6		−8.3	mA
		V_{IL} = −3.0 V			−0.43			
V_{TH+}	Input Turn-on Threshold Voltage	T_A = 25°C, $V_{OL} \leqslant$ 0.45 V	μA1489	2	1.0		1.5	V
			μA1489A		1.75	1.95	2.25	
V_{TH-}	Input Turn-off Threshold Voltage	T_A = 25°C, $V_{OH} \geqslant$ 2.5 V, I_{OH} = −0.5 mA	μA1489	2	0.75		1.25	V
			μA1489A		0.75	0.8	1.25	
V_{OH}	Output Voltage HIGH	V_{IH} = 0.75 V, I_{OH} = −0.5 mA		2	2.6	4.0	5.0	V
		Input Open Circuit, I_{OH} = −0.5 mA						
V_{OL}	Output Voltage LOW	V_{IL} = 3.0 V, I_{OL} = 10 mA		2		0.2	0.45	V
I_{OS}	Output Short Circuit Current			3		3.0		mA
I_{CC}	Supply Current	V_{IH} = 5.0 V		4		20	26	mA
P_C	Power Consumption	V_{IH} = 5.0 V		4		100	130	mW

AC Characteristics V_{CC} = 5.0 V ± 1.0%, T_A = 25°C

Symbol	Characteristic	Condition	Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time	R_L = 3.9 kΩ	5		25	85	ns
t_{PHL}		R_L = 390 Ω			25	50	ns
t_r	Rise Time	R_L = 3.9 kΩ	5		120	175	ns
t_f	Fall Time	R_L = 390 Ω			10	20	ns

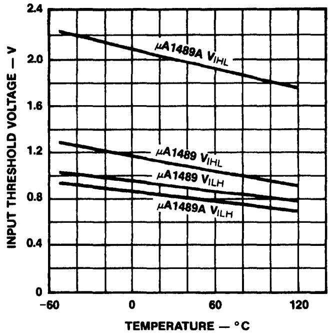
Typical Performance Curves

Input Current vs Input Voltage



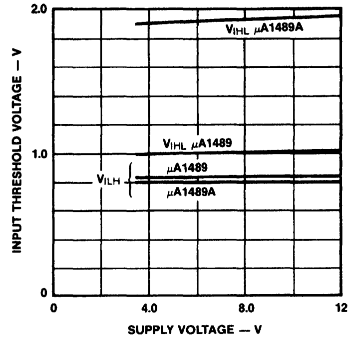
PC06021F

Input Threshold Voltage vs Temperature



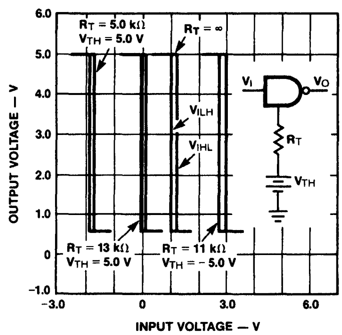
PC06031F

Input Threshold Voltage vs Supply Voltage



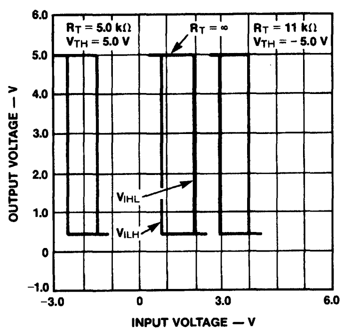
PC06041F

µA1489 Input Threshold Voltage Adjustment



PC06051F

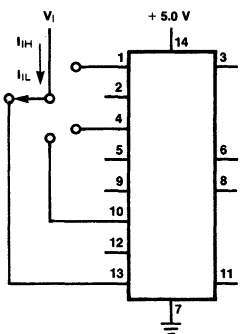
µA1489A Input Threshold Voltage Adjustment



PC06061F

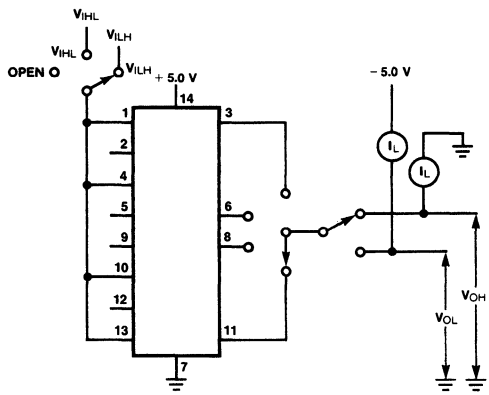
Test Circuits

Figure 1 Input Current



CR01580F

Figure 2 Output Voltage and Input Threshold Voltage



CR01600F

Test Circuits (Cont.)

Figure 3 Output Short Circuit Current

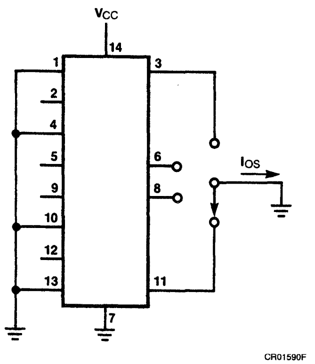


Figure 4 Supply Current

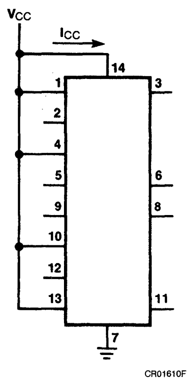


Figure 5 AC Test Circuit and Voltage Waveforms

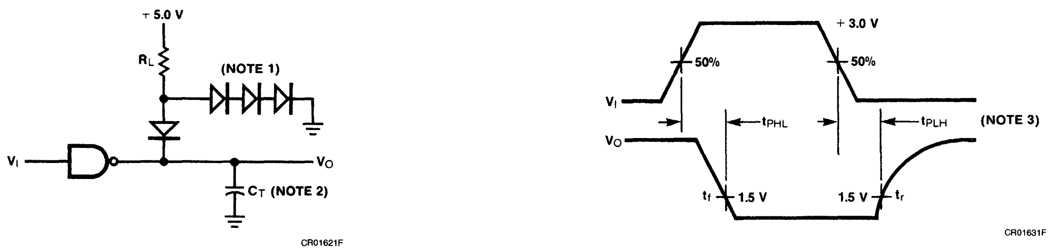
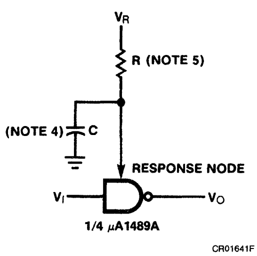


Figure 6 Response Control Node



Notes

1. All diodes FD600 or equivalent.
2. C_T = 15 pF = total parasitic capacitance, which includes probe and jig capacitance.
3. t_r and t_f measured 10% to 90%.
4. Capacitor is for noise filtering.
5. Resistor is for threshold shifting.

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μA26LS31
Quad High Speed Differential Line Driver

Linear Division Interface Products

Description

The μA26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The μA26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The μA26LS31 features three-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The μA26LS31 offers optimum performance when used with the μA26LS32 Quad Differential Line Receiver.

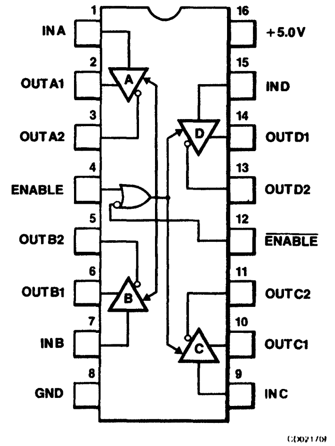
- **Output Skew - 2.0 ns Typical**
- **Input To Output Delay - 12 ns**
- **Operation From Single +5.0 V Supply**
- **16-Lead Ceramic And Molded DIP Package**
- **Outputs Won't Load Line When V_{CC} = 0 V**
- **Four Line Drivers In One Package For Maximum Package Density**
- **Output Short Circuit Protection**
- **Complementary Outputs**
- **Meets The Requirements Of EIA Standard RS-422**
- **High Output Drive Capability For 100 Ω Terminated Transmission Lines**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Input Voltage	7.0 V
Output Voltage	5.5 V

Notes
1. $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperatures at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminals.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

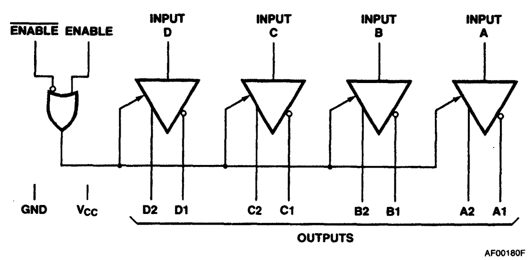
Device Code	Package Code	Package Description
μA26LS31DC	7B	Ceramic DIP
μA26LS31PC	9B	Molded DIP

Function Table (Each Driver)

Input	Enable	Outputs Y	Outputs Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Logic Symbol

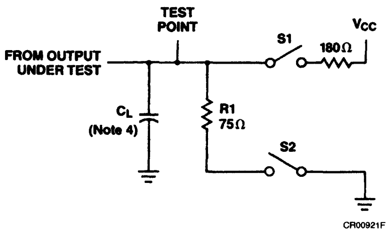


μA26LS31
Electrical Characteristics 0°C ⩽ T_A ⩽ 70°C, 4.75 V ⩽ V_{CC} ⩽ 5.25 V, unless otherwise specificied.

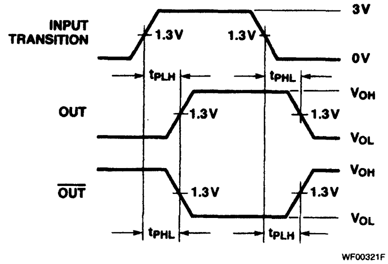
Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = −20 mA		2.5	3.2		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = 20 mA			0.32	0.5	V
V_{IH}	Input Voltage HIGH	V_{CC} = Min		2.0			V
V_{IL}	Input Voltage LOW	V_{CC} = Max				0.8	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V			−0.20	−0.36	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7 V			0.5	20	μA
I_{IR}	Input Reverse Current	V_{CC} = Max, V_I = 7.0 V			0.001	0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.5 V		0.5	20	μA
			V_O = 0.5 V		0.5	−20	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
I_{OS}	Output Short Circuit	V_{CC} = Max		−30	−60	−150	mA
I_{CC}	Supply Current	V_{CC} = Max, All Outputs Disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, C_L = 10 pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, C_L = 10 pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0 V, T_A = 25°C, Load = Note 2			30	40	ns

Notes
1. All typical values are V_{CC} = 5.0 V, T_A = 25°C
2. C_L = 30 pF, V_I = 1.3 V to V_O = 1.3 V, V_{PULSE} = 0 V to +3.0 V (See AC Load Test Circuit for Three-State Outputs)

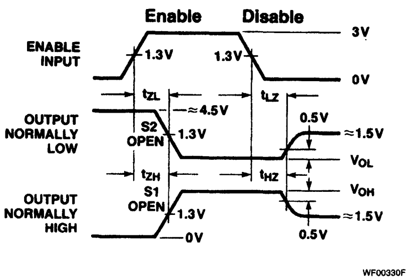
AC Load Test Circuit for Three-State Outputs



Propagation Delay (Notes 1 and 3)



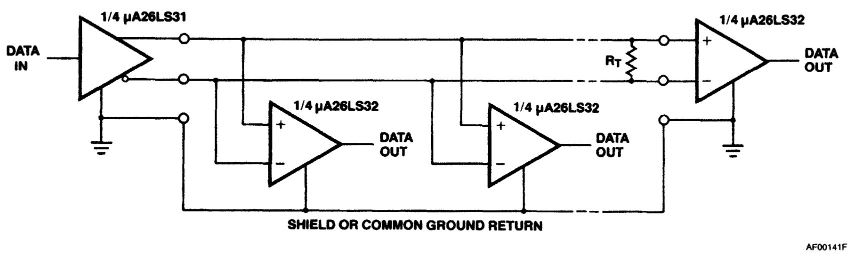
Enable and Disable Times (Notes 2 and 3)



Notes

1. Diagram shown for Enable Low. Switches S1 and S2 open.
2. S1 and S2 of Load Circuit are closed except where shown.
3. Pulse Generator for all Pulses: Rate ⩽1.0 MHz, $Z_O = 50\ \Omega$, t_r ⩽6.0 ns, t_f ⩽6.0 ns.
4. C_L includes probe and jig capacitance.

Typical Application



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μA26LS32 Quad Differential Line Receiver

Linear Division Interface Products

Description

The μA26LS32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The device features an input sensitivity of 200 mV over the input range of ±7.0 V. The μA26LS32 provides an enable function common to all four receivers and three-state outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

The μA26LS32 offers optimum performance when used with the μA26LS31 Quad Differential Line Driver.

- **Input Voltage Range Of ±7.0 V (Differential Or Common Mode) ±0.2 V Sensitivity Over The Input Voltage Range**
- **Meets All The Requirements Of EIA Standards RS-422 And RS-423**
- **Input Impedance (15K Typical)**
- **30 mV Input Hysteresis**
- **Operation From Single +5.0 V Supply**
- **Fail-Safe Input/Output Relationship. Output Always High When Inputs Are Open.**
- **Three-State Drive, With Choice Of Complementary Output Enables, For Receiving Directly Onto A Data Bus.**
- **Propagation Delay 17 ns Typical**
- **Advanced Low Power Schottky processing**
- **100% Reliability Assurance Screening To MIL-STD-883 Requirements.**

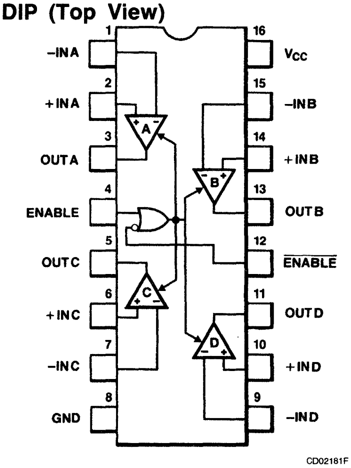
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Common Mode Voltage Range	±25 V
Differential Input Voltage	±25 V
Enable Voltage	7.0 V
Output Sink Current	50 mA

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Connection Diagram
16-Lead DIP (Top View)



Order Information

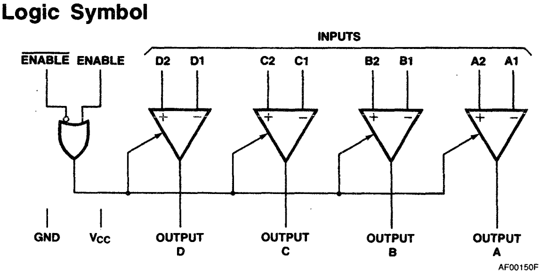
Device Code	Package Code	Package Description
μA26LS32DC	7B	Ceramic DIP
μA26LS32PC	9B	Molded DIP

Function Table (Each Receiver)

Differential Inputs	Enables		Outputs
A − B	E	$\overline{E}$	V
$V_{ID} \geqslant 0.2$ V	H	X	H
	X	L	H
$-0.2\ V < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leqslant -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
X = High Impedance (off)

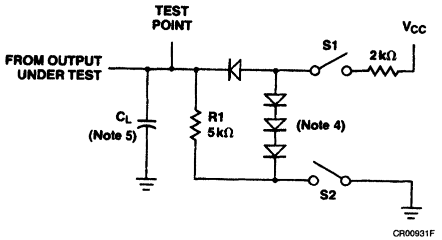
Logic Symbol



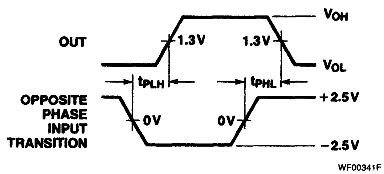
μ**A26LS32**
Electrical Characteristics 0°C $\leqslant T_A \leqslant$ 70°C, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V, unless otherwise specified.

Symbol	Characteristic	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$-7.0\ V \leqslant V_{CM} \leqslant +7.0\ V$, $V_O = V_{OL}$ or V_{OH}		−0.2	±0.06	+0.2	V
R_I	Input Resistance	$-15\ V \leqslant V_{CM} \leqslant +15\ V$, One Input AC Ground		6.0	15		kΩ
I_I	Input Current (Under Test)	$V_I = +15$ V, Other Input $-15\ V \leqslant V_I \leqslant +15\ V$				2.3	mA
I_I	Input Current (Under Test)	$V_I = -15$ V, Other Input $-15\ V \leqslant V_I \leqslant +15\ V$				−2.8	mA
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $\Delta V_I = +1.0$ V, $V_{\overline{ENABLE}} = 0.8$ V, $I_{OH} = -440\ \mu A$		2.7	3.4		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, $\Delta V_I = -1.0$ V, $V_{\overline{ENABLE}} = 0.8$ V	$I_{OL} = 4.0$ mA			0.4	V
			$I_{OL} = 8.0$ mA			0.45	
V_{IL}	Enable Voltage LOW					0.8	V
V_{IH}	Enable Voltage HIGH					2.0	
V_{IC}	Enable Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4$ V			20	μA
			$V_O = 0.4$ V			−20	
I_{IL}	Enable Current LOW	$V_I = 0.4$ V			−0.2	−0.36	mA
I_{IH}	Enable Current HIGH	$V_I = 2.7$ V			0.5	20	μA
I_I	Enable Input High Current	$V_I = 5.5$ V			1.0	100	μA
I_{OS}	Output Short Circuit Current	$V_O = 0$ V, V_{CC} = Max, $\Delta V_I = +1.0$ V		−15	−50	−85	mA
I_{CC}	Supply Current	V_{CC} = Max, All V_I = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5.0$ V, $V_{CM} = 0$ V			30		mV
t_{PLH}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			17	25	ns
t_{PHL}	Input to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			17	25	ns
t_{LZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			20	30	ns
t_{HZ}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			15	22	ns
t_{ZL}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			15	22	ns
t_{ZH}	Enable to Output	$T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF, see test circuit			15	22	ns

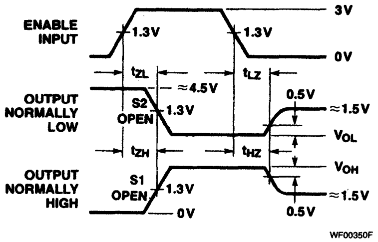
Load Test Circuit for Three-State Outputs



Propagation Delay (Notes 1 and 3)



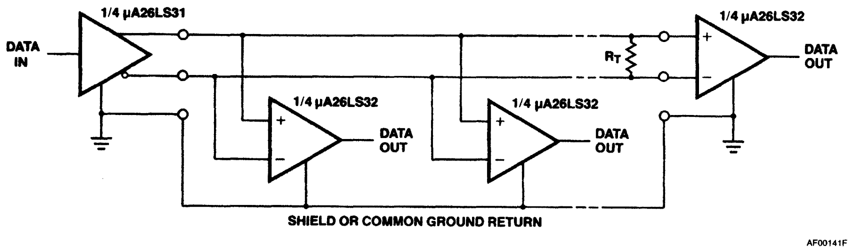
Enable and Disable Times (Notes 2 and 3)



Notes

1. Diagram shown for $\overline{\text{Enable}}$ Low.
2. S1 and S2 of Load Circuit are closed except where shown.
3. Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\ \Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.
4. All diodes are IN916 or IN3064.
5. C_L includes probe and jig capacitance.

Typical Application



FAIRCHILD

A Schlumberger Company

μA3486
RS-422/3 Quad Line Receiver With Three-State Outputs

Linear Division Interface Products

Description

Fairchild's RS-422/3 Quad Receiver features four independent receiver chains which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible three-state structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. A PNP device buffers each output control lead to assure minimum loading for either logic one or logic zero inputs. In addition each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

- **Four Independent Receiver Chains**
- **Three-State Outputs**
- **High Impedance Output Control Inputs**
- **Internal Hysteresis - 50 mV Typical**
- **Fast Propagation Times 16 ns Typical**
- **TTL Compatible**
- **Single 5.0 V Supply Voltage**
- **Output Rise And Fall Times Less Than 20 ns**
- **Lead Compatible And Interchangeable With MC3486 And DS3486**

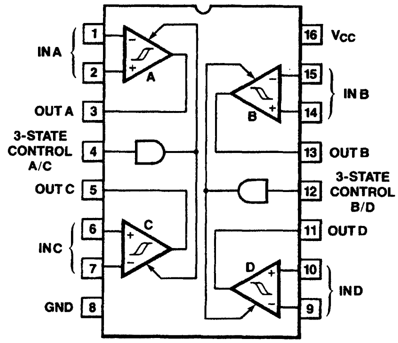
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	8.0 V
Input Voltage	8.0 V
Input Common Mode Voltage	±15 V
Input Differential Voltage	±25 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Connection Diagram
16-Lead DIP
Top View



CD00441F

Order Information

Device Code	Package Code	Package Description
μA3486DC	7B	Ceramic DIP
μA3486PC	9B	Molded DIP

Function Table (Each Receiver)

Differential Inputs AB	Enable E	Output Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\ V < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

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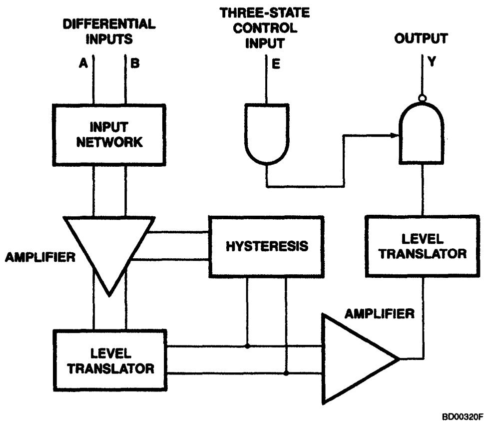
Block Diagram



Recommended Operating Conditions

Symbol	Characteristic	Value	Unit
V_{CC}	Supply Voltage	4.75 to 5.25	V
V_{CM}	Input Common Mode Voltage Range	−7.0 to +7.0	V
V_{ID}	Input Differential Voltage Range	6.0	V
T_A	Operating Temperature	0 to +70	°C

μA3486
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH	Three-State Control		2.0			V
V_{IL}	Input Voltage LOW	Three-State Control				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage[5]	$-7.0\ V \leq V_{IC} \leq 7.0\ V$, $V_{IH} = 2.0\ V$	$I_O = -0.4$ mA, $V_{OH} \geq 2.7$ V			0.2	V
			$I_O = 8.0$ mA, $V_{OL} \leq 0.5$ V			−0.2	
I_{IB}	Input Bias Current	$V_{CC} = 0$ V or 5.25 V, Other inputs at 0 V	$V_I = -10$ V			−3.25	mA
			$V_I = -3.0$ V			−1.50	
			$V_I = +3.0$ V			+1.50	
			$V_I = +10$ V			+3.25	
V_{OH}	Output Voltage HIGH[4]	$-7.0\ V \leq V_{CM} \leq 7.0\ V$, $V_{IH} = 2.0\ V$	$I_O = -0.4$ mA, $V_{ID} = 0.4$ V	2.7			V
V_{OL}	Output Voltage LOW		$I_O = 8.0$ mA, $V_{ID} = 0.4$ V			0.5	

μA3486 (Cont.)

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
I_{OZ}	Output Third State Leakage Current	$V_{I(D)} = +3.0$ V, $V_{IL} = 0.8$ V, $V_O = 0.5$ V			−40	μA
		$V_{I(D)} = -3.0$ V, $V_{IL} = 0.8$ V, $V_O = 2.7$ V			40	
I_{OS}	Output Short Circuit Current[3]	$V_{I(D)} = 3.0$ V, $V_{IH} = 2.0$ V, $V_O = 0$ V	−15		−100	mA
I_{IL}	Input Current LOW	Three-State Control $V_{IL} = 0.5$ V			−100	μA
I_{IH}	Input Current HIGH					μA
		Three-State Control $V_{IH} = 2.7$ V			20	
		Three-State Control $V_{IH} = 5.25$ V			100	
V_{IC}	Input Clamp Diode Voltage (Three-State Control)	Three-State Control $I_{IC} = -10$mA			−1.5	V
I_{CC}	Supply Current	$V_{IL} = 0$ V			85	mA

Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
	Propagation Delay Time Differential	Inputs to Outputs				
$t_{PHL(D)}$		Output HIGH to LOW		16	35	ns
$t_{PLH(D)}$		Output LOW to HIGH		16	30	ns
	Propagation Delay Time	Control to Output				
t_{PLZ}		Output LOW to Third State		24	35	ns
t_{PHZ}		Output HIGH to Third State		16	35	ns
t_{PZH}		Output Third State to HIGH		16	30	ns
t_{PZL}		Output Third State to LOW		16	30	ns

Notes

1. All currents into device leads are shown as positive, out of device leads are negative. All voltages referenced to ground unless otherwise noted.
2. Typical values are $T_A = 25°C$, $V_{CC} = 5.0$ V, and $V_{IC} = 0$ V.
3. Only one output at a time should be shorted.
4. Refer to EIA RS-422/3 for exact conditions. Input balance and V_{OH}/V_{OL} levels are tested simultaneously for worst case.
5. Differential input threshold voltage and guaranteed output levels are tested simultaneously for worst case.

Parameter Measurement Information

Figure 1 Propagation Delay Differential Input to Output

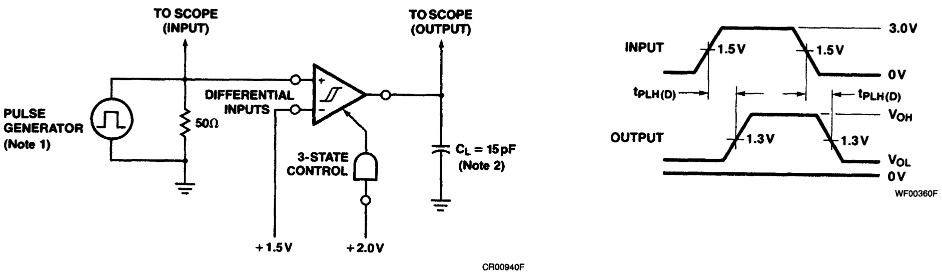
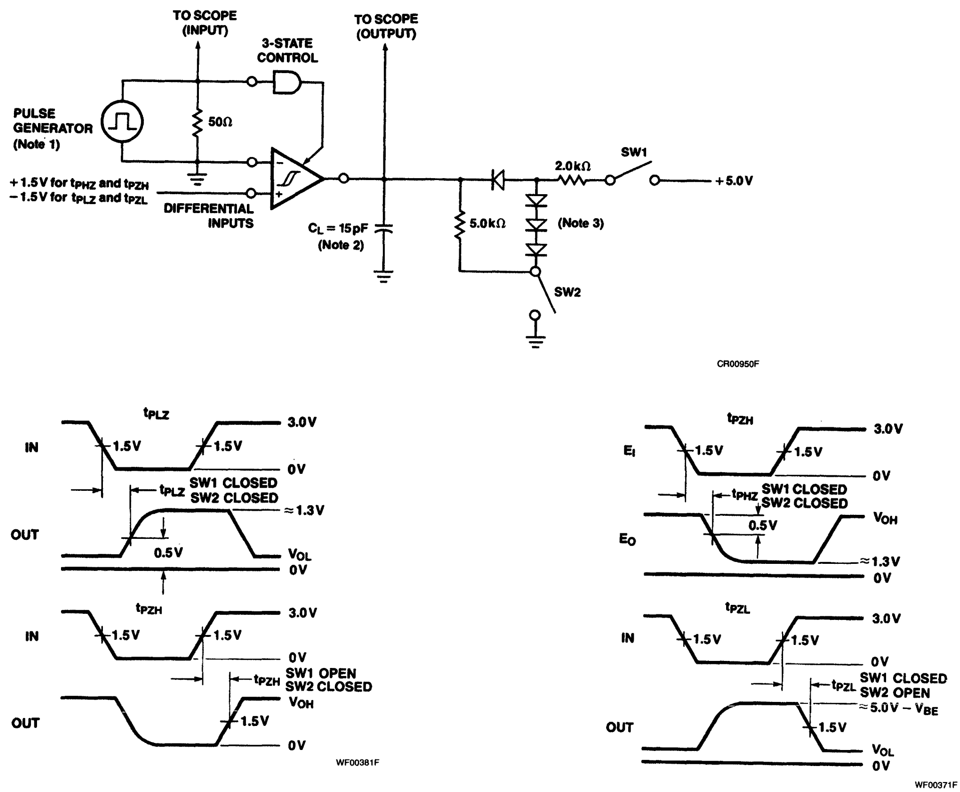


Figure 2 Propagation Delay Three-State Control Input to Output



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%), Z_O = 50 Ω.
2. C_L includes probe and jig cpacitance.
3. All diodes are IN916 or equivalent.

FAIRCHILD

A Schlumberger Company

μA3487 RS-422 Quad Line Driver With Three-State Outputs

Linear Division Interface Products

Description

Fairchild's RS-422 Quad Line Driver features four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltages digital interface circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. All input leads are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power-up and power-down.

- **Four Independent Driver Chains**
- **Three-State Outputs**
- **PNP High Impedance Inputs**
- **Fast Propagation Time**
- **TTL Compatible**
- **Single 5.0 V Supply Voltage**
- **Output Rise And Falls Times Less Than 20 ns**
- **Lead Compatible And Interchangeable With MC3487 And DS3487**

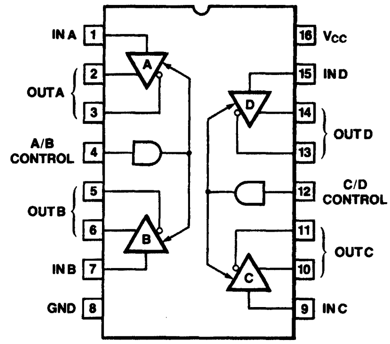
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Plastic DIP	1.04 W
Supply Voltage[3]	8.0 V
Input Voltage	5.5 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Connection Diagram 16-Lead DIP (Top View)



CD00451F

Order Information

Device Code	Package Code	Package Description
μA3487DC	7B	Ceramic DIP
μA3487PC	9B	Molded DIP

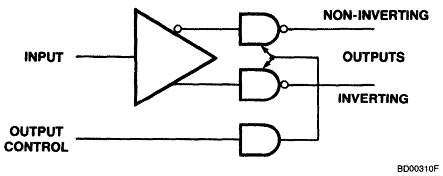
Function Table (Each Driver)

Input	Enable	Outputs Y	Outputs Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

9

Block Diagram



μA3487
Electrical Characteristics 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{IL}	Input Current LOW	V_{IL} = 0.5 V			−400	μA
I_{IH}	Input Current HIGH	V_{IH} = 2.7 V			+50	μA
		V_{IH} = 5.5 V			+100	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
V_{OL}	Output Voltage LOW	I_{OL} = 48 mA			0.5	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA	2.5			V
I_{OS}	Output Short Circuit Current[3]	V_{IH} = 2.0 V	−40		−140	mA
I_{OZ}	Output Leakage Current Hi-Z State	V_{IL} = 0.5 V, V_{IL} (z) = 0.8 V			+100	μA
		V_{IH} = 2.7 V, C_{IL} (z) = 0.8 V			+100	
$I_{OL(off)}$	Output Leakage Current	V_{OH} = 6.0 V, V_{CC} = 0 V			+100	μA
	Power Off	V_{OL} = −0.25 V, V_{CC} = 0 V			−100	
V_{OS}-$\overline{V}_{OS}$	Output Offset Voltage Difference[2]				±0.4	V
V_{OD}	Output Differential Voltage[2]		2.0			V
ΔV_{OD}	Output Differential Voltage Change				±0.4	V
I_{CCX}	Supply Current[4]	Control Leads Gnd			105	mA
I_{CC}		Control Leads 2.0 V			85	mA

μ**A3487** (Cont.)
Electrical Characteristics

Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C

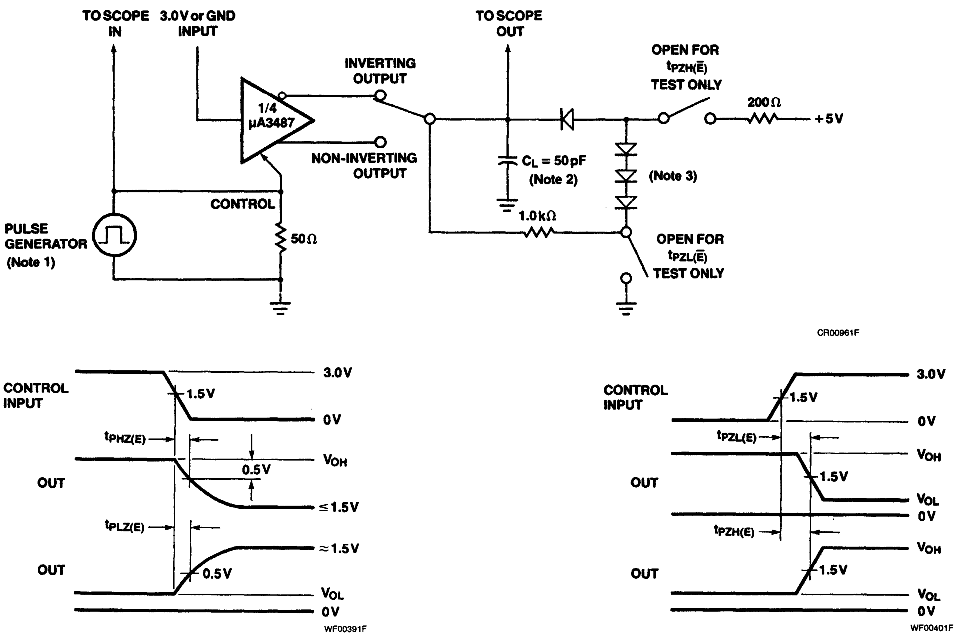
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Times	High to Low Input			20	ns
t_{PLH}		Low to High Input			20	ns
t_{THL}	Output Transition Times - Differential	High to Low Input			20	ns
t_{TLH}		Low to High Input			20	ns
$t_{PHZ(E)}$	Propagation Delay Control to Output	R_L = 200, C_L = 50 pF			25	ns
$t_{PLZ(E)}$		R_L = 200, C_L = 50 pF			25	ns
$t_{PZH(E)}$		R_L = ∞, C_L = 50 pF			30	ns
$t_{PZL(E)}$		R_L = 200, C_L = 50 pF			30	ns

Notes
1. Typical values are T_A = 25°C, V_{CC} = 5.0 V
2. See EIA Specification RS-422 for exact test conditions
3. Only one output may be shorted at a time
4. Circuit in three-state condition

9

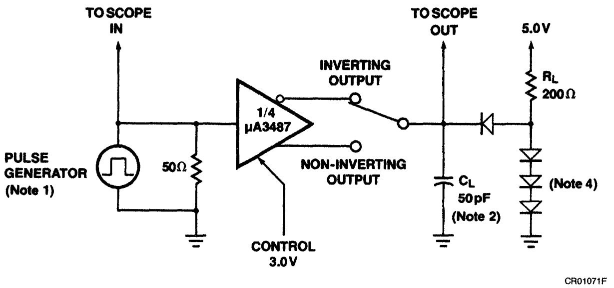
Parameter Measurement Information

Figure 1 Three-State Enable Test Circuit and Waveforms



Parameter Measurement Information (Cont.)

Figure 2 Propagation Delay Times Input to Output Waveforms and Test Circuit



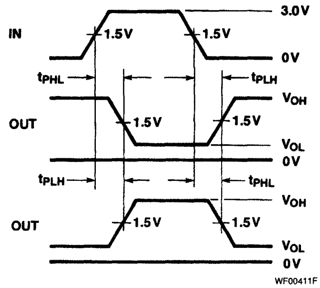
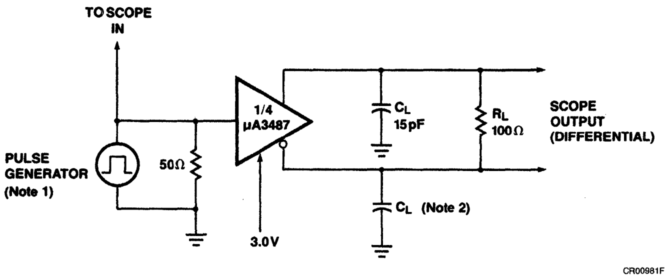
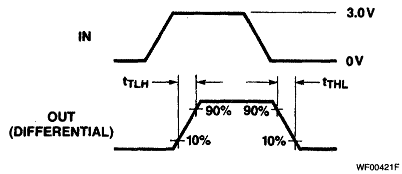


Figure 3 Output Transition Times Circuit and Waveforms





Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL} \leqslant$ 5.0 ns (10% to 90%), Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.
3. All diodes are IN3064 or equivalent.
4. All diodes are IN914 or equivalent.

FAIRCHILD

A Schlumberger Company

μA55107A • μA75107A μA75107B • μA75108B Dual Line Receivers

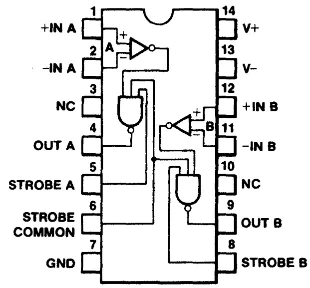
Linear Division Interface Products

Description

The devices in this series are high speed, two channel line receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3.0 V but can be increased to ±15 V by the use of input attenuators. Separate or common strobes are available. The μA55107A/μA75107A circuits feature an active pull-up (totem-pole output). The μA75108B circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the μA55110A/μA75110A line drivers. These line receivers are useful in high speed balanced, unbalanced and party-line transmission systems and as data comparators.

- **High Speed**
- **Standard Supply Voltages**
- **Dual Channels**
- **High Common Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Input Common Mode Voltage Range Of ±3.0 V**
- **Separate Or Common Strobes**
- **Wired-OR Output Capability**
- **High DC Noise Margins**
- **Strobe Input Clamp Diodes**
- **Input Is Diode Protected Against Power-Off Loading On B Version Devices**

Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



CD00930F

Order Information

Device Code	Package Code	Package Description
μA55107ADM	6A	Ceramic DIP
μA75107ADC	6A	Ceramic DIP
μA75107APC	9A	Molded DIP
μA75107ASC	KD	Molded Surface Mount
μA75107BDC	6A	Ceramic DIP
μA75107BPC	9A	Molded DIP
μA75107BSC	KD	Molded Surface Mount
μA75108BPC	9A	Molded DIP
μA75108BSC	KD	Molded Surface Mount

Absolute Maximum Ratings

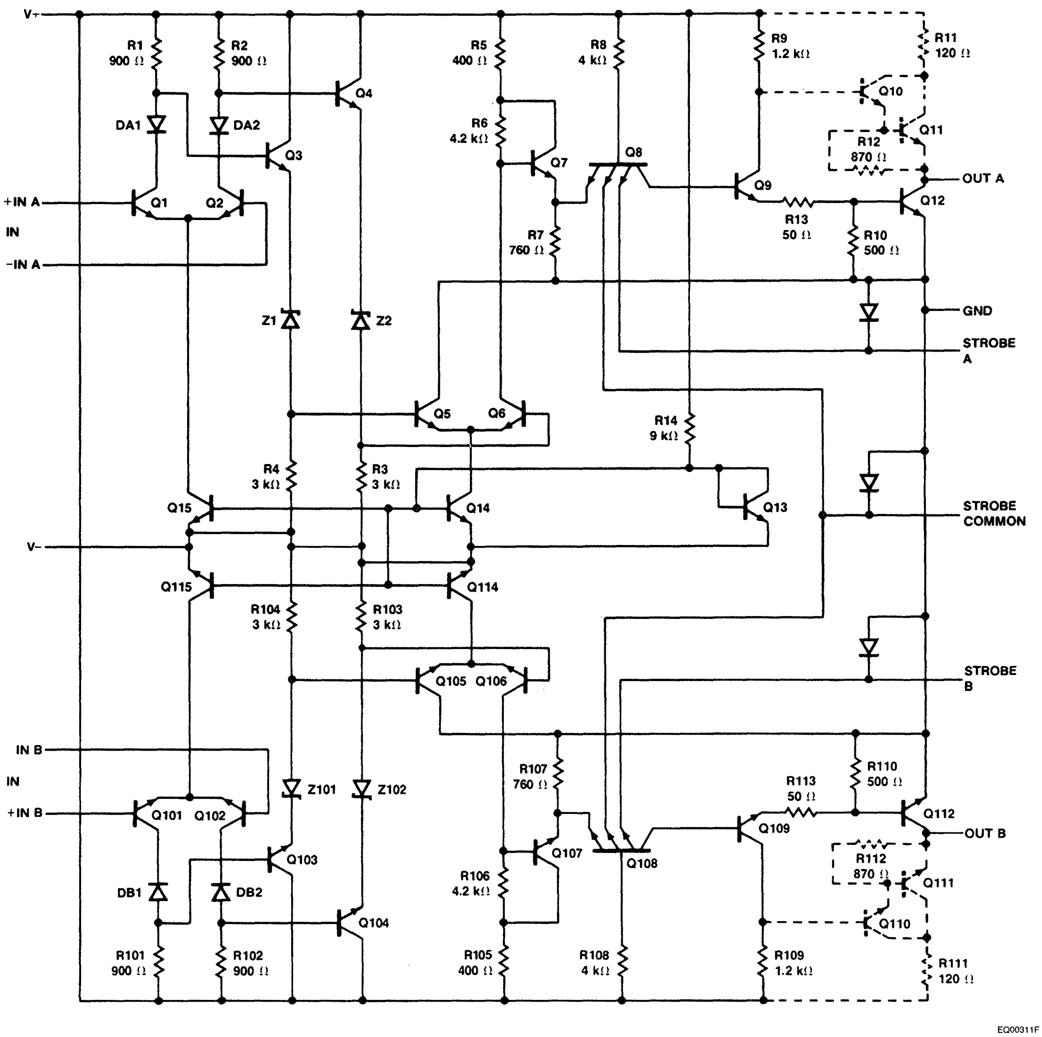
Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA55107A)	-55°C to +125°C
Commercial (μA75107A/B, μA75108B)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage[3]	±7.0 V
Differential Input Voltage[4]	±6.0 V
Common Mode Input Voltage[3]	±5.0 V
Strobe Input Voltage[3]	5.5 V

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. These voltages are with respect to network ground terminal.
4. These voltages are at the noninverting (+) terminal with respect to the inverting (−) terminal.

9

Equivalent Circuit

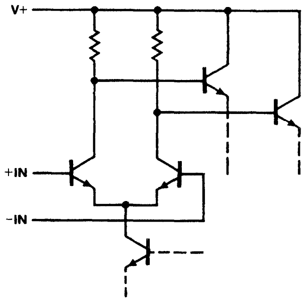


Note
Components shown with dashed lines are applicable to the μA55107A and μA75107B only. See description for differences between A and B versions.

Circuit Differences Between A and B Versions

The essential difference between the μA55107A/μA75107A and μA75107B versions is shown in the following schematics of the input stage:

A Version



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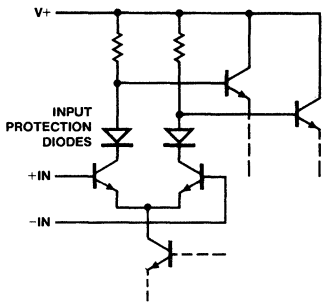
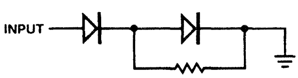
B Version



CR01830F

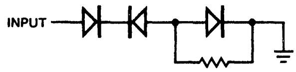
The input protection diodes are useful in certain party-line systems which may have multiple V + power supplies and, in which case, may be operated with some of the V + supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

A Version



CR01840F

B Version



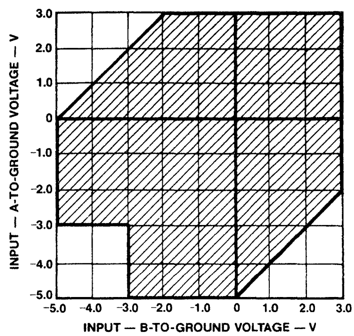
CR01850F

This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4 V. Since this is not a widespread application problem, both the A and B versions will be available. The ratings and characteristic specifications of the B versions are the same as those of the A versions.

Truth Table

Differential Inputs A-B	Strobes G	Strobes S	Output
$V_{ID} \geqslant 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	Indeterminate
$V_{ID} \leqslant -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

Recommended Combinations of Input Voltage for Line Receivers



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μA55107A, μA75107A, μA75107B
Electrical Characteristics Over recommended operating temperature range with V+ = Max and V− = Max, unless otherwise specified.[1, 3]

DC Characteristics

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
I_{IH}	Input Current HIGH	$V_{DIFF} = 0.5$ V, $V_{CM} = -3.0$ V to +3.0 V			30	75	μA
I_{IL}	Input Current LOW	$V_{DIFF} = -2.0$ V, $V_{CM} = -3.0$ V to +3.0 V				−10	μA
$I_{IH(G)}$	Gate Input Current HIGH	$V_{(G)} = 2.4$ V				40	μA
		$V_{(G)} = V+$				1.0	mA
$I_{IL(G)}$	Gate Input Current LOW	$V_{(G)} = 0.4$ V				−1.6	mA
$I_{IH(ST)}$	Strobe Input Current HIGH	$V_{(ST)} = 2.4$ V				80	μA
		$V_{(ST)} = V+$				2.0	mA
$I_{IL(ST)}$	Strobe Input Current LOW	$V_{(ST)} = 0.4$ V				−3.2	mA
V_{OH}	Output Voltage HIGH	$I_{OH} = -400$ μA, $V_{CM} = -3.0$ V to +3.0 V	V_{CC} = Min	2.4			V
V_{OL}	Output Voltage LOW	$I_{OL} = 16$ mA, $V_{CM} = -3.0$ V to +3.0 V	V_{CC} = Min			0.4	V
I_{OS}	Output Short Circuit Current[2]	$V_O = 0$ V		−18		−70	mA
I+	Positive Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ V, $T_A = 25°C$			18	30	mA
I−	Negative Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ V, $T_A = 25°C$			−8.4	−15	mA

AC Characteristics $V_{CC} = \pm 5.0$ V, $R_L = 390\ \Omega$, $C_L = 50$ pF, $T_A = 25°C$. (See Test Circuit)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$t_{PLH(D)}$	Propagation Delay Time			17	25	ns
$t_{PHL(D)}$				17	25	ns
$t_{PLH(S)}$				10	15	ns
$t_{PHL(S)}$				10	15	ns

μA75108B
DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input Current HIGH	$V_{DIFF} = 0.5$ V, $V_{CM} = -3.0$ V to +3.0 V		30	75	μA
I_{IL}	Input Current LOW	$V_{DIFF} = -2.0$ V, $V_{CM} = -3.0$ V to +3.0 V			−10	μA
$I_{IH(G)}$	Gate Input Current HIGH	$V_{(G)} = 2.4$ V			40	μA
		$V_{(G)} = V+$			1.0	mA
$I_{IL(G)}$	Gate Input Current LOW	$V_{(G)} = 0.4$ V			−1.6	mA
$I_{IH(ST)}$	Strobe Input Current HIGH	$V_{(ST)} = 2.4$ V			80	μA
		$V_{(ST)} = V+$			2.0	mA

μA75108B (Cont.)

Electrical Characteristics Over recommended operating temperature range with V+ = Max and V− = Max, unless otherwise specified.[1, 3]

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$I_{IL(ST)}$	Strobe Input Current LOW	$V_{(ST)} = 0.4$ V				−3.2	mA
V_{OL}	Output Voltage LOW	$I_{OL} = 16$ mA, $V_{CM} = -3.0$ V to +3.0 V	V_{CC} = Min			0.4	V
I_{OH}	Output Current HIGH	V_O = V+	V_{CC} = Min			250	μA
I+	Positive Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ V, $T_A = 25°C$			18	30	mA
I−	Negative Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ V, $T_A = 25°C$			−8.4	−15	mA

AC Characteristics $V_{CC} = \pm 5.0$ V, $R_L = 390\ \Omega$, $C_L = 15$ pF, $T_A = 25°C$. (See Test Circuit)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$t_{PLH(D)}$	Propagation Delay Time			19	25	ns
$t_{PHL(D)}$				19	25	ns
$t_{PLH(S)}$				13	20	ns
$t_{PHL(S)}$				13	20	ns

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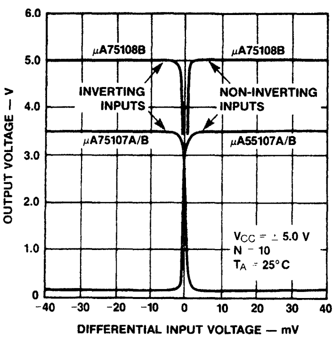
Notes
1. For μA55107A guaranteed supply voltage range is ±4.5 V to ±5.5 V and operating temperature range is $-55°C \leq T_A \leq +125°C$. For μA75107A/B and μA75108B guaranteed supply voltage range is ±4.75 V to ±5.25 V and operating temperature range is $0°C \leq T_A \leq 70°C$.
2. Not more than one output should be shorted at a time.
3. V_{CC} Max implies ±5.5 V or ±5.25 V, depending on device type.

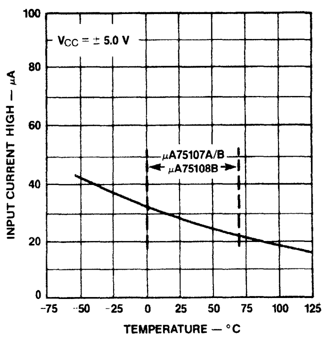
Typical Performance Curves

Output Voltage vs Differential Input Voltage



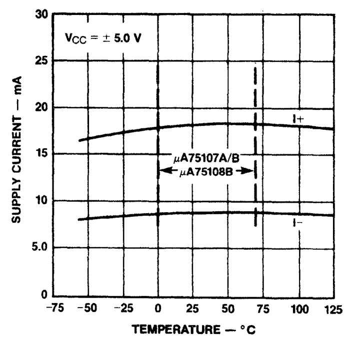
PC06141F

Input Current HIGH Into 1A or 2A vs Ambient Temperature



PC06151F

High Logic Level Supply Current vs Ambient Temperature



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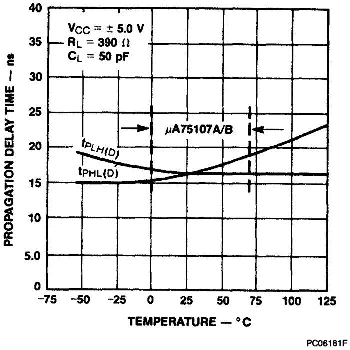
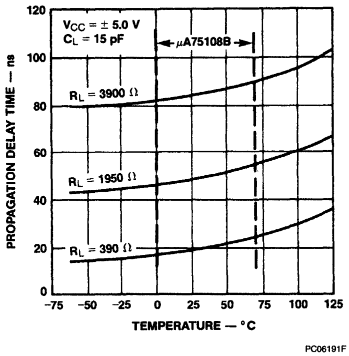
Typical Performance Curves (Cont.)

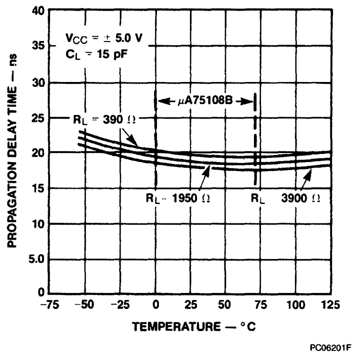
μA55107A, μA75107A/B Propagation Delay Time (Differential Inputs) vs Ambient Temperature



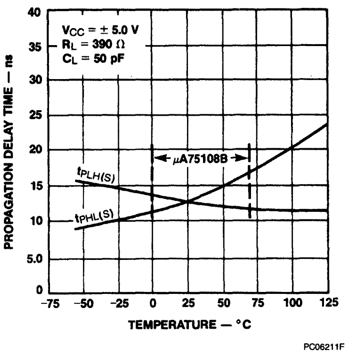
μA75108B Propagation Delay Time LOW-to-HIGH Level vs Ambient Temperature



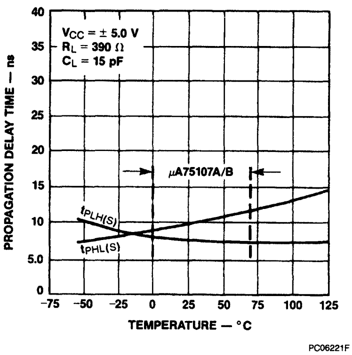
μA75108B Propagation Delay Time HIGH-to-LOW level vs Ambient Temperature



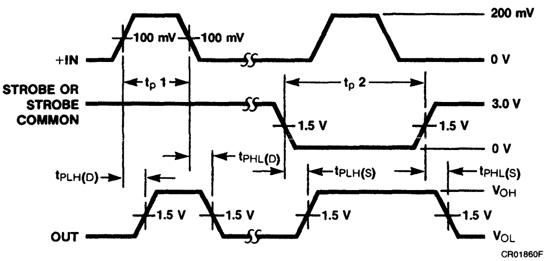
μA75108B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



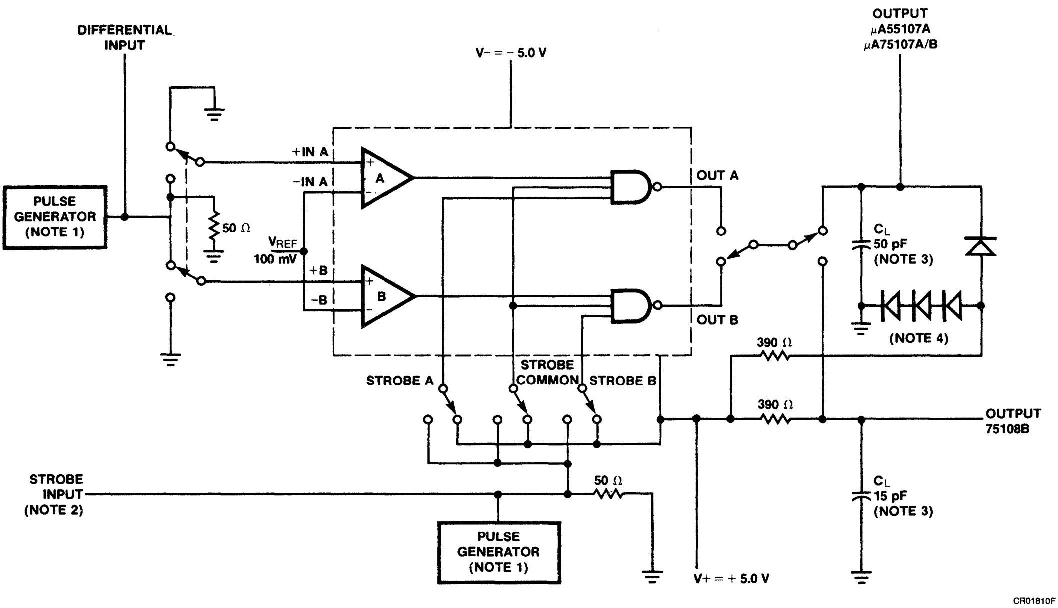
μA55107A, μA75107A/B Propagation Delay Time (Strobe Inputs) vs Ambient Temperature



Voltage Waveforms



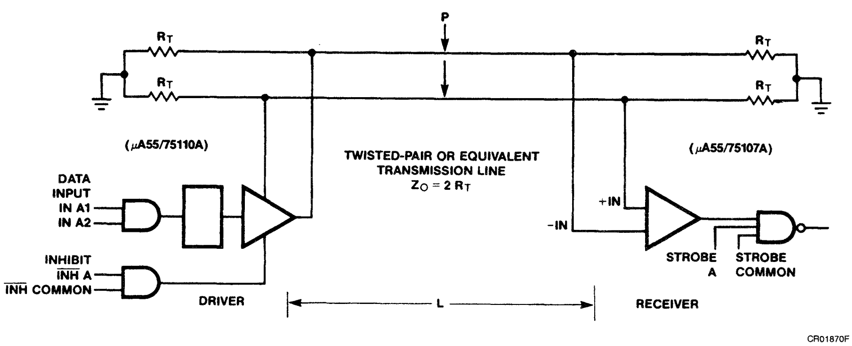
AC Test Circuit



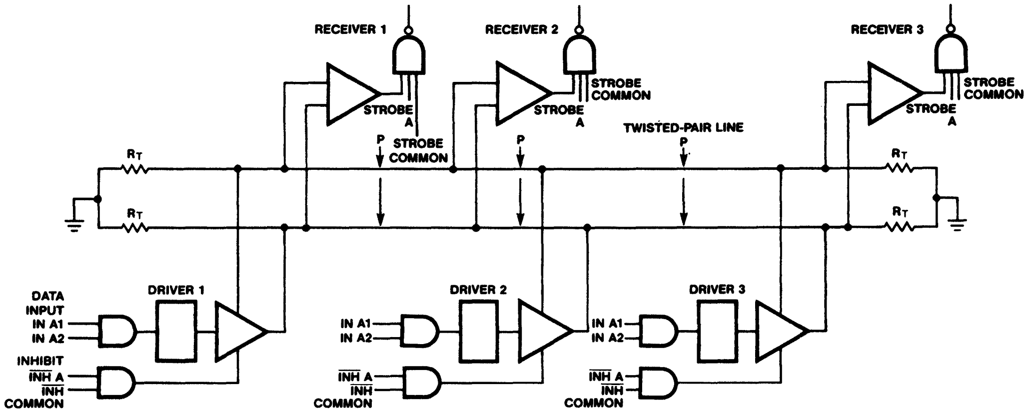
Notes

1. The pulse generators have the following characteristics: $t_r = t_f = 10 \pm 5.0$ ns, $t_{p1} = 500$ ns, PRR = 1.0 MHz, $t_{p2} = 1.0$ μs, PRR = 500 kHz, $Z_O = 50\ \Omega$.
2. Strobe input pulse is applied to Strobe A when inputs A1 − A2 are being tested; to common Strobe when inputs A1 − A2 or B1 − B2 are being tested; and to Strobe B when inputs B1 − B2 are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.

Basic Balanced-Line Transmission System



Data-Bus or Party-Line System



CR01880F

Application

The μA55107A, μA75107A dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Cross-talk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver input logic levels. The voltage difference is approximately:

$$V_{DIFF} \simeq 1/2\ I_{O(on)} \cdot R_T \quad (1)$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

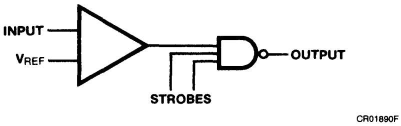
$$V_{DIFF} \simeq I_{O(on)} \cdot R_T \quad (2)$$

The strobe feature of the receivers and the inhibit feature of the drivers allow the μA55107A, μA75107A dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The μA55107A, μA75107A device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

The μA55107A, μA75107A dual line circuits may also be used in unbalanced or single line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

The receiver threshold level is established by applying a DC reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0 V to +3.0 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



Precautions in the Use of μA55107A, μA75107A and μA75108B Dual Line Receivers

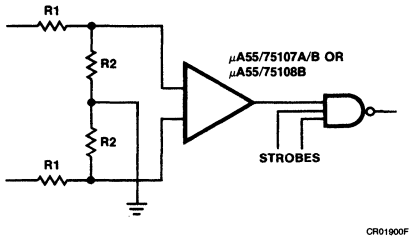
The following precaution should be observed when using or testing μA55107A, μA75107A line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0 V and +3.0 V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

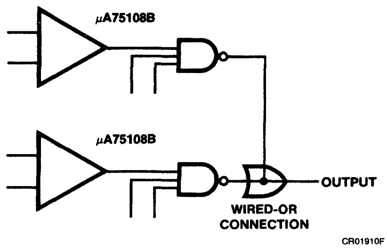
The μA55107A, μA75107A and μA75108B line receivers feature a common mode input voltage range of ±3.0 V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common mode range can be extended by the use of external input attenuators. Common mode input voltages can in this way be reduced to ±3.0 V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

The μA75108B line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other μA75108B outputs. This allows a level of logic to be implemented without additional logic delay.

Increasing Common Mode Input Voltage Range of Receiver



μA75108B Wired-OR Output Connections



9

FAIRCHILD

A Schlumberger Company

μA55110A • μA75110A Dual Line Drivers

Description

The μA55110A/μA75110A have improved output current regulation with supply voltage and temperature variations. The higher current outputs allow data to be transmitted over longer lines. These drivers offer optimum performance when used with the μA55107A, μA75107A, μA75107B, and μA75108B line receivers.

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by LOW logic levels on the inhibit inputs.

The inhibit feature is provided so the circuits can be used in party line or data bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party line system with other drivers. The output impedance of the driver in the inhibited mode is very high; the output impedance of output transistor is biased to cutoff.

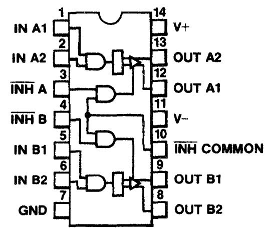
- **No Output Transients On Power-Up Or Down**
- **Improved Stability Over Supply Voltage And Temperature Ranges**
- **Constant Current, High Impedance Outputs**
- **High Speed 15 ns**
- **Standard Supply Voltages**
- **Inhibitor Available For Driver Selection**
- **High Common Mode Output Voltage Range (-3.0 V to 10 V)**
- **TTL Input Compatibility**
- **Extended Temperature Range**

Function Table

Inputs				Outputs	
Logic		Inhibitor			
A	B	C	D	A1/B1	A2/B2
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH, L = LOW, X = Don't Care

Connection Diagram 14-Lead DIP and SO-14 Package (Top View)



CD00341F

Order Information

Device Code	Package Code	Package Description
μA55110ADM	6A	Ceramic DIP
μA75110ADC	6A	Ceramic DIP
μA75110APC	9A	Molded DIP
μA75110ASC	KD	Molded Surface Mount

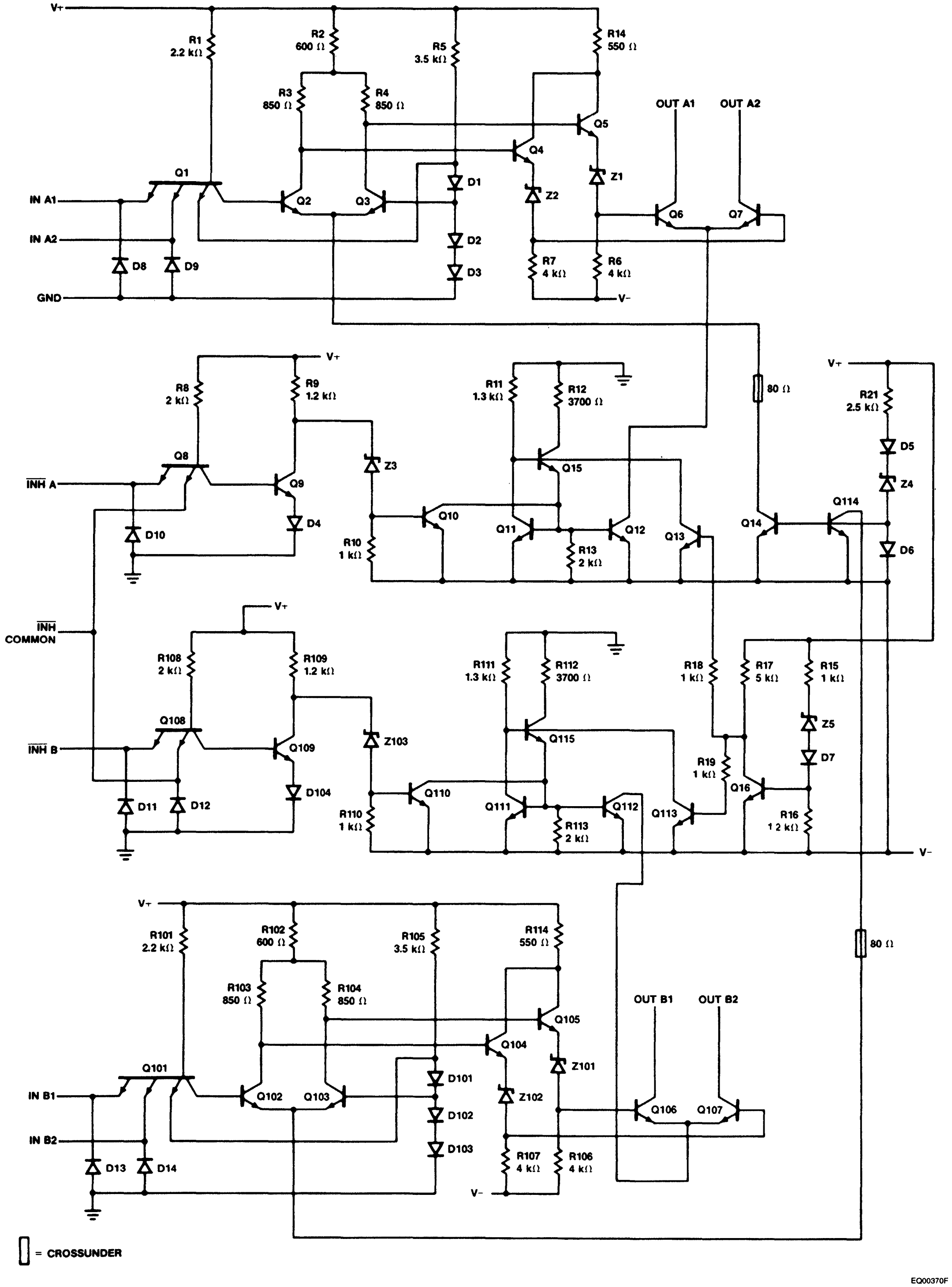
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μA55110A)	-55°C to +125°C
Commercial (μA75110A)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage[3]	±7.0 V
Input Voltage (any input)	5.5 V
Output Voltage (any output)	-5.0 V to 12 V

Notes

1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Voltage values are with respect to network ground terminal.

Equivalent Circuit



Recommended Operating Conditions[1]

Symbol	Characteristic	μA55110A			μA75110A			Unit
		Min	Typ	Max	Min	Typ	Max	
V+	Positive Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
V−	Negative Supply Voltage	−4.5	−5.0	−5.5	−4.75	−5.0	−5.25	V
$V_{CM}+$	Positive Common Mode Voltage	0		10	0		10	V
$V_{CM}-$	Negative Common Mode Voltage	0		−3.0	0		−3.0	V
T_A	Operating Temperature	−55	25	125	0	25	70	°C

μA55110A, μA75110A

Electrical Characteristics Over recommended operating temperature range, unless otherwise specified.

DC Characteristics

Symbol	Characteristic		Condition[2]	Min	Typ[3]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA		−0.9	−1.5	V
$I_{O(on)}$	On-State Output Current		V_{CC} = Max, V_O = 10 V		12	15	mA
			V_{CC} = Min, V_O = −3.0 V	6.5	12		
$I_{O(off)}$	Off-State Output Current		V_{CC} = Min, V_O = 10 V			100	μA
I_I	Input Current At Maximum Input Voltage	A, B or C Inputs	V_{CC} = Max, V_I = 5.5 V			1.0	mA
		D Input				2.0	
I_{IH}	Input Current HIGH	A, B or C Input	V_{CC} = Max, V_I = 2.4 V			40	μA
		D Input				80	
I_{IL}	Input Current LOW	A, B or C Inputs	V_{CC} = Max, V_I = 0.4 V			−3.0	mA
		D Input				−6.0	
$I+_{(on)}$	Positive Supply Current With Driver Enabled		V_{CC} = Max, A & B Inputs at 0.4 V, C & D Inputs at 2.0 V		23	35	mA
$I-_{(on)}$	Negative Supply Current With Driver Enabled				−34	−50	mA
$I+_{(off)}$	Positive Supply Current With Driver Inhibited		V_{CC} = Max, A, B, C, & D Inputs at 0.4 V		21		mA
$I-_{(off)}$	Negative Supply Current With Driver Inhibited				−17		mA

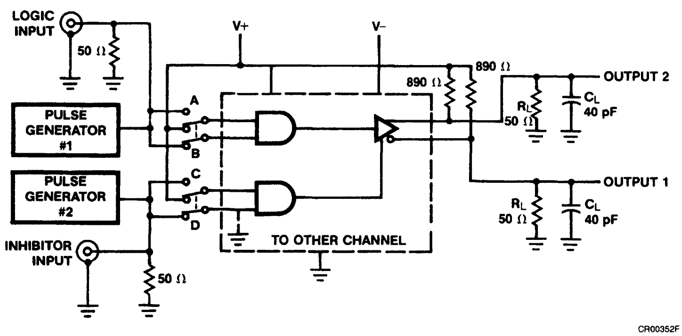
μA55110A, μA75110A (Cont.)
Electrical Characteristics

AC Characteristics $V_{CC} = \pm 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	From (Input)	To (Output)	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	$C_L = 40$ pF, $R_L = 50\ \Omega$ See *Test Circuit*	A or B	1 or 2		9.0	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9.0	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH		C or D	1 or 2		16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns

Notes
1. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.
2. For conditions shown as Min or Max, use appropriate value specified under recommended operating conditions.
3. All typical values are $V_{CC} = \pm 5.0$ V, $T_A = 25°C$

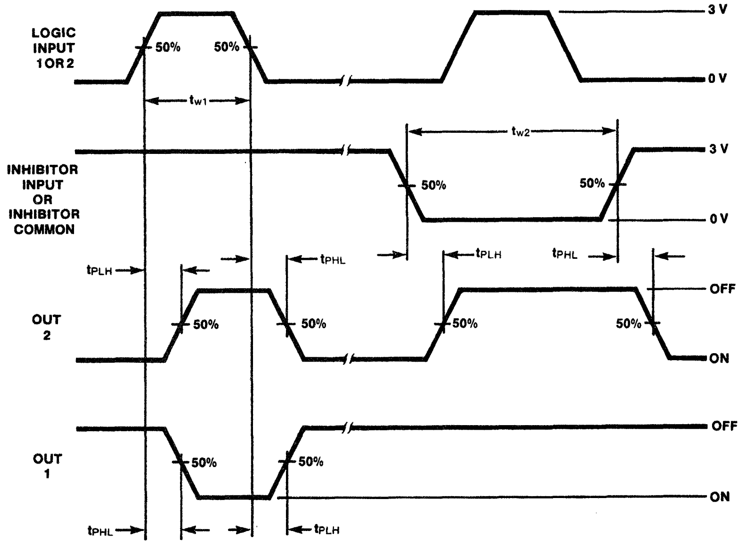
AC Test Circuit



Notes
1. The pulse generators have the following characteristics:
   $t_r = t_f = 10 \pm 5.0$ ns, $t_{w1} = 500$ ns, PRR = 1.0 MHz,
   $t_{W2} = 1.0\ \mu s$, PRR = 500 kHz, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

9

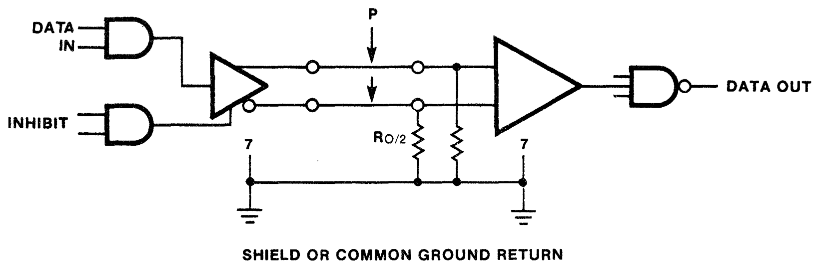
AC Waveforms



WF00122F

Typical Applications

Simplex Operation



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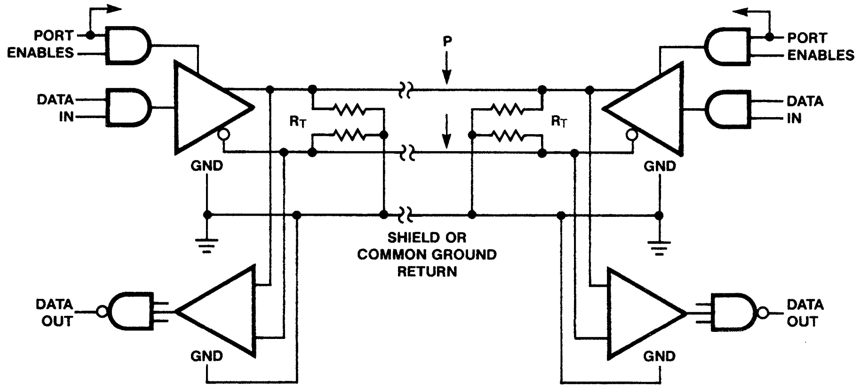
Typical Applications (Cont.)

Half-Duplex Operation



Notes

1. All drivers are μA75110A or μA55110A. Receivers are μA75107A or μA75108B. Twisted-pair or coaxial transmission line should be used for minimum noise and cross talk.
2. When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

9

FAIRCHILD

A Schlumberger Company

μA75150 RS-232C Dual Line Driver

Linear Division Interface Products

Description

The μA75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A rate of 20K bps can be transmitted with a full 2500 pF load. Other applications are in data transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12 V and −12 V power supplies.

- **Withstands Sustained Output Short Circuit To Any Low Impedance Voltage Between −25 V And +25 V**
- **2.0 μs Max Transition Time Through The +3.0 V To −3.0 V Transition Region Under Full 2500 pF Load**
- **Inputs Compatible With Most TTL And DTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With An External Capacitor At The Output**
- **Standard Supply Voltages ± 12 V**

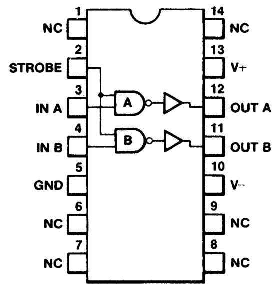
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Molded DIP	1.04 W
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	± 15 V
Input Voltage[3]	15 V
Applied Output Voltage[3]	± 25 V

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP and SO-14.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Voltage values are with respect to network ground.

Connection Diagram 14-Lead DIP (Top View)

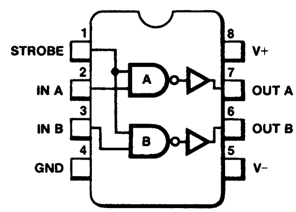


CD00880F

Order Information

Device Code	Package Code	Package Description
μA75150PC	9A	Molded DIP

Connection Diagram 8-Lead DIP and SO-8 Package (Top View)

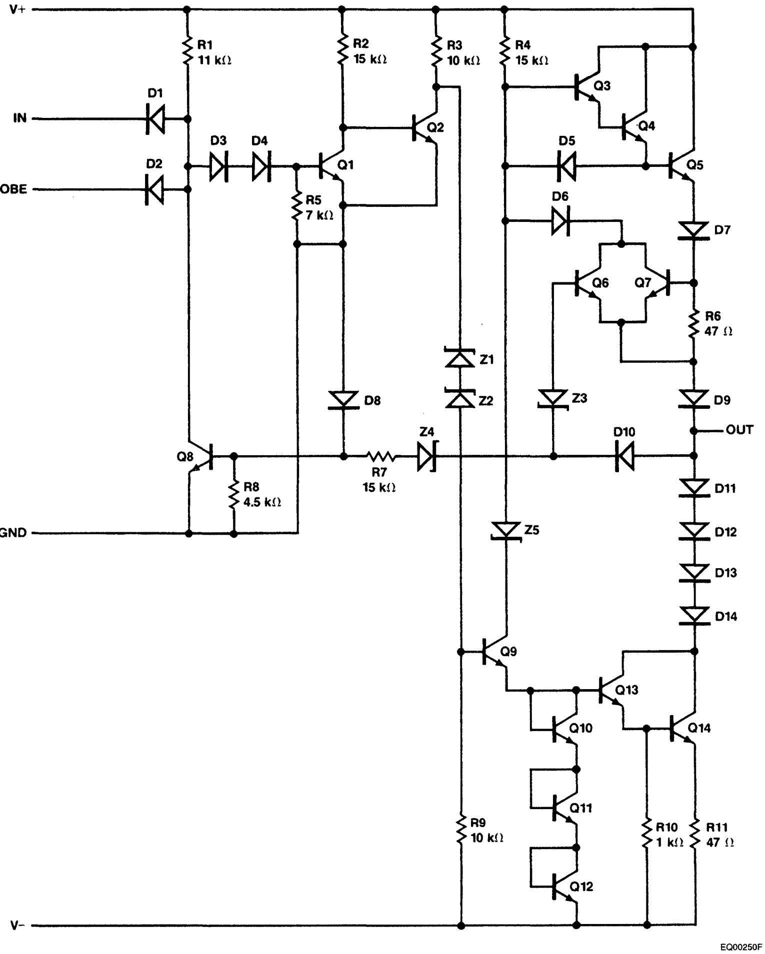


CD00870F

Order Information

Device Code	Package Code	Package Description
μA75150RC	6T	Ceramic DIP
μA75150TC	9T	Molded DIP
μA75150SC	KC	Molded Surface Mount

Equivalent Circuit (1/2 of Circuit)



Note
Component values shown are nominal.

Recommended Operating Conditions

Symbol	Characteristics	Min	Typ	Max	Unit
V +	Positive Supply Voltage	10.8	12	13.2	V
V −	Negative Supply Voltage	− 10.8	− 12	− 13.2	V
V_I	Input Voltage	0		5.5	V
V_O	Applied Output Voltage			± 15	V
T_A	Operating Temperature	0	25	70	°C

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μA75150
Electrical Characteristics $T_A = 0$ to 70°C, unless otherwise specified.[1]

DC Characteristics

Symbol	Characteristic	Condition		Figure	Min	Typ[2]	Max	Unit
V_{IH}	Input Voltage HIGH			1	2.0			V
V_{IL}	Input Voltage LOW			2			0.8	V
V_{OH}	Output Voltage HIGH	V+ = 10.8 V, V− = −13.2 V, $V_{IL} = 0.8$ V, $R_L = 3.0$ kΩ to 7.0 kΩ		2	5.0	8.0		V
V_{OL}	Output Voltage LOW	$V_{CC} = \pm 10.8$ V, $V_{IH} = 2.0$ V, $R_L = 3.0$ kΩ to 7.0 kΩ		1		−8.0	−5.0	V
I_{IH}	Input Current HIGH	$V_{CC} = \pm 13.2$ V, $V_I = 2.4$ V	Data Input	3		1.0	10	μA
			Strobe Input			2.0	20	
I_{IL}	Input Current LOW	$V_{CC} = \pm 13.2$ V, $V_I = 0.4$	Data Input	3		−1.0	−1.6	mA
			Strobe Input			−2.0	−3.2	
I_{OS}	Output Short Circuit Current	$V_{CC} = \pm 13.2$ V	$V_O = 25$ V	4		2.0		mA
			$V_O = -25$ V			−3.0		
			$V_O = 0$ V, $V_I = 3.0$ V			15		
			$V_O = 0$ V, $V_I = 0$ V			−15		
$I+_H$	Positive Supply Current HIGH	$V_{CC} = \pm 13.2$ V, $V_I = 3.0$ V, $R_L = 3.0$ kΩ, $T_A = 25$°C		5		10	22	mA
$I-_H$	Negative Supply Current HIGH					−1.0	−10	mA
$I+_L$	Positive Supply Current LOW	$V_{CC} = \pm 13.2$ V $V_I = 3.0$ V, $R_L = 3.0$ kΩ, $T_A = 25$°C		5		8.0	17	mA
$I-_L$	Negative Supply Current LOW					−9.0	−20	mA

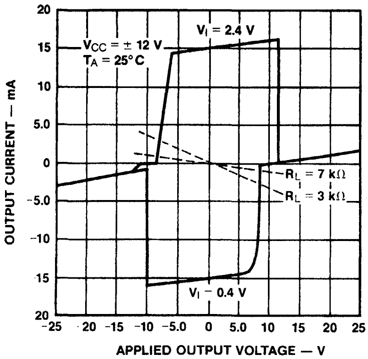
AC Characteristics $V_{CC} = \pm 12$ V, $T_A = 25$°C.

Symbol	Characteristic	Condition	Figure	Min	Typ[2]	Max	Unit
t_{TLH}	Transition Time, Output LOW to HIGH	$C_L = 2500$ pF, $R_L = 3.0$ kΩ to 7.0 kΩ	6	0.2	1.4	2.0	μs
t_{THL}	Transition Time, Output HIGH to LOW			0.2	1.5	2.0	μs
t_{TLH}	Transition Time, Output LOW to HIGH	$C_L = 15$ pF, $R_L = 7.0$ kΩ	6		40		ns
t_{THL}	Transition Time, Output HIGH to LOW				20		ns
t_{PLH}	Propagation Delay Time, Output LOW to HIGH	$C_L = 15$ pF, $R_L = 7.0$ kΩ	6		60		ns
t_{PHL}	Propagation Delay Time, Output HIGH to LOW				45		ns

Notes
1. The algebraic convention where the most positive (least negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5.0 V is the maximum, the typical value is a more negative voltage.
2. All typical values are at $V_{CC} = \pm 12$ V, $T_A = 25$°C.

Typical Performance Curves

Typical Output Current vs Applied Output Voltage



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Test Circuits

Figure 1 V_{IH}, V_{OL}

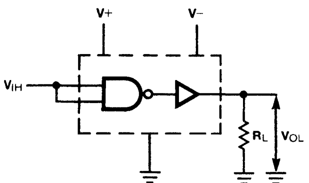

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Figure 2 V_{IL}, V_{OH} (Note 1)

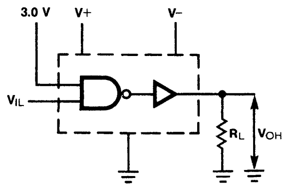

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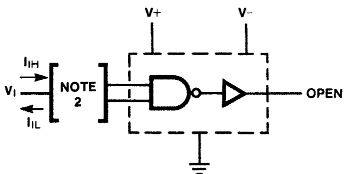
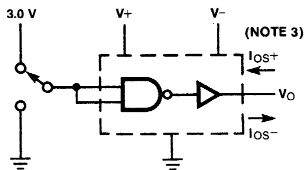
Figure 3 I_{IH}, I_{IL}



CR01731F

Figure 4 I_{OS}



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Notes

1. Each input is tested separately.
2. When testing I_{IH}, the other input is at 3.0 V; when testing I_{IL}, the other input is open.
3. I_{OS} is tested for both input conditions at each of the specified output conditions.

Figure 5 I_{+H}, I_{-H}, I_{+L}, I_{-L} (Note 1)

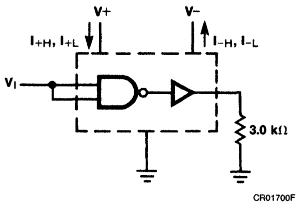
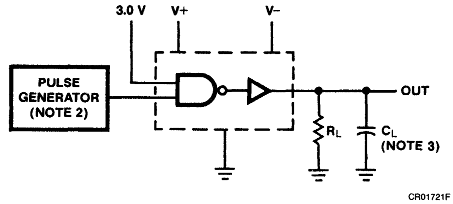


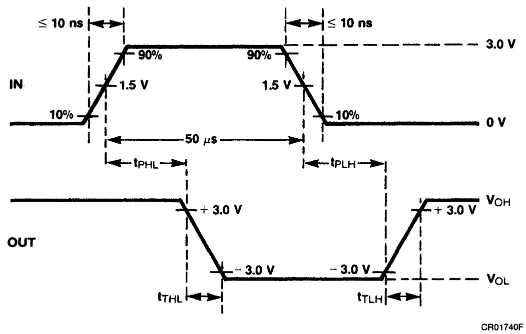
Figure 6 Switching Characteristics



Notes

1. Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
2. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_O = 50\ \Omega$.
3. C_L includes probe and jig capacitance.

Voltage Waveforms



FAIRCHILD
A Schlumberger Company

μA75154 RS-232C Quad Line Receiver

Linear Division Interface Products

Description

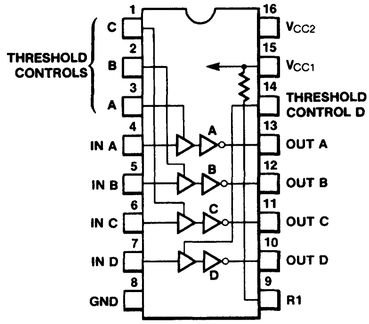
The μA75154 is a monolithic quad line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single line, point-to-point data transmission and for level translators. Operation is normally from a single 5.0 V supply; however, a built-in option allows operation from a 12 V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold control terminals are connected to the V_{CC1} terminal, lead 15, even if power is being supplied via the alternate V_{CC2} terminal, lead 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode of operation, if the input voltage goes to zero, the output voltage will remain LOW or HIGH as determined by the previous input.

For fail-safe operation, the threshold control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open circuit condition, the output will go HIGH regardless of the previous input condition.

- **Input Resistance — 3.0 kΩ To 7.0 kΩ Over Full RS-232C Voltage Range**
- **Input Threshold Adjustable To Meet Fail-Safe Requirements Without Using External Components**
- **Built-In Hysteresis For Increased Noise Immunity**
- **Inverting Output Compatible With DTL Or TTL**
- **Output With Active Pull-Up For Symmetrical Switching Speeds**
- **Standard Supply Voltages — 5.0 V Or 12 V**

Connection Diagram
16-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA75154DC	6B	Ceramic DIP
μA75154PC	9B	Molded DIP

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage (Lead 15)[3]	7.0 V
Alternate Supply Voltage (Lead 16)[3]	14 V
Input Voltage[3]	±25 V

Notes
1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. Voltage values are with respect to network ground terminal.

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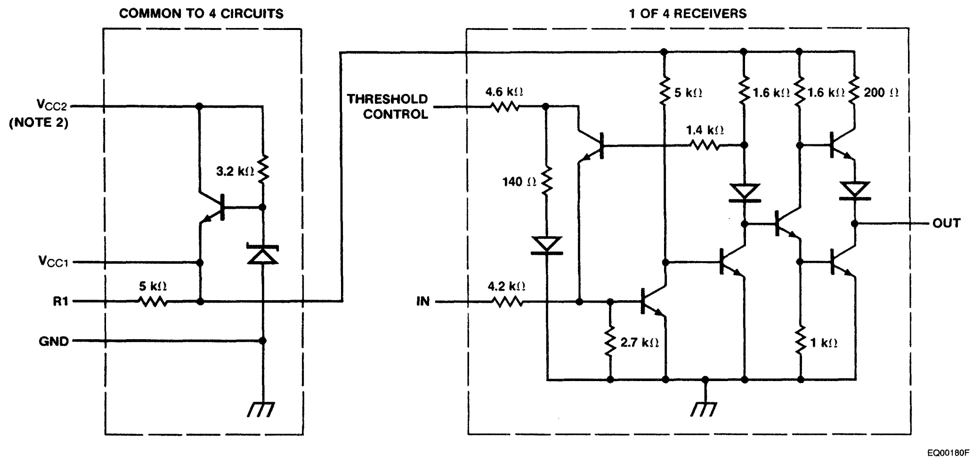
Equivalent Circuit (Note 1)



Notes

1. Component values shown are normal.
2. When using V_{CC1}, V_{CC2} may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control leads.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC1}	Supply Voltage	4.5	5	5.5	V
V_{CC2}	Supply Voltage	10.8	12	13.2	V
V_I	Input Voltage			± 15	V
N	Normalized Fan Out from Each Output			10	
T_A	Operating Temperature	0	25	70	°C

μA75154
Electrical Characteristics $T_A = 0$ to 70°C unless otherwise specified.[3]

DC Characteristics

Symbol	Characteristic		Condition	Figure	Min	Typ[2]	Max	Unit
V_{IH}	Input Voltage HIGH			1	3.0			V
V_{IL}	Input Voltage LOW			1			−3.0	V
V_{TH+}	Positive-Going Threshold Voltage	Normal Operation		1	0.8	2.2	3.0	V
		Fail-Safe Operation			0.8	2.2	3.0	
V_{TH-}	Negative-Going Threshold Voltage	Normal Operation		1	−3.0	−1.1	0	V
		Fail-Safe Operation			0.8	1.4	3.0	
$(V_{TH+}) - (V_{TH-})$	Hysteresis	Normal Operation		1	0.8	3.3	6.0	V
		Fail-Safe Operation			0	0.8	2.2	
V_{OH}	Output Voltage HIGH		$I_{OH} = -400$ μA	1	2.4	3.5		V
V_{OL}	Output Voltage LOW		$I_{OL} = 16$ mA	1		0.23	0.4	V
R_I	Input Resistance		$\Delta V_I = -25$ V to −14 V	2	3.0	5.0	7.0	kΩ
			$\Delta V_I = -14$ V to −3.0 V		3.0	5.0	7.0	
			$\Delta V_I = -3.0$ V to +3.0 V		3.0	6.0		
			$\Delta V_I = 3.0$ V to 14 V		3.0	5.0	7.0	
			$\Delta V_I = 14$ V to 25 V		3.0	5.0	7.0	
$V_{I\,(open)}$	Input Open Circuit Voltage		$I_I = 0$ mA	3	0	0.2	2.0	V
I_{OS}	Output Short Circuit Current[1]		$V_{CC1} = 5.5$ V, $V_I = -5$ V	4	−10	−20	−40	mA
I_{CC1}	Supply Current from V_{CC1}		$V_{CC1} = 5.5$ V, $T_A = 25$°C	5		20	35	mA
I_{CC2}	Supply Current from V_{CC2}		$V_{CC2} = 13.2$ V, $T_A = 25$°C			23	40	mA

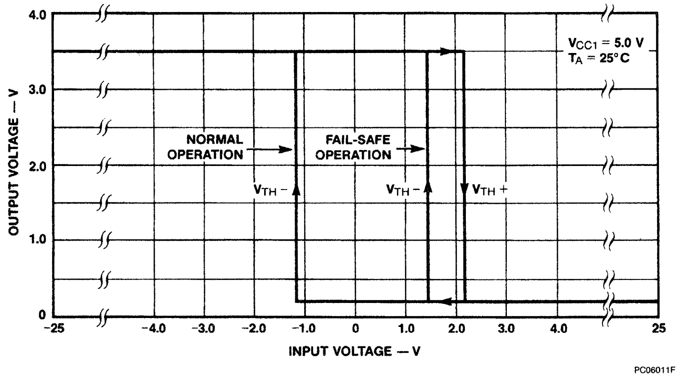
AC Characteristics $V_{CC1} = 5.0$ V, $T_A = 25$°C

Symbol	Characteristic	Condition	Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW-to-HIGH	$C_L = 50$ pF, $R_L = 390$ Ω	6		22		ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW				20		ns
t_{TLH}	Transition Time, LOW-to-HIGH				9.0		ns
t_{THL}	Transition Time, HIGH-to-LOW				6.0		ns

Notes
1. Not more than one output should be shorted at a time.
2. All typical values are at $V_I = 5.0$ V, $T_A = 25$°C.
3. The algebraic convention where the most positive (least negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3.0 V is the maximum, the minimum limit is a more negative voltage.

Typical Characteristics

Output Voltage vs Input Voltage (Note 1)

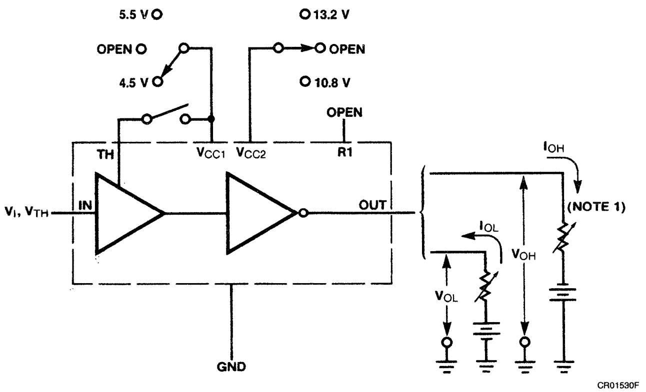


Note

1. For normal operation, the threshold controls are connected to V_{CC1}. For fail-safe operation, the threshold controls are open.

DC Test Circuits

Figure 1 V_{IH}, V_{IL}, V_{TH+}, V_{TH-}, V_{OH}, V_{OL}



Note

1. Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

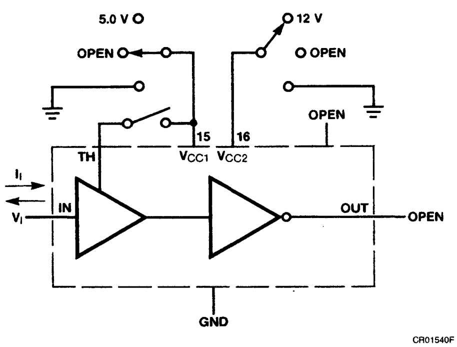
DC Test Circuits (Cont.)

Test Table

Test	Measure	In	T	Out	V_{CC1}	V_{CC2}
Open circuit input (fail-safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
$V_{TH+\ Min}$, $V_{TH-\ Min}$ (fail-safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
$V_{TH-\ Min}$ (normal)	V_{OH}	Note 1	Lead 15	I_{OH}	5.5 V and TH	Open
	V_{OH}	Note 1	Lead 15	I_{OH}	TH	13.2 V
$V_{IL\ Max}$, $V_{TH-\ Min}$ (normal)	V_{OH}	−3.0 V	Lead 15	I_{OH}	5.5 V and TH	Open
	V_{OH}	−3.0 V	Lead 15	I_{OH}	TH	13.2 V
$V_{IH\ Min}$, $V_{TH+\ Max}$, $V_{TH-\ Max}$ (fail-safe)	V_{OL}	3.0 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3.0 V	Open	I_{OL}	Open	10.8 V
$V_{IH\ Min}$, $V_{TH+\ Max}$ (normal)	V_{OL}	3.0 V	Lead 15	I_{OL}	4.5 V and TH	Open
	V_{OL}	3.0 V	Lead 15	I_{OL}	TH	10.8 V
$V_{TH-\ Max}$ (normal)	V_{OL}	Note 2	Lead 15	I_{OL}	5.5 V and TH	Open
	V_{OL}	Note 2	Lead 15	I_{OL}	TH	13.2 V

Notes
1. Momentarily apply −5.0 V, then 0.8 V.
2. Momentarily apply 5.0 V, then ground.

Figure 2 R_I



$$R_I = \frac{\Delta V_I}{\Delta I_I}$$

Test Table

TH	V_{CC1}	V_{CC2}
Open	5.0 V	Open
Open	GND	Open
Open	Open	Open
Lead 15	TH and 5.0 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Lead 15	TH	12 V
Lead 15	TH	GND
Lead 15	TH	Open

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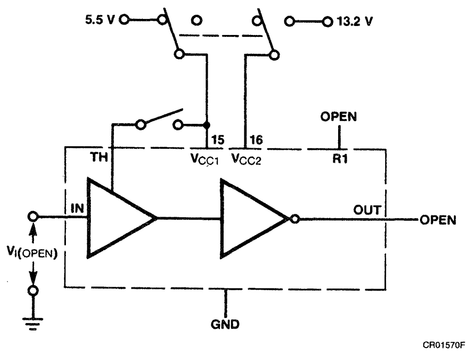
DC Test Circuits (Cont.)

Figure 3 $V_{I(open)}$



Test Table

TH	V_{CC1}	V_{CC2}
Open	5.5 V	Open
Lead 15	5.5 V	Open
Open	Open	13.2 V
Lead 15	TH	13.2 V

Figure 4 I_{OS} (Note 1)

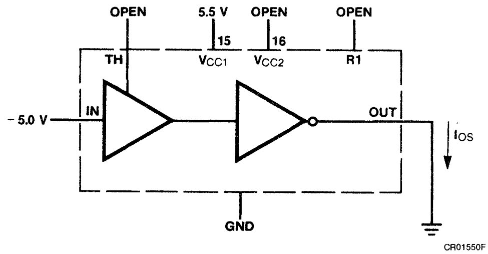
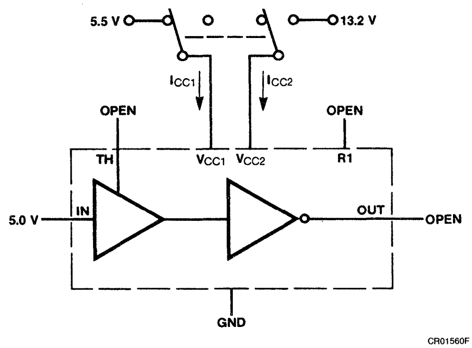


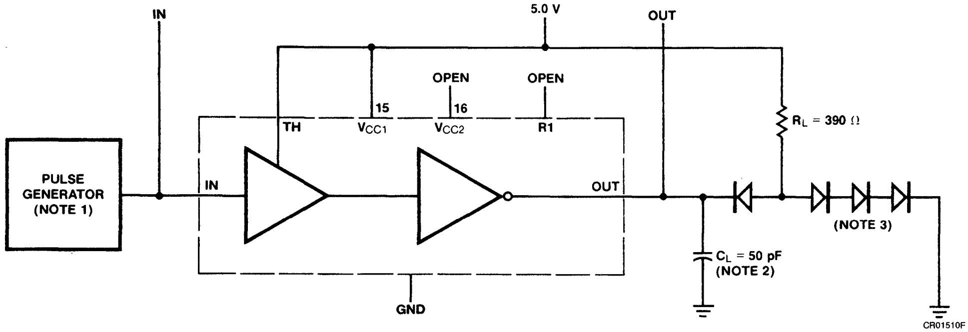
Figure 5 I_{CC} (Note 2)



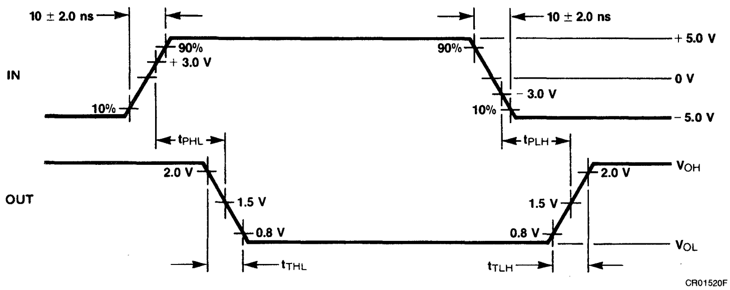
Notes

1. Each output is tested separately.
2. All four line receivers are tested simultaneously. Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

AC Test Circuit



Voltage Waveforms



Notes

1. The pulse generator has the following characteristics: $t_W = 200$ ns, duty cycle $\leq 20\%$, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

FAIRCHILD

A Schlumberger Company

μA75450/60/70 Series Dual Peripheral Drivers

Linear Division Interface Products

Description

The μA75400 series of devices are dual high speed general purpose interface drivers that convert TTL and DTL logic levels to high current drive capability. The μA75450 features two TTL NAND gates and two uncommitted transistors. The μA75451, μA75452, and μA75453 feature two standard series 74 TTL gates in AND, NAND and OR configurations respectively, driving the base of two high voltage, high current, uncommitted collector output transistors.

The μA75400 series offers flexibility in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers, and memory drivers.

- **No Latch-Up Up To 55 V**
- **High Output Current Capability**
- **TTL Or DTL Input Compatibility**
- **Input Clamp Diodes**
- **5.0 V Supply Voltage**

Absolute Maximum Ratings

	μA75450	μA75451 μA75452 μA75453 μA75461 μA75462 μA75471 μA75472
Storage Temperature Range[1]		
Ceramic DIP	−65°C to +175°C	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C	−65°C to +150°C
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Lead Temperature		
Ceramic DIP (soldering, 60 s)	300°C	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C	265°C
Internal Power Dissipation[2, 3]		
14L-Ceramic DIP	1.36 W	
14L-Molded DIP	1.04 W	
8L-Ceramic DIP		1.30 W
8L-Molded DIP		0.93 W
SO-8		0.81 W
Supply Voltage[4]	7.0 V	7.0 V
Input Voltage[4]	5.5 V	5.5 V
Inter-emitter Voltage[5]	5.5 V	5.5 V
V_{CC} to Substrate Voltage[9]	35 V	
Collector to Substrate Voltage[9]	35 V	
Collector to Base Voltage	35 V	
Collector to Emitter Voltage[6]	30 V	
Emitter to Base Voltage	5.0 V	
Output Voltage[4 and 7]		Table 2
Continuous Collector Current[8]	300 mA	
Continuous Output Current[8]		300 mA

Notes

1. μA75452 is Molded DIP and SO-8 only.
2. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
3. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, the 8L-Ceramic DIP at 8.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
4. Voltage values are with respect to network ground terminal unless otherwise specified.
5. This is the voltage between two emitters of a mulitiple emitter input transistor.
6. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
7. This is the maximum voltage which should be applied to any output when it is in the off state.
8. Both halves of these dual circuits may conduct rated current simultaneously.
9. For the μA75450 only, the substrate (Lead 8), must always be at the most negative device voltage for proper operation.

Test Table 1 Operating Temperature Range and Supply Voltage Range

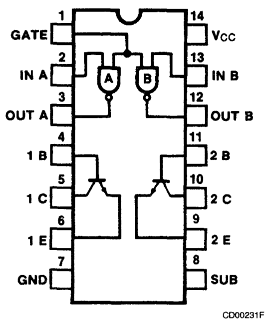
Symbol	Characteristic	μA75000 Series
T_A	Operating Temperature	0°C to 70°C
V_{CC}	Supply Voltage	+4.75 V to +5.25 V

Test Table 2

Symbol	Characteristic	μA7545X	μA75461 μA75462	μA75471 μA75472
V_{OH}	Maximum Output	30 V	35 V	80 V
V_S	Maximum, Latch-up	20 V	30 V	55 V

μA75450
Dual Positive AND Peripheral Drivers

Connection Diagram
14-Lead DIP
(Top View)

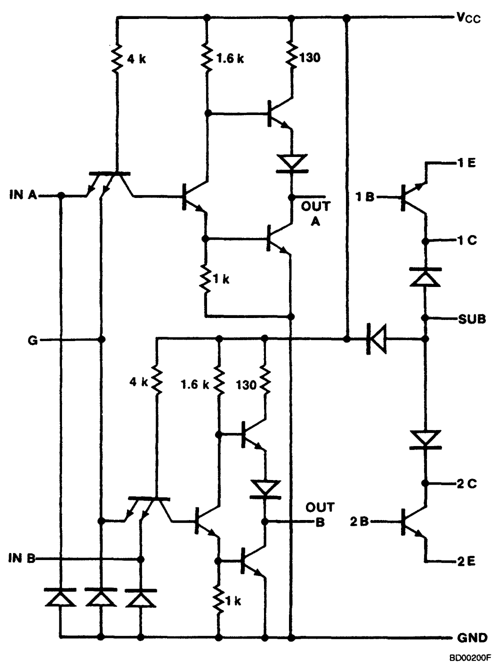


Logic Function
Positive Logic: $Z = \overline{XY}$ (gate only)
$Z = XY$ (gate and transistor)

Order Information

Device Code	Package Code	Package Description
μA75450DC	6A	Ceramic DIP
μA75450PC	9A	Molded DIP

Equivalent Circuit



All resistor values in ohms

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μA75450

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

TTL Gates

Symbol	Characteristic		Condition	Test Figure	Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			1	2.0			V
V_{IL}	Input Voltage LOW			2			0.8	V
V_{IC}	Input Clamp Diode Voltage		V_{CC} = Min, I_I = −12 mA	3			−1.5	V
V_{OH}	Output Voltage HIGH		V_{CC} = Min, V_{IL} = 0.8 V, I_{OH} = −400 μA	2	2.4	3.3		V
V_{OL}	Output Voltage LOW		V_{CC} = Min, V_{IH} = 2.0 V, I_{OL} = 16 mA	1		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A	V_{CC} = Max, V_I = 5.5 V	4			1.0	mA
		Input G					2.0	mA
I_{IH}	Input Current HIGH	Input A	V_{CC} = Max, V_I = 2.4 V	4			40	μA
		Input G					80	
I_{IL}	Input Current LOW	Input A	V_{CC} = Max, V_I = 0.4 V	3			−1.6	mA
		Input G					−3.2	
I_{OS}	Output Short Circuit Current[2]		V_{CC} = Max	5	−18		−55	mA
I_{CCH}	Supply Current HIGH		V_{CC} = Max, V_I = 0 V	6		2.0	4.0	mA
I_{CCL}	Supply Current LOW		V_{CC} = Max, V_I = 5.0 V			6.0	11	

Output Transistors (Note 4)

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 100 μA, I_E = 0 μA	35			V
$V_{(BR)CER}$	Collector to Base Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω	30			V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage	I_E = 100 μA, I_C = 0 μA	5.0			V
h_{FE}	Static Forward Current Transfer Ratio[3]	V_{CE} = 3.0 V, I_C = 100 mA, T_A = 25°C	25			
		V_{CE} = 3.0 V, I_C = 300 mA, T_A = 25°C	30			
		V_{CE} = 3.0 V, I_C = 100 mA	20			
		V_{CE} = 3.0 V, I_C = 300 mA	25			
$V_{BE(sat)}$	Base to Emitter Voltage[3]	I_B = 10 mA, I_C = 100 mA		0.85	1.0	V
		I_B = 30 mA, I_C = 300 mA		1.05	1.2	
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage[3]	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA		0.5	0.7	

μA75450 (Cont.)

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

TTL Gates

Symbol	Characteristic	Condition	Test Figure	μA75450B Min	μA75450B Typ	μA75450B Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	C_L = 15 pF, R_L = 400 Ω	12		12	22	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				8.0	15	ns

Output Transistors

Symbol	Characteristic	Condition[3]	Test Figure	Min	Typ	Max	Unit
t_d	Delay Time	I_C = 200 mA, $V_{BE(off)}$ = −1.0 V, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, C_L = 15 pF, R_L = 50 Ω	13		8.0	15	ns
t_r	Rise Time				12	20	ns
t_S	Storage Time				7.0	15	ns
t_f	Fall Time				6.0	15	ns

Gates and Transistors Combined

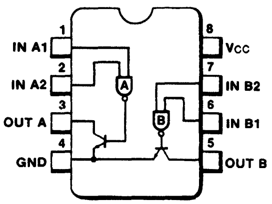
Symbol	Characteristic	Condition	Test Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	I_C = 200 mA, C_L = 15 pF, R_L = 50 Ω	14		20	30	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				20	30	ns
t_{TLH}	Transition Time, LOW to HIGH				7.0	12	ns
t_{THL}	Transition Time, HIGH to LOW				9.0	15	ns
V_{OH}	HIGH Level Output Voltage After Switching	V_I = 20 V, I_C ≈ 300 mA, R_{BE} = 500 Ω	15	V_I−6.5			mV

Notes

1. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Not more than one output should be shorted at a time.
3. These parameters must be measured using the pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
4. Voltage and current values shown are nominal; exact values vary slightly with transistor parameter.

μA75451, μA75461, μA75471
Dual Positive AND Peripheral Drivers

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



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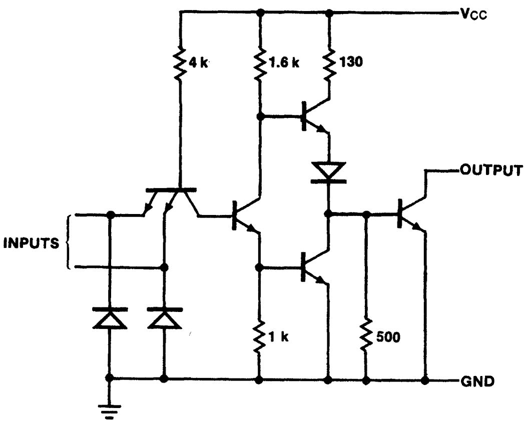
Order Information

Device Code	Package Code	Package Description
μA75451RC	6T	Ceramic DIP
μA75451SC	KC	Molded Surface Mount
μA75451TC	9T	Molded DIP
μA75461TC	9T	Molded DIP
μA75471TC	9T	Molded DIP

Equivalent Circuit (1/2 of Circuit)



BD00211F

Notes
Component values shown are nominal.
All resistor values in ohms.

Truth Table

Inputs		Output
X	Y	Z
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = HIGH Level, L = LOW Level

μA75451

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

Symbol	Characteristic	Condition	Test Figure	μA75451 Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH		7	2.0			V
V_{IL}	Input Voltage LOW		7			0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_I = −12 mA	8			−1.5	V
I_{OH}	Output Current HIGH[2]	V_{CC} = Min, V_{IH} = 2.0 V	7			100	μA
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA	7		0.25	0.4	V
		V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 300 mA			0.5	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V	9			1.0	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.4 V	9			40	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	8		−1.0	−1.6	mA
I_{CCH}	Supply Current HIGH	V_{CC} = Max, V_I = 5.0 V	10		7.0	11	mA
I_{CCL}	Supply Current LOW	V_{CC} = Max, V_I = 0 V			52	65	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Test Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω	14		18	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				25	25	ns
t_{TLH}	Transition Time, LOW to HIGH				5.0	8.0	ns
t_{THL}	Transition Time, HIGH to LOW				7.0	12	ns
V_{OH}	HIGH Level Output Voltage After Switching[3]	$I_O \approx$ 300 mA	15	V_I−6.5			mV

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μA75461, μA75471

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

Symbol	Characteristic	Condition	Test Figure	μA75461 Min	μA75461 Typ[1]	μA75461 Max	μA75471 Min	μA75471 Typ[1]	μA75471 Max	Unit
V_{IH}	Input Voltage HIGH		7	2.0			2.0			V
V_{IL}	Input Voltage LOW		7			0.8			0.8	V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_I = −12 mA	8		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	Output Current HIGH[2]	V_{CC} = Min, V_{IH} = 2.0 V	7			100			100	μA
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA	7		0.16	0.4		0.16	0.4	V
		V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 300 mA			0.35	0.7		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V	9			1.0			1.0	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.4 V	9			40			40	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	8		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current HIGH	V_{CC} = Max, V_I = 5.0 V	10		8.0	11		8.0	11	mA
I_{CCL}	Supply Current LOW	V_{CC} = Max, V_I = 0 V			61	76		61	76	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

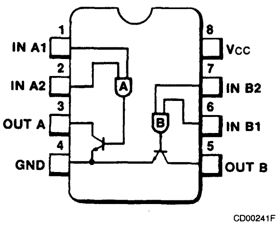
Symbol	Characteristic	Condition	Test Figure	μA75461 Min	μA75461 Typ	μA75461 Max	μA75471 Min	μA75471 Typ	μA75471 Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω	14		35	55		35	55	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				25	40		25	40	ns
t_{TLH}	Transition Time, LOW to HIGH				8	20		8.0	20	ns
t_{THL}	Transition Time, HIGH to LOW				10	20		10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching[3]	I_O ≈ 300 mA	15	V_I − 10			V_I − 18			mV

Notes

1. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. V_{OH} = 30 V for μA75451, 35 V for μA75461, 80 V for μA75471.
3. V_I = 20 V for μA75451, 30 V for μA75461, 55 V for μA75471.

μA75452, μA75462, μA75472
Dual Positive NAND Peripheral Driver

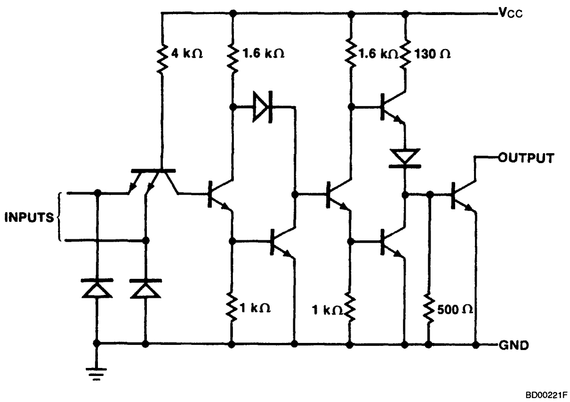
Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

Device Code	Package Code	Package Description
μA75452SC	KC	Molded Surface Mount
μA75452TC	9T	Molded DIP
μA75462TC	9T	Molded DIP
μA75472TC	9T	Molded DIP

Equivalent Circuit (1/2 of Circuit)



Notes
Component values shown are nominal.
All resistor values in ohms.

Truth Table

Inputs		Output
1	2	
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = HIGH Level, L = LOW Level

9

μA75452

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

Symbol	Characteristic	Condition	Test Figure	μA75452B			Unit
				Min	Typ[1]	Max	
V_{IH}	Input Voltage HIGH		7	2.0			V
V_{IL}	Input Voltage LOW		7			0.8	V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_I = −12 mA	8			−1.5	V
I_{OH}	Output Current HIGH[2]	V_{CC} = Min, V_{IL} = 0.8 V	7			100	μA
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IH} = 2.0 V, I_{OL} = 100 mA	7		0.25	0.4	V
		V_{CC} = Min, V_{IH} = 2.0 V, I_{OL} = 300 mA			0.5	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V	9			1.0	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.4 V	9			40	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	8		−1.0	−1.6	mA
I_{CCH}	Supply Current HIGH	V_{CC} = Max, V_I = 0 V	10		11	14	mA
I_{CCL}	Supply Current LOW	V_{CC} = Max, V_I = 5.0 V			56	71	mA

μA75452

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Test Figure	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, LOW to HIGH	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω	14		25	35	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				22	35	ns
t_{TLH}	Transition Time, LOW to HIGH				5.0	8.0	ns
t_{THL}	Transition Time, HIGH to LOW				7.0	12	ns
V_{OH}	HIGH Level Output Voltage After Switching[3]	$I_O \approx$ 300 mA	15	V_I − 6.5			mV

μA75462/μA75472

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

Symbol	Characteristic	Condition	Test Figure	μA75462			μA75472			Unit
				Min	Typ[1]	Max	Min	Typ[1]	Max	
V_{IH}	Input Voltage HIGH		7	2.0			2.0			V
V_{IL}	Input Voltage LOW		7			0.8			0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_I = −12 mA	8		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	Output Current HIGH[2]	V_{CC} = Min, V_{IL} = 0.8 V	7			100			100	μA
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IH} = 2.0 V, I_{OL} = 100 mA	7		0.16	0.4		0.16	0.4	V
		V_{CC} = Min, V_{IH} = 2.0 V, I_{OL} = 300 mA			0.35	0.7		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V	9			1.0			1.0	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.4 V	9			40			40	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	8		−1.0	−1.6		−1.0	−1.6	mA
I_{CCH}	Supply Current HIGH	V_{CC} = Max, V_I = 0 V	10		13	17		13	17	mA
I_{CCL}	Supply Current LOW	V_{CC} = Max, V_I = 5.0 V			65	76		65	76	mA

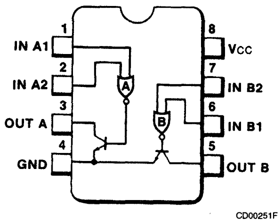
AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Test Figure	μA75462			μA75472			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω	14		50	65		45	65	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				40	50		30	50	ns
t_{TLH}	Transition Time, LOW to HIGH				12	25		13	25	ns
t_{THL}	Transition Time, HIGH to LOW				15	20		10	20	ns
V_{OH}	HIGH Level Output Voltage After Switching[3]	I_O ≈ 300 mA	15	V_I − 10			V_I − 18			mV

Notes
1. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. V_{OH} = 30 V for μA75452, 35 V for μA75462, 80 V for μA75472.
3. V_S = 20 V for μA75452, 30 V for μA75462 and 55 V for μA75472.

μA75453
Dual Positive OR Peripheral Drivers

Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Truth Table

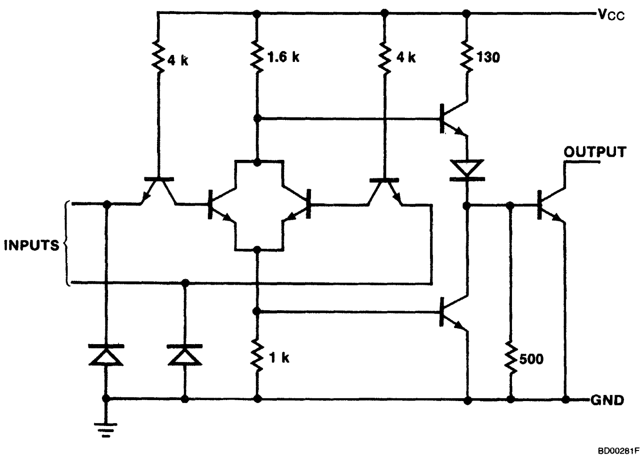
Inputs		Output
1	2	
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = HIGH Level, L = LOW Level

Order Information

Device Code	Package Code	Package Description
μA75453RC	6T	Ceramic DIP
μA75453SC	KC	Molded Surface Mount
μA75453TC	9T	Molded DIP

Equivalent Circuit (1/2 of Circuit)



Notes
Component values shown are nominal.
All resistor values in ohms.

μA75453

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, (use Test Table 1), unless otherwise indicated.

DC Characteristics

Symbol	Characteristic	Condition	Test Figure	Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH		7	2.0			V
V_{IL}	Input Voltage LOW		7			0.8	V
V_{IC}	Input Clamp Diode Voltage	V_{CC} = Min, I_I = −12 mA	8			−1.5	V
I_{OH}	Output Current HIGH	V_{CC} = Min, V_{OH} = 30 V, V_{IH} = 2.0 V	7			100	μA
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 100 mA	7		0.25	0.4	V
		V_{CC} = Min, V_{IL} = 0.8 V, I_{OL} = 300 mA			0.5	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V	9			1.0	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.4 V	9			40	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	8		−1.0	−1.6	mA
I_{CCH}	Supply Current HIGH	V_{CC} = Max, V_I = 5.0 V	11		8.0	11	mA
I_{CCL}	Supply Current LOW	V_{CC} = Max, V_I = 0 V			54	68	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Test Figure	μA75453			Unit
				Min	Typ	Max	
t_{PLH}	Propagation Delay Time, LOW to HIGH	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω	14		18	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW				16	25	ns
t_{TLH}	Transition Time, LOW to HIGH				5.0	8.0	ns
t_{THL}	Transition Time, HIGH to LOW				7.0	12	ns
V_{OH}	HIGH Level Output Voltage After Switching	V_I = 20 V, $I_O \approx$ 300 mA	15	V_I − 6.5			mV

Notes

1. All typical values are at V_{CC} = 5.0 V, T_A = 25°C.

Characteristics Measurement Information

DC Test Circuits (Note 1)

Figure 1 V_{IH}, V_{OL} (Note 2)

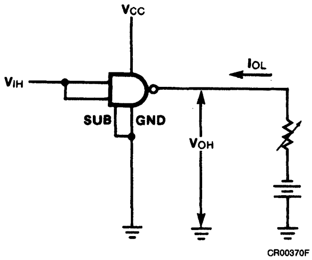


Figure 2 V_{IL}, V_{OH} (Note 3)

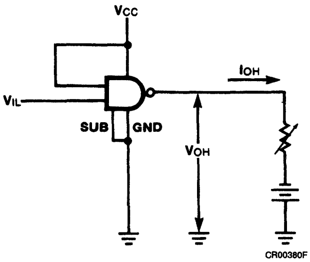
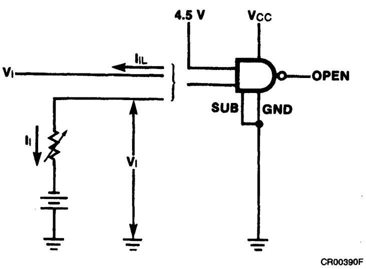


Figure 3 V_{IC}, I_{IL} (Notes 3 and 4)



Notes
1. Arrows indicate actual direction of current flow. Current into a terminal is a positive value.
2. Both inputs are tested simultaneously.
3. Each input is tested separately.
4. When testing V_{IC}, input not under test is open.
5. Each gate is tested separately.
6. Both gates are tested simultaneously.

Figure 4 I_I, I_{IH} (Note 3)

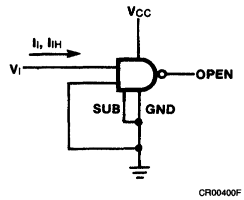


Figure 5 I_{OS} (Note 5)

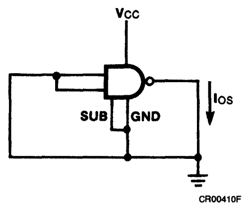


Figure 6 I_{CCH}, I_{CCL} (Note 6)

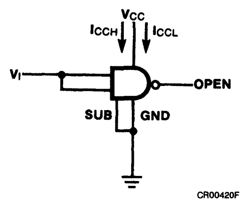
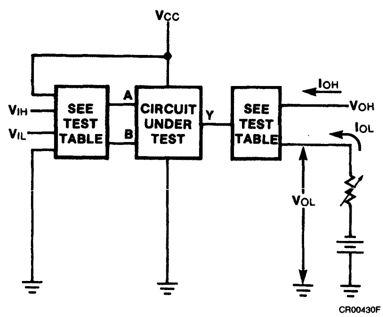


Figure 7 V_{IH}, V_{IL}, I_{OH}, V_{OL} (Note 3)



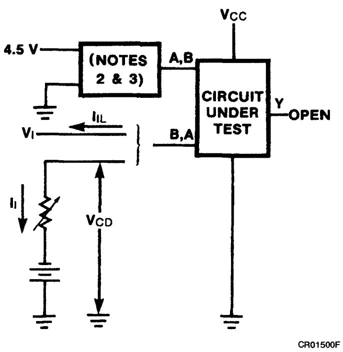
Characteristics Measurement Information (Cont.)

DC Test Circuits (Note 5)

Test Table 2

Circuit	Input Under Test	Other Input	Output	
			Apply	Measure
μA754X1	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
μA754X2	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
μA754X3	V_{IH} V_{IL}	GND V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}

Figure 8 V_{IC}, I_{IL} (Note 1)



Notes

1. Each input is tested separately.
2. When testing I_{IL} μA75400, the input not under test is grounded. For all other circuits it is at 4.5 V.
3. When testing V_{IC}, input not under test is open.
4. Both gates are tested simultaneously.
5. Arrows indicate actual direction of current flow. Current into a terminal is a position value.

Figure 9 I_I, I_{IH} (Note 1)

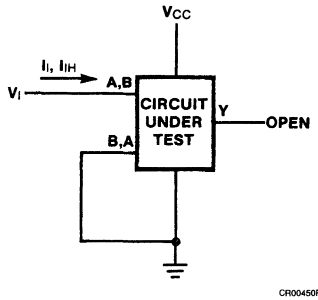


Figure 10 I_{CCH}, I_{CCL} **for AND, NAND Circuits** (Note 4)

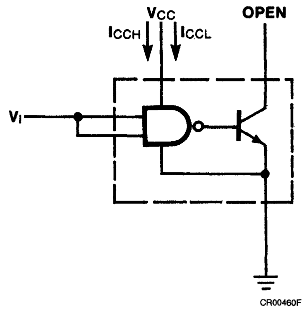
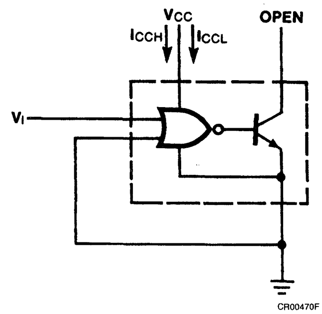


Figure 11 I_{CCH}, I_{CCL} **for OR, NOR Circuits** (Note 4)

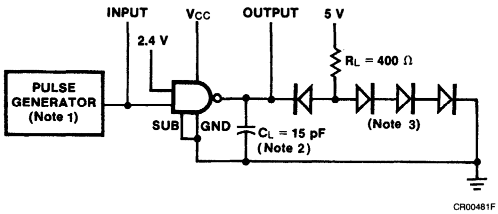


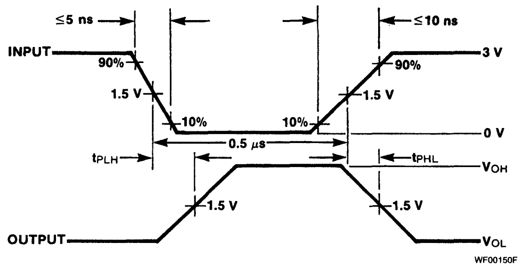
9

Characteristics Measurement Information (Cont.)

Switching Characteristics

Figure 12 Propagation Delay Times, Each Gate (μA75450 Only)

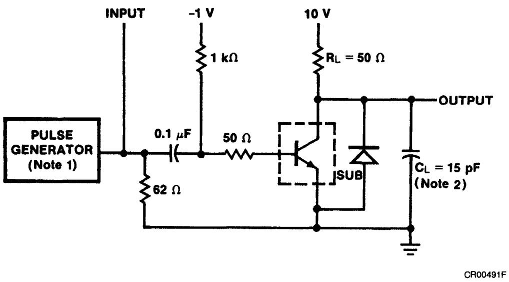


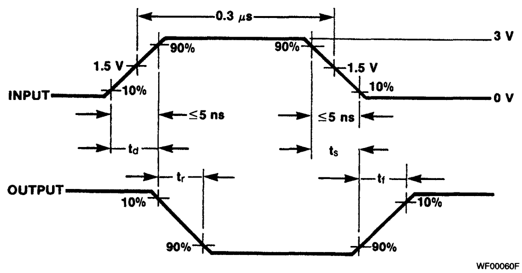


Notes

1. The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_O \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. All diodes are FD777.

Figure 13 Switching Times, Each Transistor (μA75450 Only)





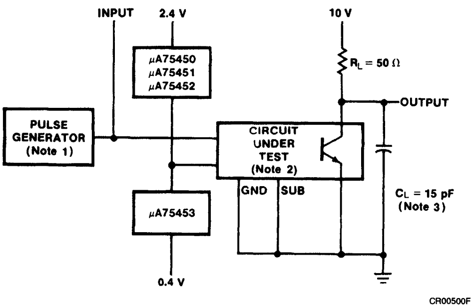
Notes

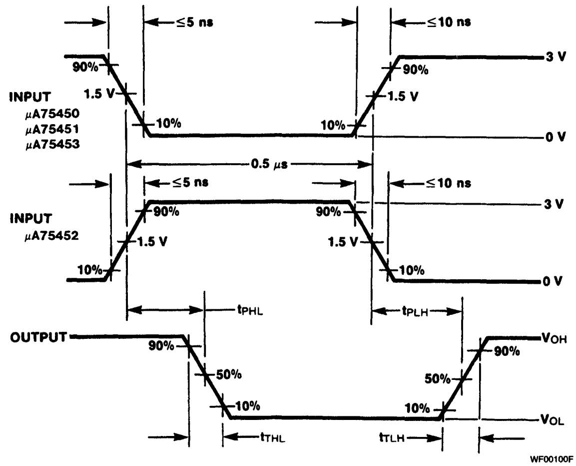
1. The pulse generator has the following characteristics: duty cycle ⩽ 1%, $Z_O \approx 50\ \Omega$.
2. C_L includes probe and jig capacitance.

Characteristics Measurement Information (Cont.)

Switching Characteristics

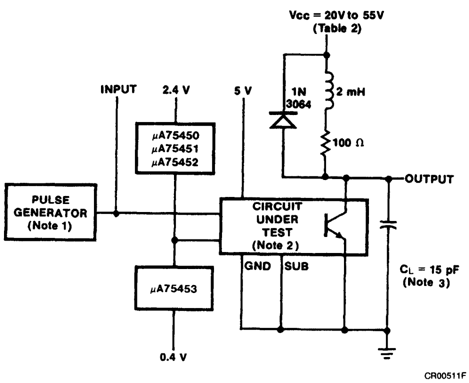
Figure 14 Switching Times of Complete Drivers

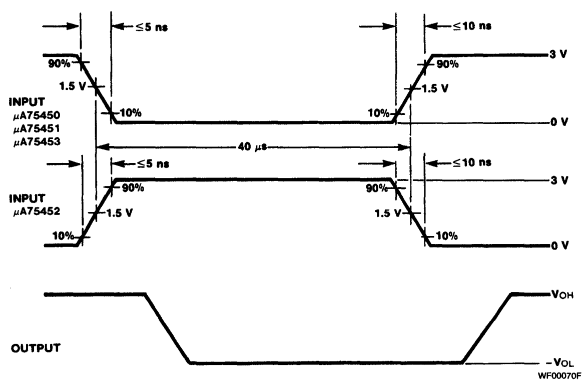




Notes
1. The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_O \approx 50\ \Omega$.
2. When testing μA75450, connect output Y to transistor base with a 500 Ω resistor to ground.
3. C_L includes probe and jig capacitance.

Figure 15 Latch-up Test of Complete Drivers





Notes
1. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O \approx 50\ \Omega$.
2. When testing μA75450, connect output Y to transistor base with a 500 Ω resistor from there to ground, and ground the substrate terminal.
3. C_L includes probe and jig capacitance.

μA75491 • μA75492 MOS To LED Segment And Digit Drivers

Linear Division Interface Products

Description
The μA75491 LED Quad Segment Digit Driver interfaces MOS signals to common cathode LED displays. High output current capability makes the device ideal for use in time multiplex systems using the segment address or digit scan method of driving LEDs to minimize the number of drivers required.

The μA75492 Hex LED/Lamp Driver converts MOS signals to high output currents for LED display digit select or lamp select. The high output current capability makes this device ideal for use in time multiplex systems using the segment address or digit scan method of driving LEDs to minimize the number of drivers required.

μA75491
- **50 mA Source Or Sink Capability**
- **Low Input Currents For MOS Compatibility**
- **Low Standby Power**
- **Four High Gain Darlington Circuits**

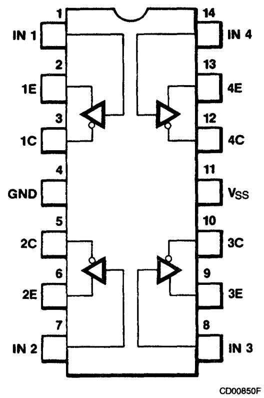
μA75492
- **250 mA Sink Capability**
- **MOS Compatible Inputs**
- **Low Standby Power**
- **Six High Gain Darlington Circuits**

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	1.04 W
Supply Voltage	10 V
Input Voltage[3]	−5.0 V to V_{SS}
Collector (Output) Voltage[4]	10 V
Collector (Output) to Input Voltage	10 V
Emitter to Ground Voltage	
($V_I \geq 5.0$ V) μA75491	10 V
Emitter to Input Voltage μA75491	5.0 V
Continuous Collector Current	
μA75491	50 mA
μA75492	250 mA
Collector Output Current	
(all collectors) μA75492	600 mA

Notes
1. $T_{J\ Max} = 150°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 8.3 mW/°C.
3. The input is the only device terminal which may be negative with respect to ground.
4. Voltage values are with respect to network ground terminal unless otherwise noted.

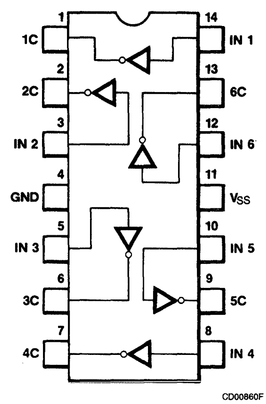
Connection Diagram
14-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA75491PC	9A	Molded DIP

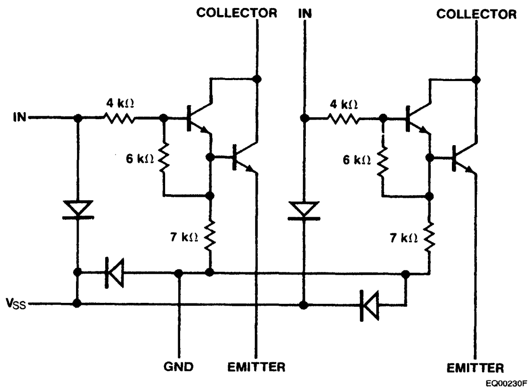
Connection Diagram
14-Lead DIP
(Top View)



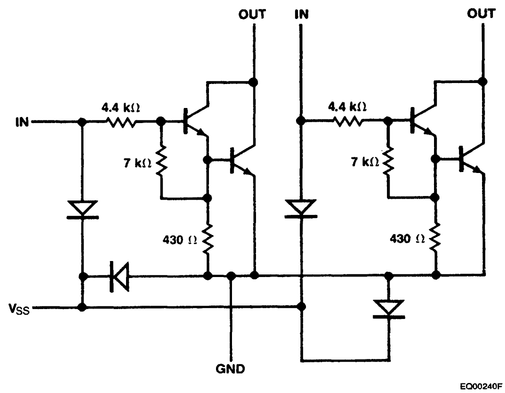
Order Information

Device Code	Package Code	Package Description
μA75492PC	9A	Molded DIP

Equivalent Circuit (1/2 of µA75491)



Equivalent Circuit (1/3 of µA75492)



Truth Tables

µA75491

INPUTS	OUTPUTS	
	1E-4E	1C-4C
L	L	H
H	H	L

µA75492

INPUTS	OUTPUTS 1C-6C
L	H
H	L

H = HIGH Level, L = LOW Level

µA75491

Electrical Characteristics V_{SS} = 10 V, T_A = 0°C to 70°C, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{CEL}	LOW Level Collector to Emitter Voltage	V_I = 8.5 V through 1.0 kΩ, I_{OL} = 50 mA, V_E = 5.0 V, T_A = 25°C			0.9	1.2	V
		V_I = 8.5 V through 1.0 kΩ, I_{OL} = 50 mA, V_E = 5.0 V			0.9	1.5	V
I_{CH}	Collector Current HIGH	V_{CH} = 10 V	V_E = 0 V, V_I = 0.7 V			100	µA
		V_{CH} = 10 V	V_E = 0 V, I_I = 40 µA			100	
I_I	Input Current at Maximum Input Voltage	V_I = 10 V	I_{OL} = 20 mA		2.0	3.3	mA
I_{ER}	Reverse Biased Emitter Current	I_C = 0 V, V_I = 0 V, V_E = 5.0 V				100	µA
I_{SS}	Supply Current					1.0	mA

μ**A75491** (Cont.)
Electrical Characteristics

AC Characteristics V_{SS} = 7.5 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Time	R_L = 200 Ω, V_{IH} = 4.5 V C_L = 15 pF, V_E = 0 V		20		ns
t_{PLH}				100		ns

μ**A75492**
Electrical Characteristics V_{SS} = 10 V, T_A = 0°C to 70°C, unless otherwise specified.

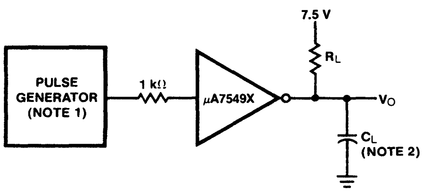
DC Characteristics

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
V_{OL}	Output Voltage LOW	V_I = 6.5 V through 1.0 kΩ, I_{OL} = 250 mA, T_A = 25°C			0.9	1.2	V
		V_I = 6.5 V through 1.0 kΩ, I_{OL} = 250 mA			0.9	1.5	
I_{OH}	Output Current HIGH	V_{OH} = 10 V	I_I = 40 μA			200	μA
		V_{OH} = 10 V	V_I = 0.5 V			200	
I_I	Input Current at Maximum Input Voltage	V_I = 10 V	I_{OL} = 20 mA		2.0	3.3	mA
I_{SS}	Supply Current					1.0	mA

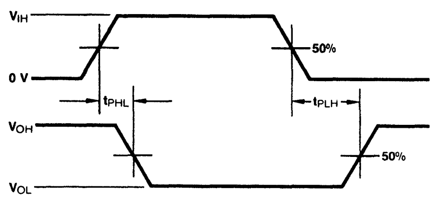
AC Characteristics V_{SS} = 7.5 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PHL}	Propagation Delay Time	R_L = 39 Ω, V_I = 7.5 V C_L = 15 pF		30		ns
t_{PLH}				300		ns

Test Circuit and Waveforms



CR01650F



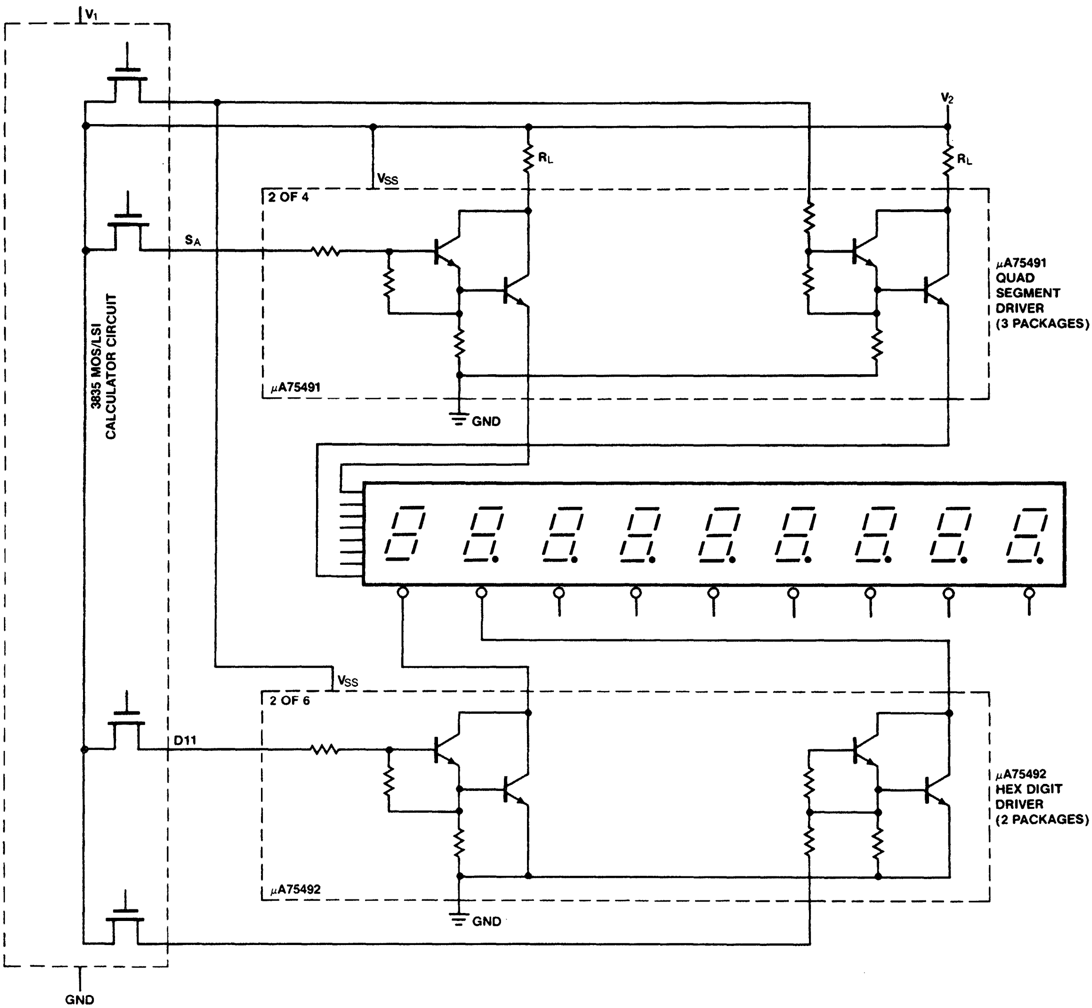
CR01670F

Notes
1. The pulse generator has the following characteristics: PRR = 100 kHz, t_w = 1.0 μs, Z_O = 50 Ω.
2. C_L includes probe and jig capacitance.

Typical Applications

Interfacing Between MOS Calculator Circuit and LED Multi-Digit Display

This example of time multiplexing the individual digits in a visible display minimizes display circuitry. Up to twelve digits of a 7-segment display plus decimal point may be displayed using only three μA75491 and two μA75492 drivers.



CR01661F

FAIRCHILD

A Schlumberger Company

μA9614 Dual Differential Line Driver

Linear Division Interface Products

Description

The μA9614 is a TTL compatible dual differential line driver. It is designed to drive transmission lines either differentially or single ended, back matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent leads. This allows multiplex operation (wired-OR) at the driving site in either the single ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Applications). The active pull-up is short circuit protected and offers a low output impedance to allow back matching. The two pairs of outputs are complementary, providing NAND and AND functions of the inputs and adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **Single 5.0 V Supply**
- **TTL Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Output Clamp Diodes For Termination Of Line Transients**
- **Complementary Outputs For NAND/AND Operation**
- **Uncommitted Collector Outputs For Wired-OR Application**
- **Extended Temperature Range**

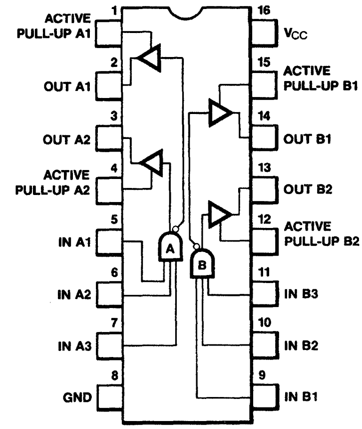
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA9614M)	−55°C to +125°C
Commercial (μA9614C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V_{CC} Lead Potential to Ground Lead	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collectors)	−0.5 V to +12 V

Note

1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



CD00301F

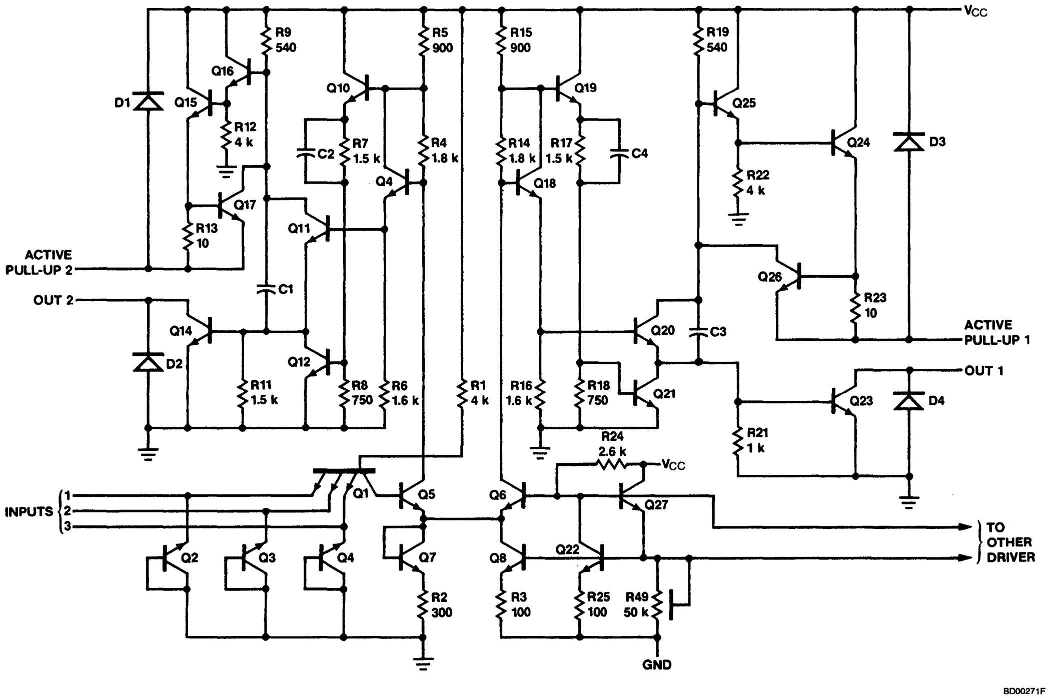
Order Information

Device Code	Package Code	Package Description
μA9614DM	6B	Ceramic DIP
μA9614DC	6B	Ceramic DIP
μA9614PC	9B	Molded DIP

Truth Table

INPUTS			OUTPUTS	
3	2	1	1	2
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

Equivalent Circuit (1/2 of circuit)



Note
All resistor values in ohms.

µA9614
Electrical Characteristics V_{CC} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified.

Symbol	Characteristic	Condition	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
V_{OL}	Output Voltage LOW	I_{OL} = 40 mA V_{CC} = 4.5 V		400		200	400		400	mV
V_{OH1}	Output Voltage HIGH	I_{OH} = −10 mA, V_{CC} = 4.5 V	2.4		2.4	3.2		2.4		V
V_{OH2}		I_{OH} = −20 mA, V_{CC} = 4.5 V	2.0		2.0	2.6		2.0		V
I_{OS}	Output Short Circuit Current	V_O = 0 V V_{CC} = 5.5 V			−40	−90	−120			mA
I_{CEX}	Output Leakage Current	V_{CEX} = 12.0 V V_{CC} = 5.5 V				10	100		200	µA
I_{IL}	Input Current LOW	V_I = 0.4 V V_{CC} = 5.5 V		−1.60		−1.10	−1.60		−1.60	mA
I_{IH}	Input Current HIGH	V_I = 4.5 V V_{CC} = 5.5 V				35	60		100	µA
V_{IL}	Input Voltage LOW	V_{CC} = 5.5 V		0.8		1.3	0.8		0.8	V
V_{IH}	Input Voltage HIGH	V_{CC} = 4.5 V	2.0		2.0	1.5		2.0		V
V_{OC}	Clamp Output Voltage LOW	I_{OC} = −40 mA V_{CC} = 5.5 V				−0.8	−1.5			V
I_{CC}	Supply Current	Inputs = 0 V V_{CC} = 5.5 V				34	50			mA
I_{Max}	Supply Current	Inputs = 0 V V_{Max} = 7.0 V				46	65			mA
t_{PLH}	Turn-Off Time	C_L = 30 pF V_{CC} = 5.0 V (See AC Circuit) V_M = 1.5 V				14	20			ns
t_{PHL}	Turn-On Time					18	20			ns
V_{IC}	Input Clamp Diode Voltage	V_{CC} = 4.5 V I_{IC} = −12 mA				−1.0	−1.5			V

μA9614C

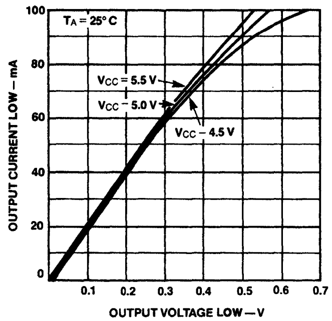
Electrical Characteristics V_{CC} = 5.0 V ± 5%, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Characteristic	Condition	0°C Min	0°C Max	25°C Min	25°C Typ	25°C Max	70°C Min	70°C Max	Unit
V_{OL}	Output Voltage LOW	I_{OL} = 40 mA V_{CC} = 4.75 V		450		200	450		450	mV
V_{OH1}	Output Voltage HIGH	I_{OH} = −10 mA, V_{CC} = 4.75 V	2.4		2.4	3.2		2.4		V
V_{OH2}		I_{OH} = −40 mA, V_{CC} = 4.75 V	2.0		2.0	2.6		2.0		V
I_{OS}	Output Short Circuit Current	V_O = 0 V V_{CC} = 5.25 V			−40	−90	−120			mA
I_{CEX}	Output Leakage Current	V_{CEX} = 5.25 V V_{CC} = 5.25 V				10	100		200	μA
I_{IL}	Input Current LOW	V_I = 0.45 V V_{CC} = 5.25 V		−1.60		−1.10	−1.60		−1.60	mA
I_{IH}	Input Current HIGH	V_I = 4.5 V V_{CC} = 5.25 V				35	60		100	μA
V_{IL}	Input Voltage LOW	V_{CC} = 5.25 V		0.8		1.3	0.8		0.8	V
V_{IH}	Input Voltage HIGH	V_{CC} = 4.75 V	2.0		2.0	1.5		2.0		V
V_{OC}	Clamp Output Voltage LOW	I_{OC} = −40 mA V_{CC} = 5.25 V				−0.8	−1.5			V
I_{CC}	Supply Current	Inputs = 0 V V_{CC} = 5.25 V				33	50			mA
I_{Max}	Supply Current	Inputs = 0 V V_{Max} = 7.0 V				46	70			mA
t_{PLH}	Turn-Off Time	C_L = 30 pF V_{CC} = 5.0 V				14	30			ns
t_{PHL}	Turn-On Time	(See AC Circuit) V_M = 1.5 V				18	30			ns
V_{IC}	Input Clamp Diode Voltage	V_{CC} = 4.75 V I_{IC} = −12 mA				−1.0	−1.5			V

9

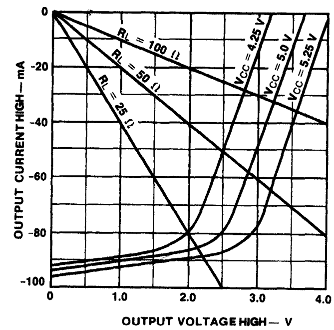
Typical Performance Curves

Active Pull-Down Output Current LOW vs Output Voltage LOW



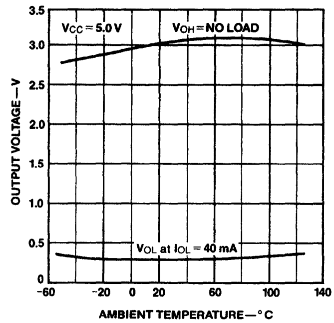
PC02242F

Active Pull-Up Output Current HIGH vs Output Voltage HIGH



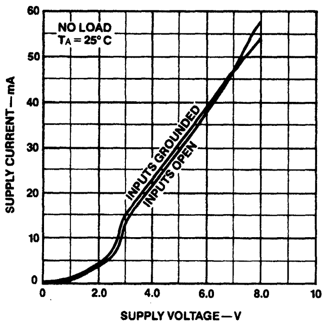
PC02252F

Logic Levels vs Ambient Temperature



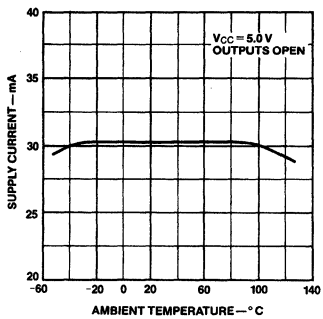
PC02262F

Supply Current vs Supply Voltage



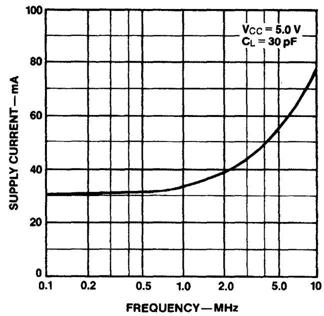
PC02271F

Supply Current vs Temperature



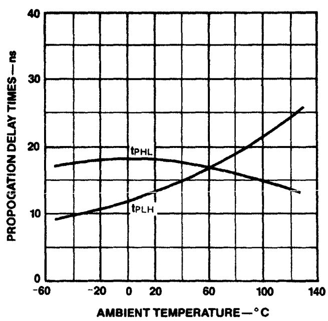
PC02281F

Supply Current vs Operating Frequency



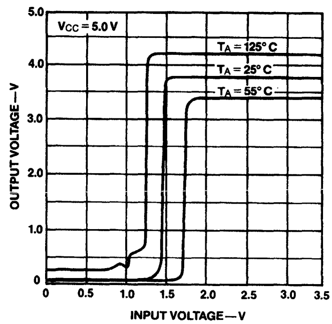
PC02291F

Propagation Delay Time vs Temperature



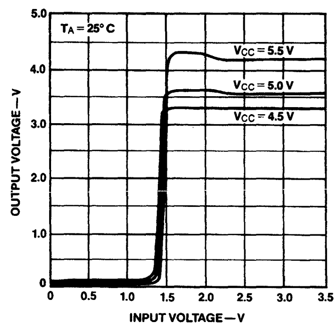
PC02301F

Transfer Characteristics vs Temperature



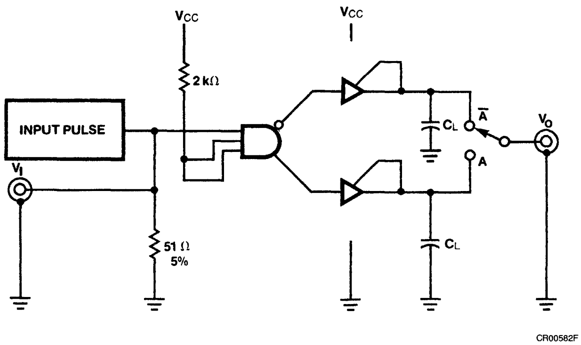
PC02312F

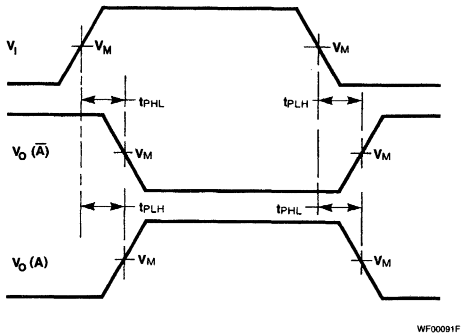
Transfer Characteristics vs Supply Voltage



PC02322F

AC Test Circuit and Waveforms

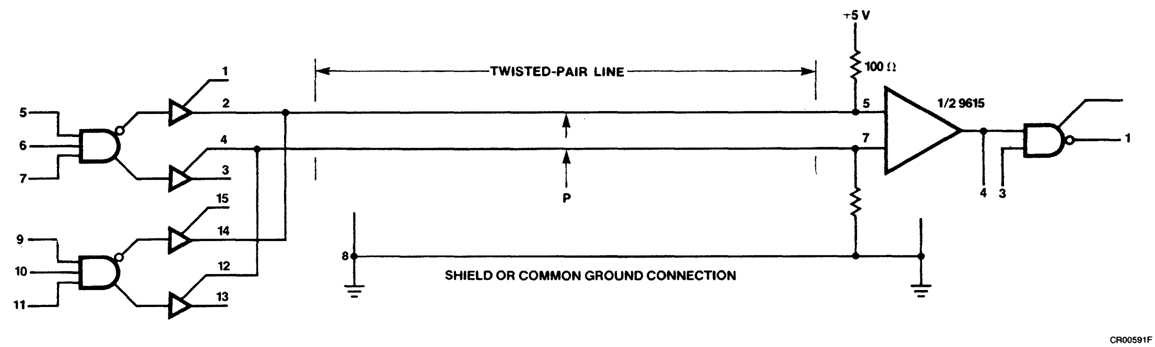




Input Pulse
Frequency = 500 kHz
Amplitude = 3.0 ± 0.1 V
Pulse Width = 110 ± 10 ns
$t_r = t_f \leqslant 5.0$ ns

Typical Applications

Differential Mode Expansion Multiplex Operation

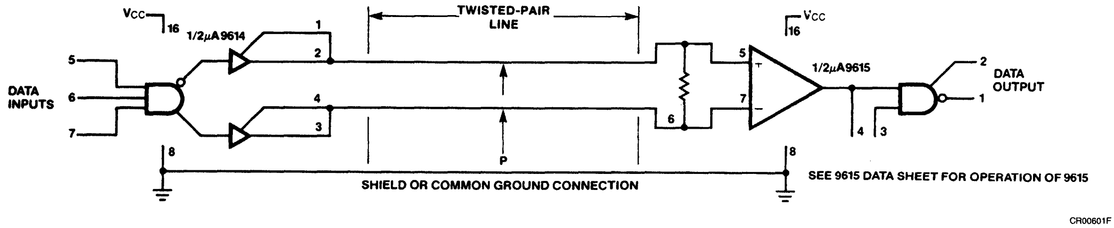


Only one driver is enabled at one time

Expand by tying NAND active pull-down outputs together and by tying AND active pull-up outputs together. The drivers can be inhibited by taking one input to ground.

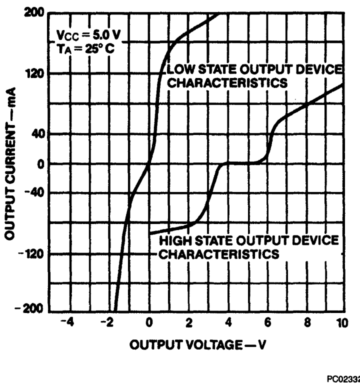
Typical Applications (Cont.)

Simplex — Differential Operation



See μA9615 data sheet for operation of μA9615

Typical Reflection Diagram



See μA9621 data sheet for usage of reflection diagram

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A Schlumberger Company

μA9615 Dual Differential Line Receiver

Linear Division Interface Products

Description

The μA9615 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the extended and industrial temperature ranges using a single 5.0 V supply. It can receive differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent lead to allow either wired-OR or active pull-up TTL output configuration.

- **TTL Compatible Output**
- **High Common Mode Voltage Range**
- **Choice Of An Uncommitted Collector Or Active Pull-Up**
- **Strobe**
- **Extended Temperature Range**
- **Single 5.0 V Supply Voltages**
- **Frequency Response Control**
- **130 Ω Terminating Resistor**

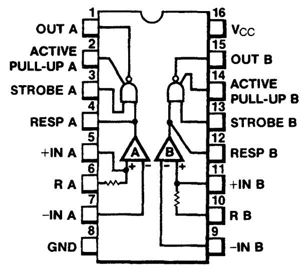
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA9615M)	-55°C to +125°C
Commercial (μA9615C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V_{CC} Lead Potential to Ground Lead	-0.5 V to +7.0 V
Input Voltage Referred to Ground	±20 V
Voltage Applied to Outputs for High Output State without Active Pull-up	-0.5 V to +13.2 V
Voltage Applied to Strobe	-0.5 V to +5.5 V

Note

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA9615DM	6B	Ceramic DIP
μA9615DC	6B	Ceramic DIP
μA9615PC	9B	Molded DIP

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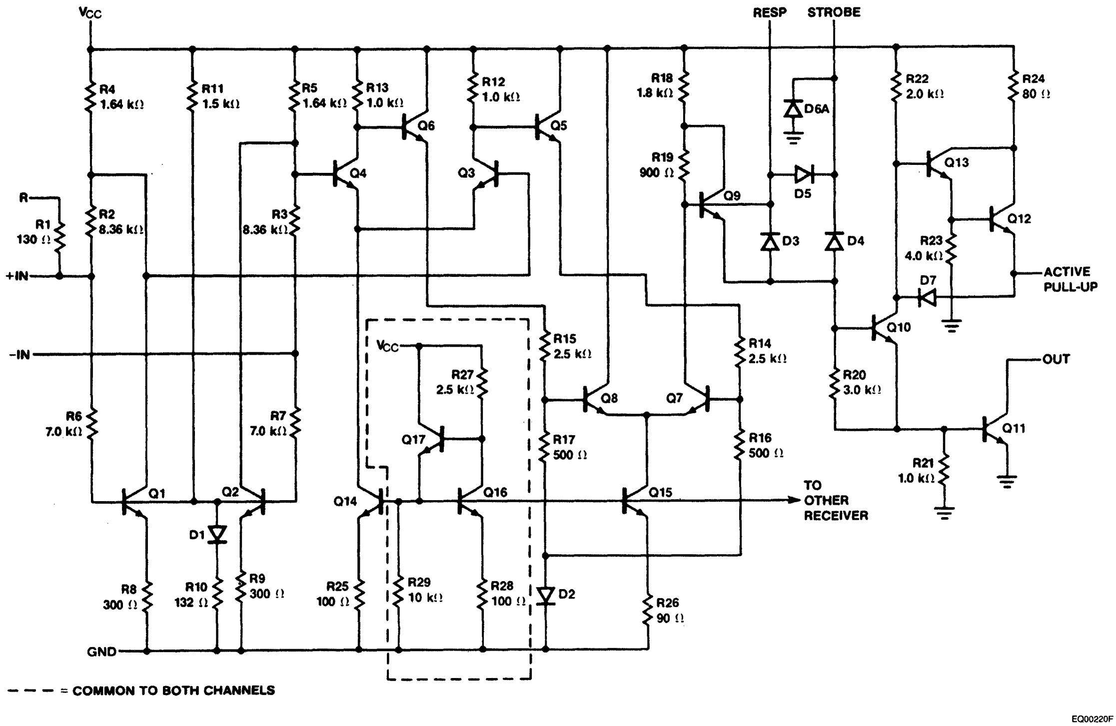
Equivalent Circuit (1/2 of Circuit)



μA9615
Electrical Characteristics V_{CC} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified.

Symbol	Characteristic	Condition[1]	T = −55°C Min	T = −55°C Max	T = 25°C Min	T = 25°C Typ	T = 25°C Max	T = +125°C Min	T = +125°C Max	Unit
V_{OL}	Output Voltage LOW	V_{CC} = 4.5 V, V_O = (Note 2), I_{OL} = 15.0 mA, V_{DIFF} = 0.5 V		0.40		0.18	0.40		0.40	V
V_{OH}	Output Voltage HIGH	V_{CC} = 4.5 V, V_O = (Note 2), I_{OH} = −5.0 mA, V_{DIFF} = −0.5 V	2.2		2.4	3.2		2.4		V
I_{CEX}	Output Leakage Current	V_{CC} = 4.5 V, V_{CEX} = 12 V, V_{DIFF} = V_{CC}					100		200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.5 V, V_{OS} = 0 V[2], V_{DIFF} = −0.5 V			−15	−39	−80			mA
I_I	Input Current	V_{CC} = 5.5 V, V_I = 0.4 V, Other input = 5.5 V		−0.9		−0.49	−0.7		−0.7	mA
$I_{I(ST)}$	Strobe Input Current	V_{CC} = 5.5 V, V_I = 0.4 V, V_{DIFF} = 0.5 V				−1.15	−2.4			mA
$I_{I(R-C)}$	Response Control Input Current	V_{CC} = 5.5 V, $V_{I(R-C)}$ = 0.4 V, V_{DIFF} = 0.5 V			−1.2	−3.4				mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V, V_{DIFF} = 1.0 V	−15	+15	−15	±17.5	+15	−15	+15	V
$I_{R(ST)}$	Strobe Input Leakage Current	V_{CC} = 4.5 V, V_R = 4.5 V, V_{DIFF} = −0.5 V					2.0		5.0	μA
R_I	Input Resistance	V_{CC} = 5.0 V, $V_{I(R)}$ = 1.0 V, +Input = GND			77	130	167			Ω
V_{TH}	Differential Input Threshold Voltage[3]	V_{CC} = 5.0 V ±10%, V_{CM} = 0 V	−500	+500	−500	+80	+500	−500	+500	mV
		V_{CC} = 5.0 V ±10%, −15 V ≤ V_{CM} ≤ +15 V	−1.0	+1.0	−1.0		+1.0	−1.0	+1.0	V
I_{CC}	Supply Current	V_{CC} = 5.5 V, −Inputs = 0 V, +Inputs = 0.5 V				28.7	50			mA
t_{PLH}	Turn-Off Time	V_{CC} = 5.0 V, R_L = 3.9 kΩ, C_L = 30 pF, *Figure 1*				30	50			ns

µA9615 (Cont.)
Electrical Characteristics V_{CC} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified.

Symbol	Characteristic	Condition[1]	T = −55°C Min	T = −55°C Max	T = 25°C Min	T = 25°C Typ	T = 25°C Max	T = +125°C Min	T = +125°C Max	Unit
t_{PHL}	Turn-On Time	V_{CC} = 5.0 V, R_L = 390 Ω, C_L = 30 pF, *Figure 1*				30	50			ns

µA9615C
Electrical Characteristics V_{CC} = 5.0 V ± 5%, T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Characteristic	Condition[1]	T = 0°C Min	T = 0°C Max	T = 25°C Min	T = 25°C Typ	T = 25°C Max	T = 70°C Min	T = 70°C Max	Unit
V_{OL}	Output Voltage LOW	V_{CC} = 4.75 V, V_O = (Note 2), I_{OL} = 15.0 mA, V_{DIFF} = 0.5 V		0.45		0.25	0.45		0.45	V
V_{OH}	Output Voltage HIGH	V_{CC} = 4.75 V, V_O = (Note 2), I_{OH} = −5.0 mA, V_{DIFF} = −0.5 V	2.4		2.4	3.3		2.4		V
I_{CEX}	Output Leakage Current	V_{CC} = 4.75 V, V_{CEX} = 5.25 V, V_{DIFF} = V_{CC}					100		200	µA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.25 V, V_{OS} = 0 V[2], V_{DIFF} = −0.5 V			−14		−100			mA
I_I	Input Current	V_{CC} = 5.25 V, V_I = 0.45 V, Other Input = 5.25 V		−0.9		−0.49	−0.7		−0.7	mA
$I_{I(ST)}$	Strobe Input Current	V_{CC} = 5.25 V, V_I = 0.45 V, V_{DIFF} = 0.5 V				−1.15	−2.4			mA
$I_{I(R-C)}$	Response Control Input Current	V_{CC} = 5.25 V, $V_{I(R-C)}$ = 0.4 V, V_{DIFF} = 0.5 V			−1.2	−3.4				mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V, V_{DIFF} = 1.0 V	−15	+15	−15	±17.5	+15	−15	+15	V
$I_{R(ST)}$	Strobe Input Leakage Current	V_{CC} = 4.75 V, V_R = 4.5 V, V_{DIFF} = −0.5 V					5.0		10	µA

μA9615C (Cont.)
Electrical Characteristics V_{CC} = 5.0 V ±5%, T_A = °C to 70°C, unless otherwise specified.

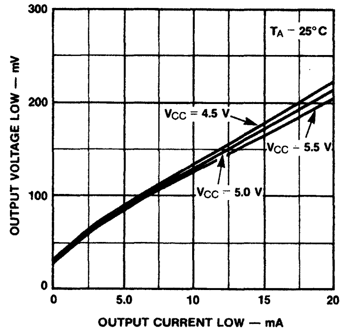
Symbol	Characteristic	Condition[1]	T = 0°C		T = 25°C			T = 70°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
R_I	Input Resistance	V_{CC} = 5.0 V, $V_{I(R)}$ = 1.0 V, +Input = GND			74	130	179			Ω
V_{TH}	Differential Input Threshold Voltage[3]	V_{CC} = 5.0 V ± 5%, V_{CM} = 0 V	−500	+500	−500	+80	+500	−500	+500	mV
		V_{CC} = 5.0 V ± 5%, −15 V ≤ V_{CM} ≤ +15 V	−1.0	+1.0	−1.0		+1.0	−1.0	+1.0	V
I_{CC}	Supply Current	V_{CC} = 5.25 V, +Inputs = 0.5 V, −Inputs = 0 V				28.7	50			mA
t_{PLH}	Turn-Off Time	V_{CC} = 5.0 V, R_L = 3.9 kΩ, C_L = 30 pF, *Figure 1*				30	75			ns
t_{PHL}	Turn-On Time	V_{CC} = 5.0 V, R_L = 390 Ω, C_L = 30 pF, *Figure 1*				30	75			ns

Notes
1. V_{DIFF} is a differential input voltage referred from +IN A to −IN A and from +IN B to −IN B.
2. Connect Output A to Active Pull-up A and Output B to Active Pull-up B.
3. See input output transfer characteristic graphs on following pages.

9

Typical Performance Curves for μA9615 and μA9615C

Output Voltage LOW vs Output Current LOW



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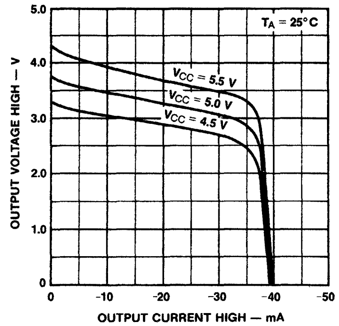
Output Voltage HIGH vs Output Current HIGH



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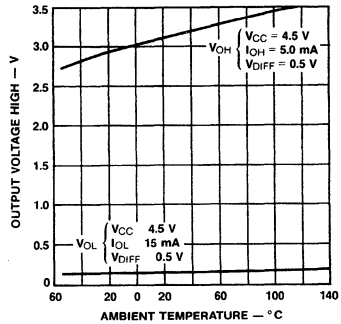
Output Voltage HIGH vs Ambient Temperature



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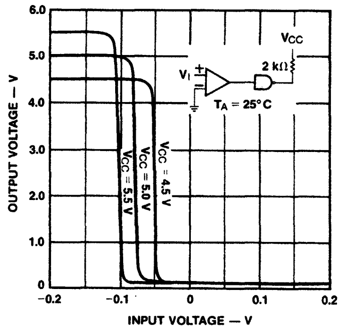
Input/Output Transfer Characteristics vs V_{CC}



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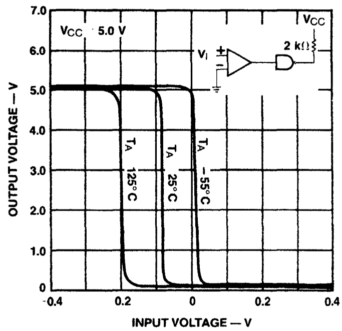
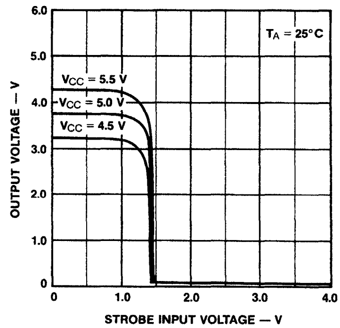
Input/Output Transfer Characteristics vs Temperature



PC06351F

Strobe Input/Output Transfer Characteristics vs V_{CC}



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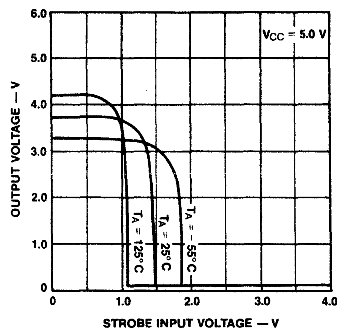
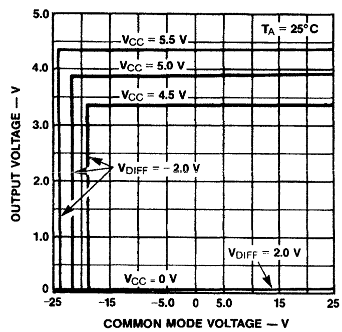
Strobe Input/Output Transfer Characteristic vs Ambient Temperature



PC06371F

Output Voltage vs Common Mode Voltage



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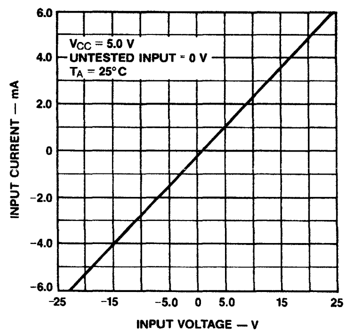
Input Current vs Input Voltage



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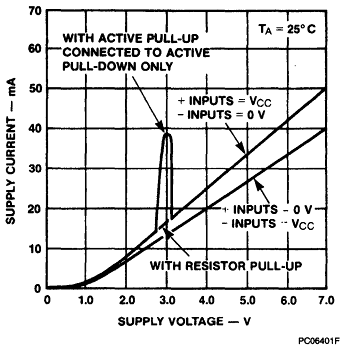
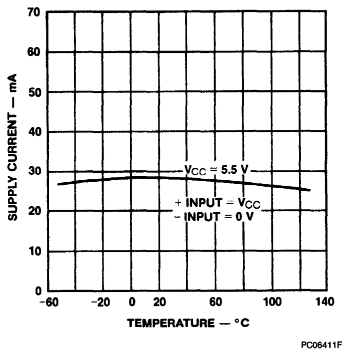
Typical Performance Curves for μA9615 and μA9615C (Cont.)

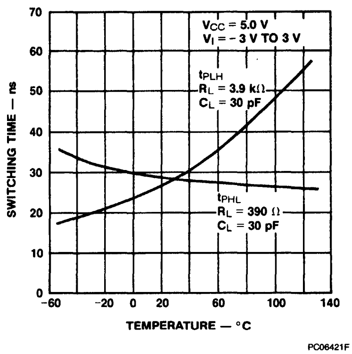
Supply Current vs Supply Voltage



Supply Current vs Ambient Temperature

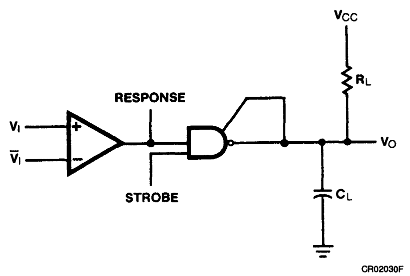


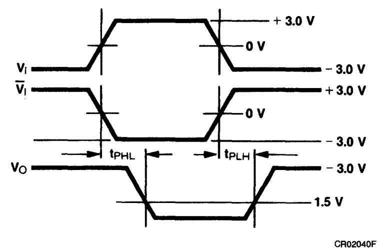
Switching Time vs Ambient Temperature



Switching Time Test Circuit and Waveforms (Note 1)

Figure 1

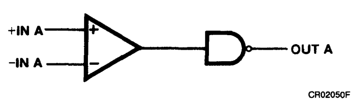


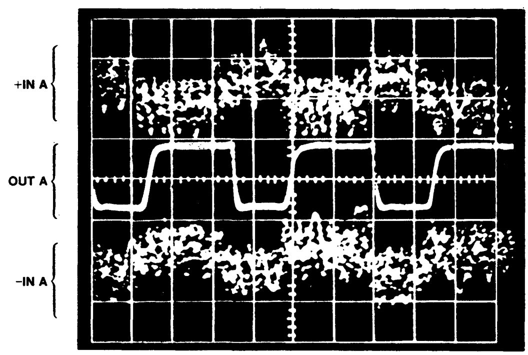


Note

1. Use V_I or $\overline{V_I}$, ground other input.

Figure 2





VERTICAL = 2.0 V/DIV. HORIZONTAL = 50 ns/DIV.

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Photograph of a μA9615 switching differential data in the presence of high common mode noise.

Notes

1. For t_{PHL} measurement $R_L = 390\ \Omega$
2. For t_{PHL} measurement $R_L = 3.9\ k\Omega$
3. For input pulse: Width = 100 ns ± 10 ns,
   t_r, t_f = ≤5.0 ns
   PRR = 500 kHz
4. C_L = 30 pF including probe and jig capacitance
5. Response control open, maximum scocket capacitance = 5.0 pF

Typical Applications

Figure 3 Standard Usage

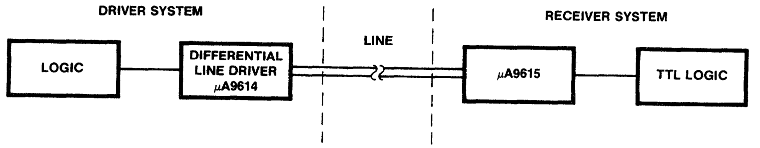
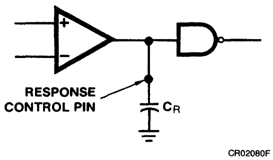


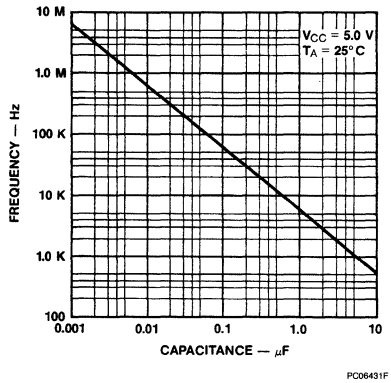
Figure 4 Frequency Response Control



Notes

$C_R > 0.01$ μF may cause slowing of rise and fall times of the output.
Due to the mechanism of induction of differential noise, the use of the response control is not normally needed.

Frequency Response as a Function of Capacitance



FAIRCHILD

A Schlumberger Company

μA96172 • μA96174 Quad Differential Line Drivers

Linear Division Interface Products

Description

The μA96172 and μA96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have three-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12 V to -7.0 V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The μA96172 features an active high and active low Enable, common to all four drivers. The μA96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered by Fairchild and are designed to provide optimum bus performance. The respective device types are μA96173/96175, μA96176, and μA96177/96178.

- **Meets EIA Standard RS-485 And RS-422A**
- **Monotonic Differential Output Switching**
- **Transmission Rate To 10 Mbs**
- **Three-State Outputs**
- **Designed For Multipoint Bus Transmission**
- **Common Mode Output Voltage Range: -7.0 V To +12 V**
- **Operates From Single +5.0 V Supply**
- **Thermal Shutdown Protection**
- **μA96172/96174 Are Lead And Function Compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively**

Function Table (Each Driver) μA96172

Input	Enables		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

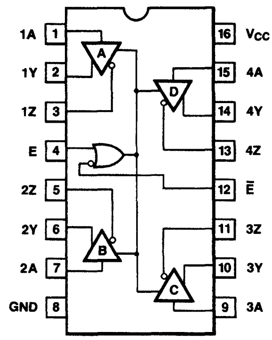
Function Table (Each Driver) μA96174

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Connection Diagram 16-Lead DIP (Top View)

μA96172



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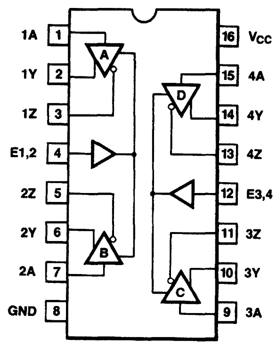
μA96174



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Order Information

Device Code	Package Code	Package Description
μA96172DC	7B	Ceramic DIP
μA96172PC	9B	Molded DIP
μA96174DC	7B	Ceramic DIP
μA96174PC	9B	Molded DIP

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Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Enable Input Voltage	5.5 V

Notes
1. $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{OC}	Common Mode Output Voltage	−7.0[1]		+12.0	V
I_{OH}	Output Current HIGH			−60	mA
I_{OL}	Output Current LOW			60	mA
T_A	Operating Temperature	0	25	70	°C

Note
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

µA96172, µA96174
Electrical Characteristics Over recommended temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20mA$		3.1		V
V_{OL}	Output Voltage LOW	$I_{OL} = 20mA$		0.8		V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 54\ \Omega$, Fig. 1a $R_L = 100\ \Omega$, Fig. 1b	1.5 2.0	2.0 2.3		V V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage[2]	$R_L = 54\ \Omega$ or $100\ \Omega$, Fig. 1b			±0.2	V

µA96172, µA96174 (Cont.)

Electrical Characteristics Over recommended temperature and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{OC}	Common Mode Output Voltage[3]					3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage[2]					±0.2	V
I_O	Output Current with Power off	$V_{CC} = 0$ V, $V_O = -7.0$ V to 12 V				±100	µA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0$ V to 12 V			±50	±200	µA
I_{IH}	Input Current HIGH	$V_I = 2.7$ V				20	µA
I_{IL}	Input Current LOW	$V_I = 0.5$ V				−100	µA
I_{OS}	Short Circuit Output Current	$V_O = -7.0$ V				−250	mA
		$V_O = 0$ V				−150	
		$V_O = V_{CC}$				150	
		$V_O = 12$ V				250	
I_{CC}	Supply Current (all drivers)	No load	Outputs Enabled		50	70	mA
			Outputs Disabled		50	60	

Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	$R_L = 60\ \Omega$, Fig. 2		15	25	ns
t_{TD}	Differential Output Transition Time			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\ \Omega$, Fig. 3		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\ \Omega$, Fig. 4		30	45	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\ \Omega$, Fig. 5		30	45	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\ \Omega$, Fig. 4		25	35	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\ \Omega$, Fig. 5		30	45	ns

Notes

1. All typical values are $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
3. In EIA Standard RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltages, V_{OS}.

Parameter Measurement Information

Figure 1a Differential Output Voltage with Varying Common Mode Voltage

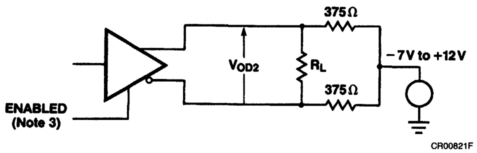


Figure 1b Differential and Common Mode Output Voltage

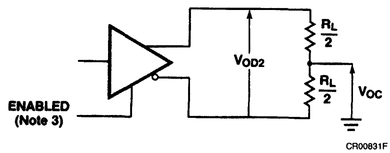


Figure 2 Differential Output Delay and Transition Times

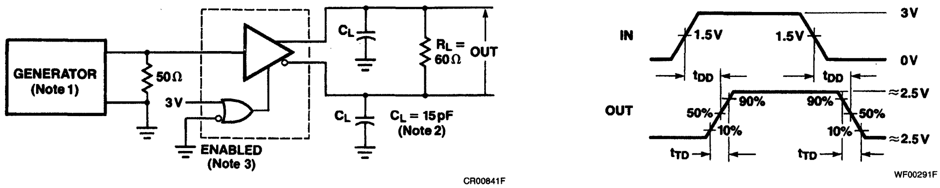


Figure 3 Propagation Delay Times

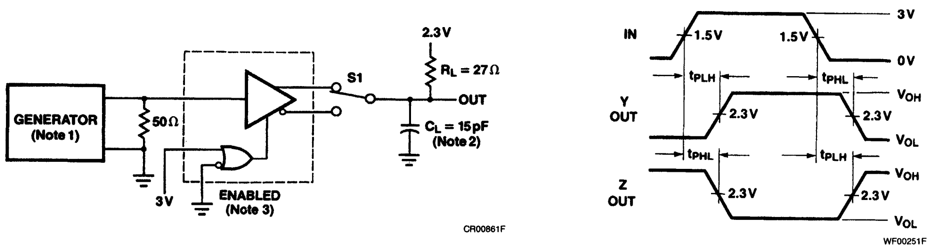
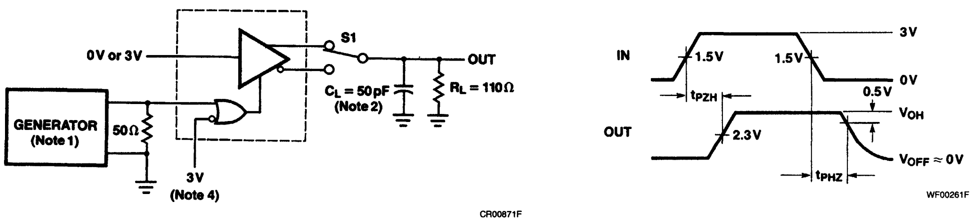
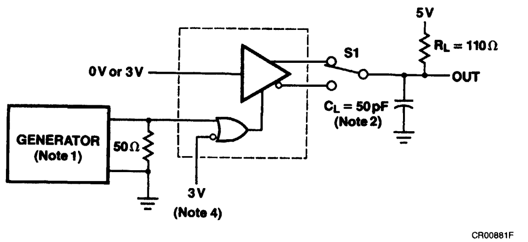


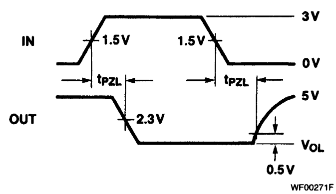
Figure 4 t_{PZH} and t_{PHZ}



Parameter Measurement Information (Cont.)

Figure 5 t_{PZL} and t_{PLZ}

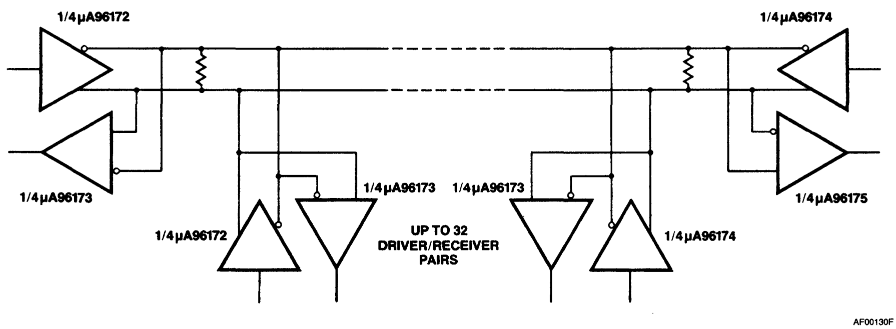




Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. μA96172 with active high and active low Enables is shown here. μA96174 has active high Enable only.
4. To test the active low Enable $\overline{E}$ of μA96172, ground E and apply an inverted waveform to $\overline{E}$. μA96174 has active high Enable only.

Typical Application



Note

The line length should be terminated at both ends in its characteristic impedance.

Stub lengths off the main line should be kept as short as possible.

9

FAIRCHILD

A Schlumberger Company

µA96173 • µA96175 Quad Differential Line Receivers

Linear Division Interface Products

Description

The µA96173 and µA96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have three-state outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12 V to +12 V. The receivers are therefore suitable for multipoint applications in noisy environments. The µA96173 features an active high and active low Enable, common to all four receivers. The µA96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered by Fairchild and are designed to provide optimum bus performance. The respective device types are µA96172/96174, µA96176 and µA96177/96178.

- **Meets EIA Standard RS-485, RS-422A, RS-423A**
- **Designed For Multipoint Bus Applications**
- **Three-State Outputs**
- **Common Mode Input Voltage Range: −12 V To +12 V**
- **Operates From Single +5.0 V Supply**
- **Input Sensitivity Of ±200 mV Over Common Mode Range**
- **Input Hysteresis Of 50 mV Typical**
- **High Input Impedance**
- **Fail-Safe Input/Output Features Drive Output HIGH When Input Is Open**
- **µA96173/96175 Are Lead And Function Compatible With SN75173/75175 Or The AM26LS32/MC3486 Respectively.**

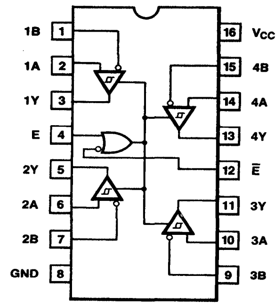
Function Table (Each Receiver) µA96173

Differential Inputs	Enables		Outputs
A − B	E	$\overline{E}$	V
$V_{ID} > 0.2$ V	H	X	H
	X	L	H
$-0.2\ V < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} < -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

Connection Diagram
16-Lead DIP
(Top View)

µA96173



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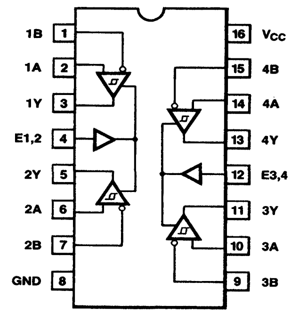
µA96175



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Order Information

Device Code	Package Code	Package Description
µA96173DC	7B	Ceramic DIP
µA96173PC	9B	Molded DIP
µA96175DC	7B	Ceramic DIP
µA96175PC	9B	Molded DIP

Function Table (Each Receiver) µA96175

Differential Inputs A − B	Enable	Output Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\ V < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage[3]	7.0 V
Input Voltage, A or B Inputs	±25 V
Differential Input Voltage	±25 V
Enable Input Voltage	7.0 V
Low Level Output Current	50 mA

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. All voltages are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CM}	Common Mode Input Voltage	−12[1]		+12	V
V_{ID}	Differential Input Voltage[2]	−12		+12	V
I_{OH}	Output Current HIGH			−400	µA
I_{OL}	Output Current LOW			16	mA
T_A	Operating Temperature	0	25	70	°C

Notes
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
2. Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

µA96173, µA96175
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit
V_{TH}	Differential-Input High Threshold Voltage	$V_O = 2.7$ V, $I_O = -0.4$ mA			0.2	V
V_{TL}	Differential-Input Low Threshold Voltage	$V_O = 0.5$ V, $I_O = 16$ mA	−0.2[2]			V
$V_{T+} - V_{T-}$	Hysteresis[3]	$V_{CM} = 0$ V		50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V

μA96173, μA96175 (Cont.)
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				-1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA				2.7	V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4$ V to 2.4 V				±20	μA
I_I	Line Input Current[4]	Other Input = 0 V	$V_I = 12$ V			1.0	mA
			$V_I = -7.0$ V			-0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7$ V				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4$ V				-100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current			-15		-85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5$ V to 2.5 V, $C_L = 15$ pF, Fig. 1		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, Fig. 2		15	22	ns
t_{PZL}	Output Enable Time to Low Level	$C_L = 15$ pF, Fig. 3		15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, Fig. 2		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5.0$ pF, Fig. 3		24	40	ns

Notes
1. All Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
3. Hysteresis is the difference between the positive-going input threshold voltage, V_T+, and the negative-going input threshold voltage, V_T-.
4. Refer to EIA standard RS-485 for exact conditions.

Parameter Measurement Information

Figure 1 t_{PLH}, t_{PHL} (Note 3)

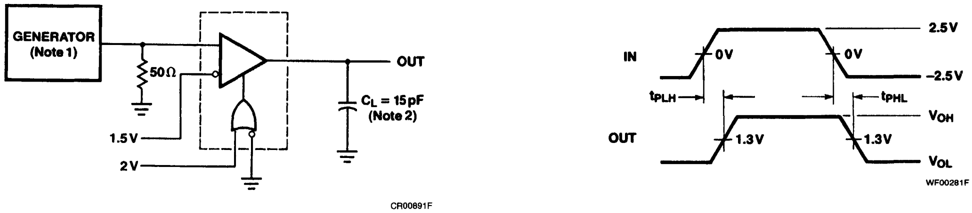


Figure 2 t_{PHZ}, t_{PZH} (Note 3)

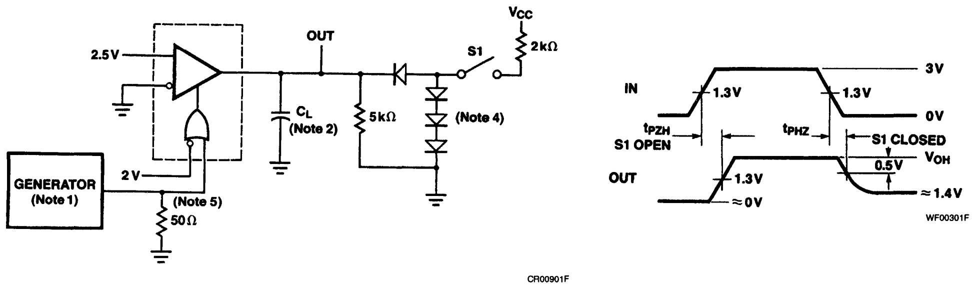
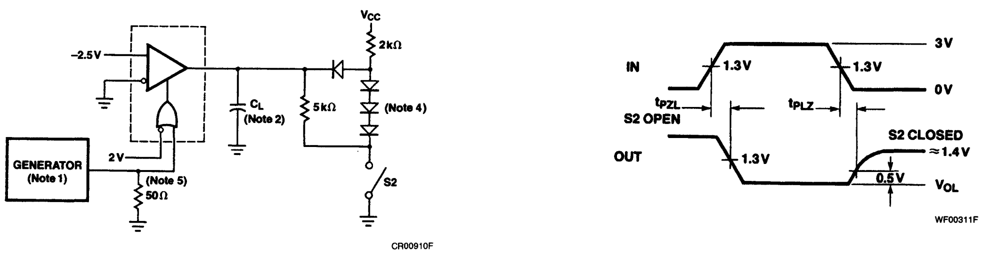


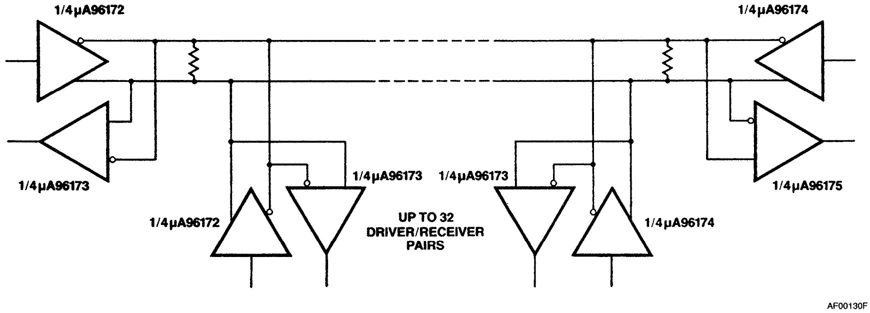
Figure 3 t_{PZL}, t_{PLZ} (Note 3)



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leqslant 6.0$ ns, $t_f \leqslant 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and jig capacitance.
3. μA96173 with active high and active low Enables is shown here. μA96175 has active high Enable only.
4. All diodes are 1N916 or equivalent.
5. To test the active low Enable $\overline{E}$ of μA96173, ground E and apply an inverted input waveform to $\overline{E}$. μA96175 has active high Enable only.

Typical Application



Note

The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FAIRCHILD

A Schlumberger Company

μA96176
Differential Bus Transceiver

Linear Division Interface Products

Description

The μA96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

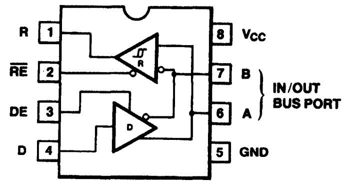
The μA96176 combines a three-state differential line driver and a differential input line receiver, both of which operate from a single 5.0 V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when $V_{CC} = 0$ V. These ports feature wide positive and negative common mode voltage ranges making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The μA96176 can be used in transmission line applications employing the μA96172 and the μA96174 quad differential line drivers and the μA96173 and μA96175 quad differential line receivers.

- **Bidirectional Transceiver**
- **Meets EIA Standard RS-422A And RS-485**
- **Designed For Multipoint Transmission**
- **Three-State Driver And Receiver Enables**
- **Individual Driver And Receiver Enables**
- **Wide Positive And Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability ±60mA Maximum**
- **Thermal Shutdown Protection**
- **Driver Positive And Negative Current-Limiting**
- **High Impedance Receiver Input**
- **Receiver Input Sensitivity Of ±200 mV**
- **Receiver Input Hysteresis Of 50 mV Typical**
- **Operates From Single 5.0 V Supply**
- **Low Power Requirements**

Connection Diagram
8-Lead DIP
(Top View)



CD00461F

Order Information

Device Code	Package Code	Package Description
μA96176RC	6T	Ceramic DIP
μA96176TC	9T	Molded DIP

Function Table (Driver)

Differential Inputs D	Enable DE	Outputs A	Outputs B
H	H	H	L
L	H	L	H
X	L	Z	Z

Function Table (Receiver)

Differential Inputs A-B	Enable $\overline{RE}$	Output R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

9

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
Supply Voltage[3]	7.0 V
Differential Input Voltage	±25 V
Enable Input Voltage	5.5 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic		Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_I or V_{CM}	Voltage at any Bus Terminal (Separately or Common Mode)		-7.0[1]		12	V
V_{ID}	Differential Input Voltage[2]				±12	V
I_{OH}	Output Current HIGH	Driver			-60	mA
		Receiver			-400	μA
I_{OL}	Output Current LOW	Driver			60	mA
		Receiver			16	
T_A	Operating Temperature		0	25	70	°C

Notes

1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
2. Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

μA96176

Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Driver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -20mA$			3.1		V
V_{OL}	Output Voltage LOW	$I_{OL} = 20mA$			0.85		V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\lvert V_{OD1} \rvert$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\lvert V_{OD2} \rvert$	Differential Output Voltage	$R_L = 100\ \Omega$, Fig. 1		2.0	2.25		V
		$R_L = 54\ \Omega$, Fig. 2		1.5	2.0		
$\triangle \lvert V_{OD} \rvert$	Change in Magnitude of Differential Output Voltage[2]					±0.2	V
V_{OC}	Common Mode Output Voltage[3]	$R_L = 54\ \Omega$ or $100\ \Omega$, Fig. 1				3.0	V
$\triangle \lvert V_{OC} \rvert$	Change in Magnitude of Common Mode Output Voltage[2]					±0.2	V
I_O	Output Current[4] (Includes Receiver I_I)	Output Disabled	$V_O = 12$ V			1.0	mA
			$V_O = -7.0$			−0.8	
I_{IH}	Input Current HIGH	$V_I = 2.4$ V				20	μA
I_{IL}	Input Current LOW	$V_I = 0.4$ V				−100	μA
I_{OS}	Short Circuit Output Current	$V_O = -7.0$ V				−250	mA
		$V_O = 0$ V				−150	
		$V_O = V_{CC}$				150	
		$V_O = 12$ V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

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μA96176 (Cont.)

Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Drive Switching Characteristics $V_{CC} = 5$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	$R_L = 60\ \Omega$, Fig. 4		15	25	ns
t_{TD}	Differential Output Transition Time	$R_L = 60\ \Omega$, Fig. 4		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\ \Omega$, Fig. 5		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 27\ \Omega$, Fig. 5		12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\ \Omega$, Fig. 6		25	35	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\ \Omega$, Fig. 7		25	35	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\ \Omega$, Fig. 6		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\ \Omega$, Fig. 7		29	35	ns

Receiver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7$ V, $I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage	$V_O = 0.5$ V, $I_O = 8.0$ mA		−0.2[5]			V
$V_{T+} - V_{T-}$	Hysteresis[6]	$V_{CM} = 0$ V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV, $I_{OH} = -400\ \mu A$, Fig. 3		2.7			V
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV, Fig. 3	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High Impedance State Output	$V_O = 0.4$ V to 2.4 V				±20	μA
I_I	Line Input Current[7]	Other Input = 0 V	$V_I = 12$ V			1.0	mA
			$V_I = -7.0$ V			0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7$ V				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4$ V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current			−15		−85	mA
I_{CC}	Supply Current (total package)	No Load	Outputs Enabled			40	mA
			Outputs Disabled				

Receiver Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$V_{ID} =$ 0 V to 3.0 V $C_L = 15$ pF, Fig. 8		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	$C_L = 15$ pF, Fig. 9		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	$C_L = 5.0$ pF, Fig. 9		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Notes

1. All typical values are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
2. $\triangle|V_{OD}|$ and $\triangle|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
3. In EIA Standard RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
4. This applies for both power-on and power-off. Refer to EIA Standard RS-485 for exact conditions.
5. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
6. Hysteresis is the difference between the positive-going input threshold voltage, V_T+, and the negative-going input threshold voltage, V_T-.
7. This applies for both power-on and power-off. Refer to EIA Standard RS-485 for exact conditions.

9

Parameter Measurement Information

Figure 1 Driver V_{OD} and V_{OC}

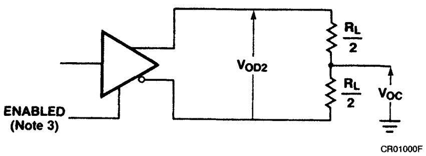


Figure 2 Driver V_{OD} with Varying Common Mode Voltage

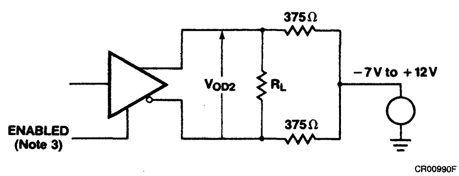
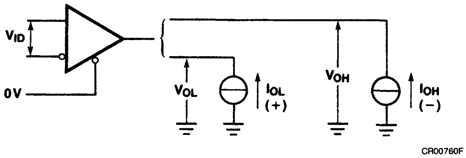


Figure 3 Receiver V_{OH} and V_{OL}



Parameter Measurement Information (Cont.)

Figure 4 Driver Differential Output Delay and Transition Times

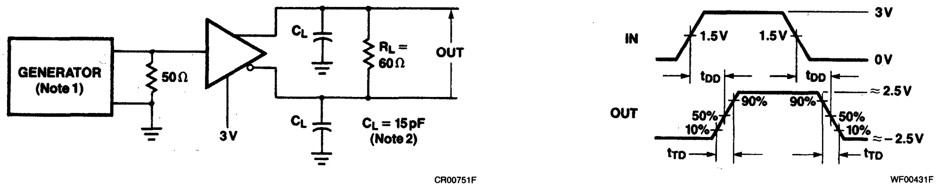


Figure 5 Driver Propagation Times

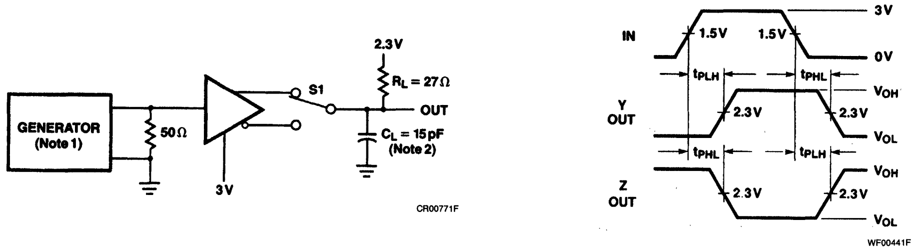


Figure 6 Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

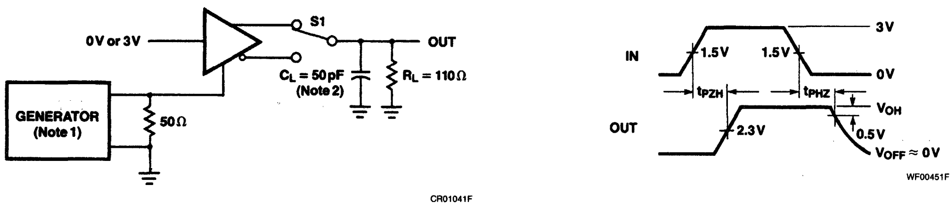
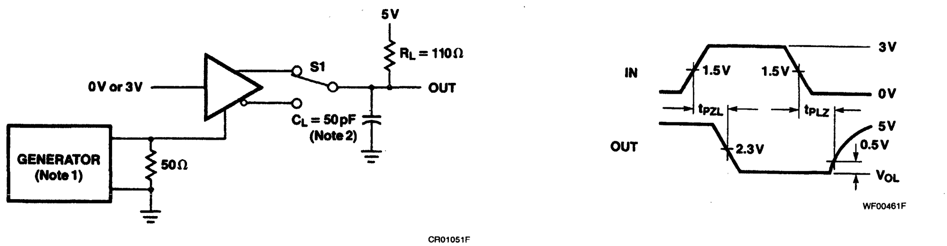


Figure 7 Driver Enable and Disable Times (t_{PZL}, t_{PLZ})



Parameter Measurement Information (Cont.)

Figure 8 Receiver Propagation Delay Times

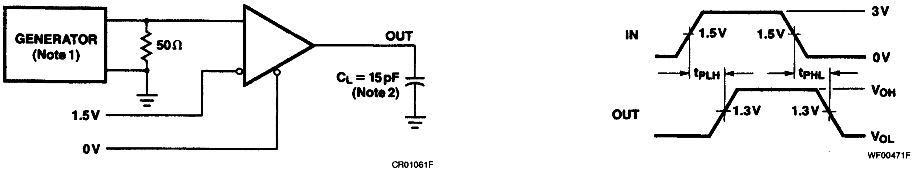
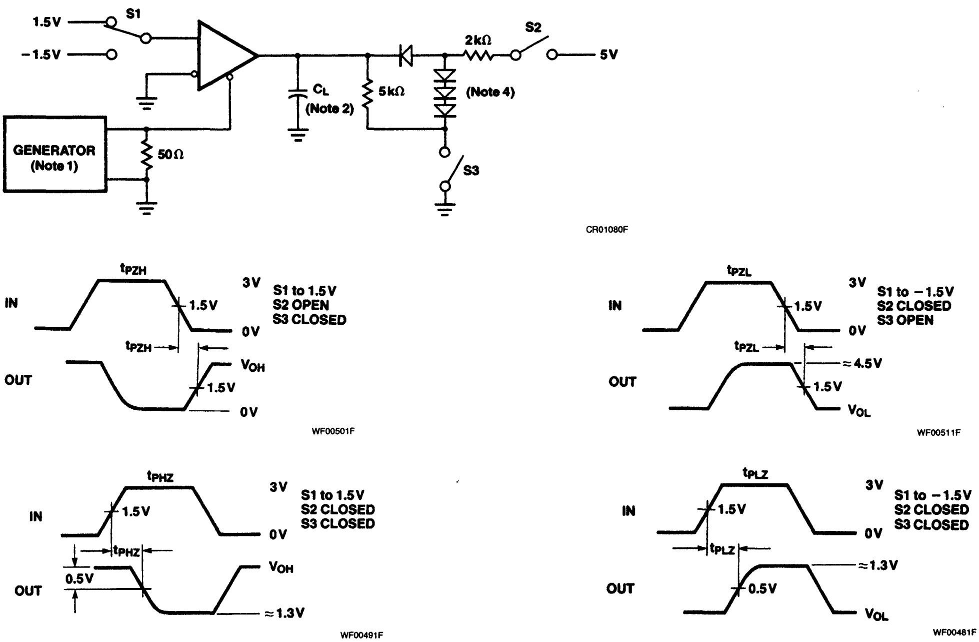


Figure 9 Receiver Enable and Disable Times

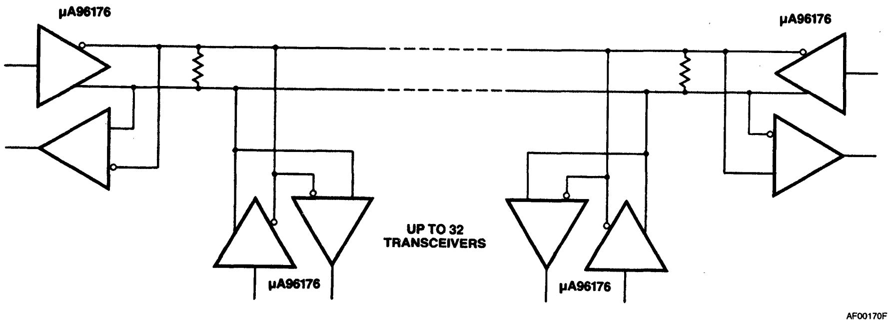


Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and stray capacitance.
3. μA96176 Driver enable is Active-High
4. All diodes are 1N916 or equivalent.

9

Typical Application



Note
The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

μA96177 • μA96178 Differential Bus Repeaters

FAIRCHILD
A Schlumberger Company

Linear Division Interface Products

Description

The μA96177 and μA96178 Differential Bus Repeaters are monolithic integrated devices each designed for one-way data communications on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-485 and RS-422A. Each device is designed to improve the performance of the data communication over long bus lines. The μA96177 and μA96178 are identical except for the Enable inputs, which are complementary. The μA96177 is an active high Enable. The μA96178 is an active low Enable. These complementary Enables allow the devices to be used in pairs for bidirectional communication.

The μA96177 and μA96178 feature positive and negative current limiting and three-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12 V to +12 V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

The μA96177 and μA96178 are designed for optimum performance when used on transmission buses employing the μA96172 and μA96174 differential line drivers, μA96173 and μA96175 differential line receivers, or μA96176 differential bus transceiver.

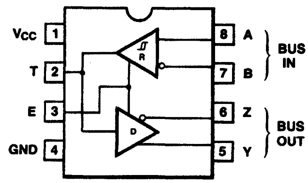
- **Meets EIA Standard RS-422A And RS-485**
- **Designed For Multipoint Transmission On Long Bus Lines In Noisy Environments**
- **Three-State Outputs**
- **Bus Voltage Range −7.0 V To 12 V**
- **Positive And Negative Current Limiting**
- **Driver Output Capability ±60 mA Max**
- **Driver Thermal Shutdown Protection**
- **Receiver Input High Impedance**
- **Receiver Input Sensitivity Of ±200 mV**
- **Receiver Input Hysteresis Of 50 mV Typical**
- **Operates From Single 5.0 V Supply**
- **Low Power Requirements**

Function Table μA96177

Differential Inputs A-B	Enable E	Outputs T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
$-0.2\ V < V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq -0.2$ V	H	L	L	H
X	L	Z	Z	Z

Connection Diagram 8-Lead DIP (Top View)

μA96177



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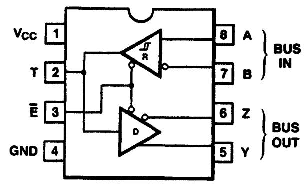
μA96178



CD00371F

Order Information

Device Code	Package Code	Package Description
μA96177RC	6T	Ceramic DIP
μA96177TC	9T	Molded DIP
μA96178RC	6T	Ceramic DIP
μA96178TC	9T	Molded DIP

Function Table μA96178

Differential Inputs A-B	Enable Ē	Outputs T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
$-0.2\ V < V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq -0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
Supply Voltage[3]	7.0 V
Input Voltage	5.5 V

Notes
1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.
3. All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

Symbol	Characteristic		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_I or V_{CM}	Voltage at any Bus Terminal (Separately or Common mode)		-7.0[1]		12	V
V_{ID}	Differential Input Voltage[2]				±12	V
I_{OH}	Output Current HIGH	Driver			-60	mA
		Receiver			-400	μA
I_{OL}	Output Current LOW	Driver			60	mA
		Receiver			16	
T_A	Operating Temperature		0	25	70	°C

Notes
1. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
2. Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

μA96177, μA96178
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Driver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 100\ \Omega$ Fig. 2		2.0	2.25		V
		$R_L = 54\ \Omega$ Fig. 1		1.5	2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage[2]	$R_L = 54\ \Omega$ or $100\ \Omega$, Fig.1				±0.2	V
V_{OC}	Common Mode Output Voltage[3]					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage[2]					±0.2	V
I_O	Output Current with Power off	$V_{CC} = 0$ V, $V_0 = -7.0$ V to 12 V				±100	μA
I_{OZ}	High Impedance State Output Current	$V_O = -7.0$ V to 12 V			±50	±200	μA
I_{IH}	Input Current HIGH	$V_I = 2.7$ V				20	μA
I_{IL}	Input Current LOW	$V_I = 0.5$ V				−100	μA
I_{OS}	Short Circuit Output Current	$V_O = -7.0$ V				−250	mA
		$V_O = 0$ V				−150	
		$V_O = V_{CC}$				150	
		$V_O = 12$ V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

μA96177, μA96178 (Cont.)
Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Drive Switching Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	$R_L = 60\ \Omega$, Fig. 4		15	25	ns
t_{TD}	Differential Output Transition Time	$R_L = 60\ \Omega$, Fig. 4		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\ \Omega$, Fig. 5		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$R_L = 27\ \Omega$, Fig. 5		12	20	ns
t_{PZH}	Output Enable Time to High Level	$R_L = 110\ \Omega$, Fig. 6		25	45	ns
t_{PZL}	Output Enable Time to Low Level	$R_L = 110\ \Omega$, Fig. 7		25	40	ns
t_{PHZ}	Output Disable Time from High Level	$R_L = 110\ \Omega$, Fig. 6		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	$R_L = 110\ \Omega$, Fig. 7		29	35	ns

Receiver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{TH}	Differential Input High Threshold Voltage	$V_O = 2.7$ V, $I_O = -0.4$ mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage	$V_O = 0.5$ V, $I_O = 8.0$ mA		−0.2[5]			V
$V_{T+} - V_{T-}$	Hysteresis[6]	$V_{CM} = 0$ V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$V_{ID} = 200$ mV, $I_{OH} = -400$ μA, Fig. 3		2.7			V
V_{OL}	Low Level Output Voltage	$V_{ID} = -200$ mV, Fig. 3	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 16$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4$ V				−360	μA
		$V_O = 2.4$ V				20	
I_I	Line Input Current[7]	Other Input = 0 V	$V_I = 12$ V			1.0	mA
			$V_I = -7.0$ V			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7$ V				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4$ V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current			−15		−85	mA
I_{CC}	Supply Current (total package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

µA96177, µA96178 (Cont.)

Electrical Characteristics Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified.

Receiver Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0 V to 3.0 V C_L = 15 pF, Fig. 8		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, Fig. 9		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, Fig. 9		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Notes

1. 1. All typical values are at V_{CC} = 5.0 V and T_A = 25°C.
2. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
3. In EIA Standard RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
4. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
5. Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-}.
6. Refer to EIA Standard RS-485 for exact conditions.

Parameter Measurement Information

Figure 1 Driver V_{OD2} and V_{OC}

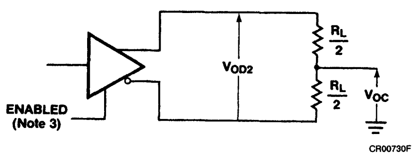


Figure 3 Receiver V_{OH} and V_{OL}

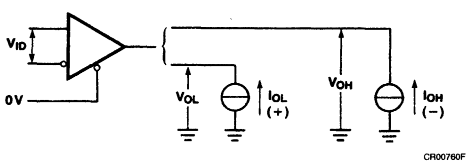
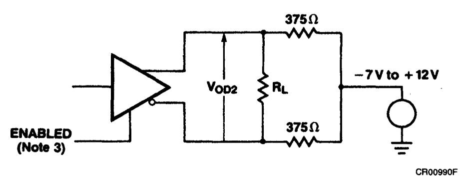


Figure 2 Driver V_{OD2} with Varying Common Mode Voltage



Parameter Measurement Information (Cont.)

Figure 4 Driver Differential Output Delay and Transition Times

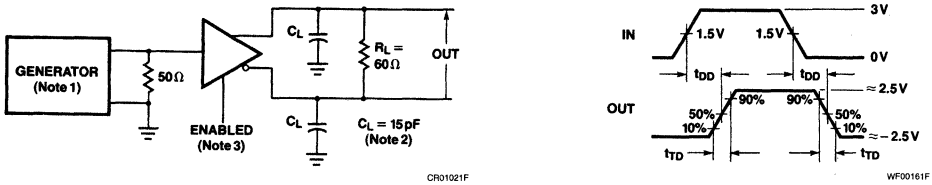


Figure 5 Drive Propagation Times

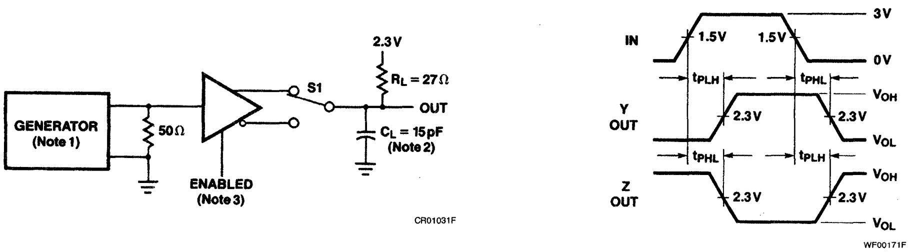


Figure 6 Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

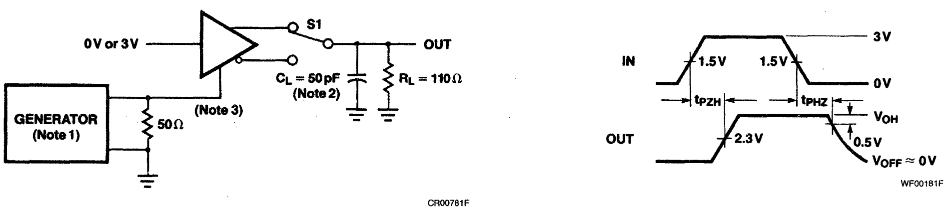
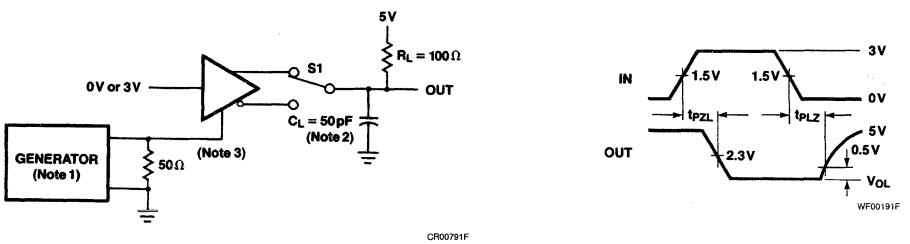


Figure 7 Driver Enable and Disable Times (t_{PZL}, t_{PLZ})



Parameter Measurement Information (Cont.)

Figure 8 Receiver Propagation Delay Times

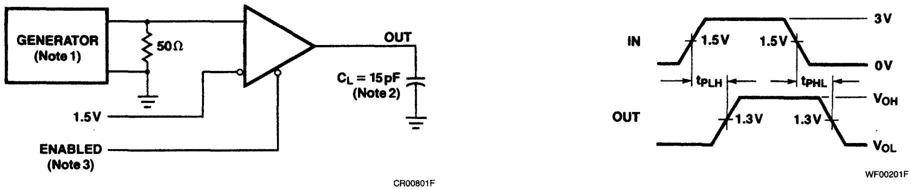
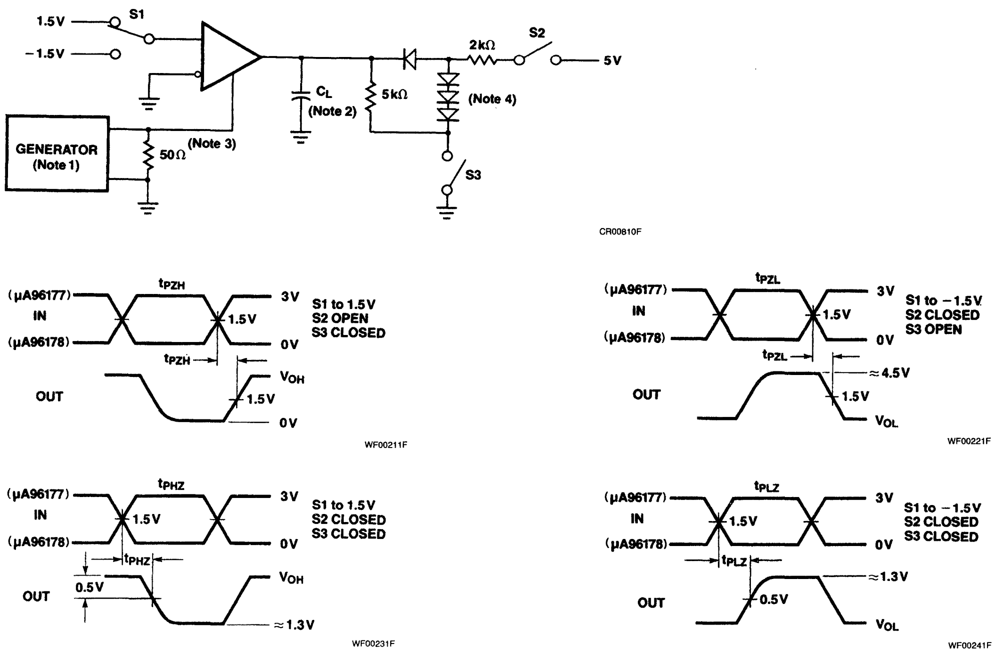


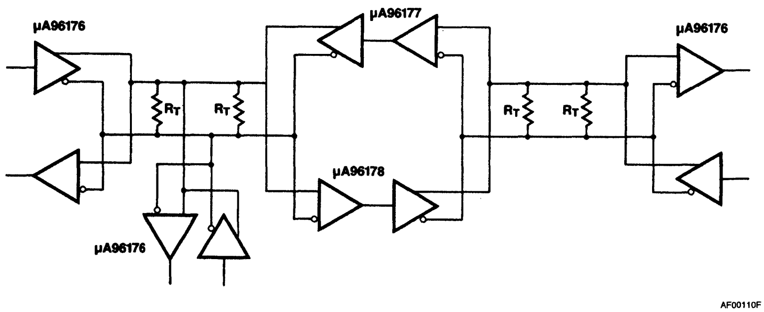
Figure 9 Receiver Enable and Disable Times



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle≈50%, $t_r \leqslant 6.0$ ns, $t_f \leqslant 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and stray capacitance.
3. μA96178 Enable is active low, μA96177 Enable is active high.
4. All diodes are 1N916 or equivalent.

Typical Application



Note
The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

μA9636A
RS-423 Dual Programmable Slew Rate Line Driver

FAIRCHILD
A Schlumberger Company

Linear Division Interface Products

Description

The μA9636A is a TTL/CMOS compatible, dual, single ended line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The μA9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current-limiting is provided in both output states. The μA9636A is designed for nominal power supplies of ±12 V.

Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

- **Programmable Slew Rate Limiting**
- **Meets EIA Standard RS-423**
- **Commercial Or Extended Temperature Range**
- **Output Short Circuit Protection**
- **TTL And CMOS Compatible Inputs**

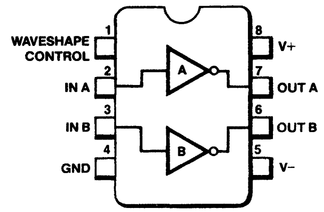
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA9636AM)	−55°C to +125°C
Commercial (μA9636AC)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
V+ Lead Potential to Ground Lead	V− to +15 V
V− Lead Potential to Ground Lead	+0.5 V to −15 V
V+ Lead Potential to V− Lead	0 V to +30 V
Output Potential to Ground Lead	±15 V
Output Source Current	−150 mA
Output Sink Current	150 mA

Notes

1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, and the 8L-Molded DIP at 7.5 mW/°C.

Connection Diagram
8-Lead DIP
(Top View)



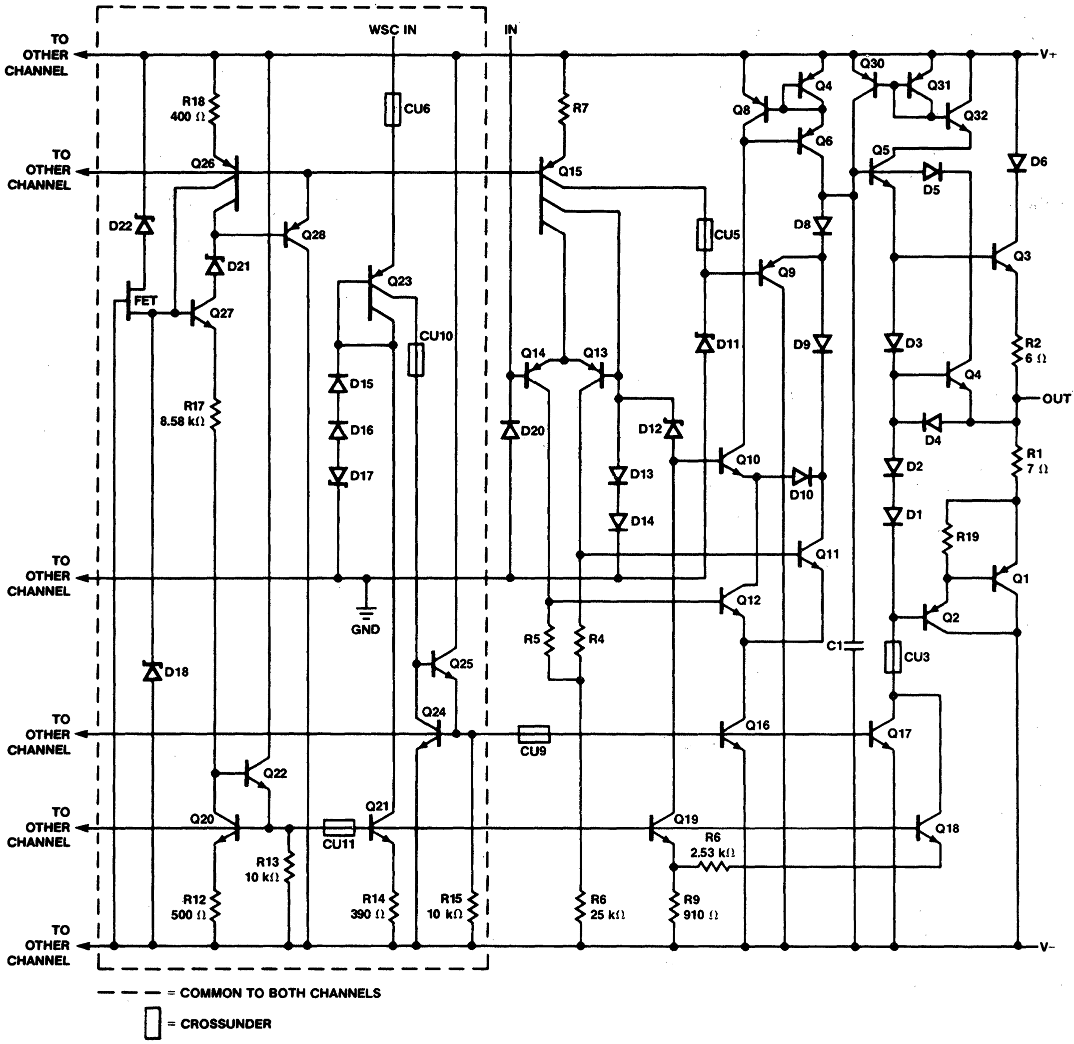
CD00920F

Order Information

Device Code	Package Code	Package Description
μA9636ARM	6T	Ceramic DIP
μA9636ARC	6T	Ceramic DIP
μA9636ATC	9T	Molded DIP

9

Equivalent Circuit



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Recommended Operating Conditions

Symbol	Characteristic	μA9636A			μA9636AC			Unit
		Min	Typ	Max	Min	Typ	Max	
V+	Positive Supply Voltage	10.8	12	13.2	10.8	12	13.2	V
V−	Negative Supply Voltage	−13.2	−12	−10.8	−13.2	−12	−10.8	V
T_A	Operating Temperature	−55	25	125	0	25	70	°C
R_{WS}	Wave Shaping Resistance	10		500	10		1000	kΩ

μA9636A

Electrical Characteristics Over recommended operating temperature, supply voltage and wave shaping resistance ranges unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH1}	Output Voltage HIGH	R_L to GND ($R_L = \infty$)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND ($R_L = 3.0$ kΩ)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND ($R_L = 450$ Ω)	4.0	5.5	6.0	V
V_{OL1}	Output Voltage LOW	R_L to GND ($R_L = \infty$)	−6.0	−5.7	−5.0	V
V_{OL2}		R_L to GND ($R_L = 3.0$ kΩ)	−6.0	−5.6	−5.0	V
V_{OL3}		R_L to GND ($R_L = 450$ Ω)	−6.0	−5.4	−4.0	V
R_O	Output Resistance	$450\ \Omega \leqslant R_L$		25	50	Ω
I_{OS+}	Output Short Circuit Current[1]	$V_O = 0$ V, $V_I = 0$ V	−150	−60	−15	mA
I_{OS-}		$V_O = 0$ V, $V_I = 2.0$ V	15	60	150	mA
I_{CEX}	Output Leakage Current	$V_O = \pm 6.0$ V, Power-Off	−100		+100	μA
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{IC}	Input Clamp Diode Voltage	$I_I = 15$ mA	−1.5	−1.1		V
I_{IL}	Input Current LOW	$V_I = 0.4$ V	−80	−16		μA
I_{IH}	Input Current HIGH	$V_I = 2.4$ V		1.0	10	μA
		$V_I = 5.5$ V		10	100	
I+	Positive Supply Current	$V_{CC} = \pm 12$ V, $R_L = \infty$, $R_{WS} = 100$ kΩ, $V_I = 0$ V		13	18	mA
I−	Negative Supply Current	$V_{CC} = \pm 12$ V, $R_L = \infty$, $R_{WS} = 100$ kΩ, $V_I = 0$ V	−18	−13		mA

Notes

1. Only one output should be shorted at a time.

μ**A9636A** (Cont.)

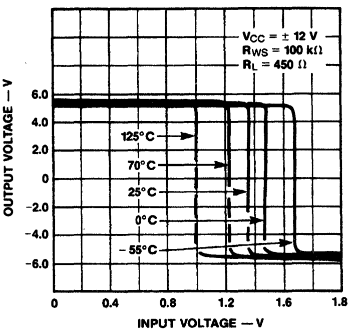
Electrical Characteristics Over recommended operating temperature, supply voltage and wave shaping resistance ranges unless otherwise specified.

AC Characteristics $V_{CC} = \pm 12\ V \pm 10\%$, $T_A = 25°C$, see AC Test Circuit

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_r	Rise Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	
t_f	Fall Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	

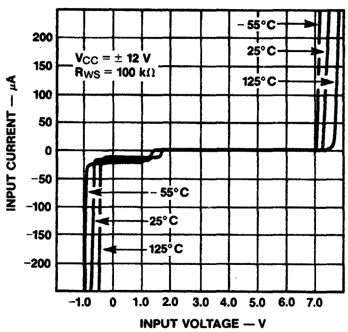
Typical Performance Curves

Input/Output Transfer Characteristic vs Temperature



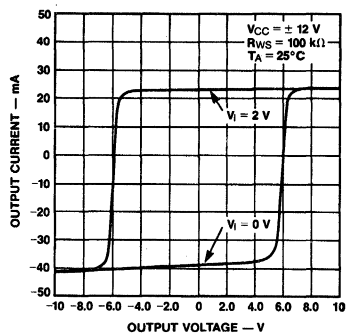
PC06091F

Input Current vs Input Voltage



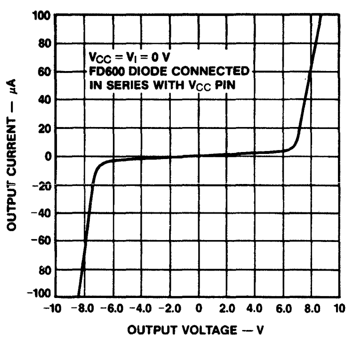
PC06081F

Output Current vs Output Voltage (Power On)



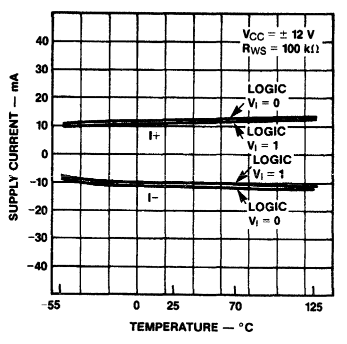
PC06101F

Output Current vs Output Voltage (Power Off)



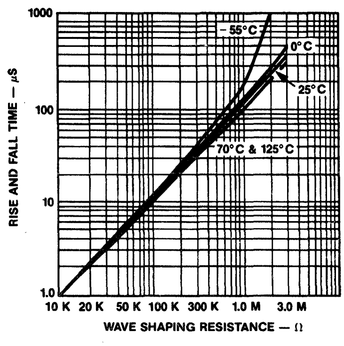
PC06111F

Supply Current vs Temperature



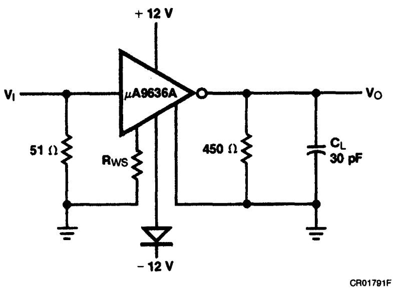
PC06121F

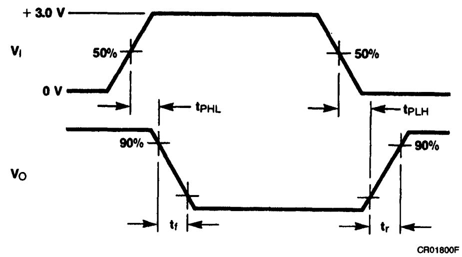
Transition Time vs R_{WS}



PC06131F

AC Test Circuit and Waveforms

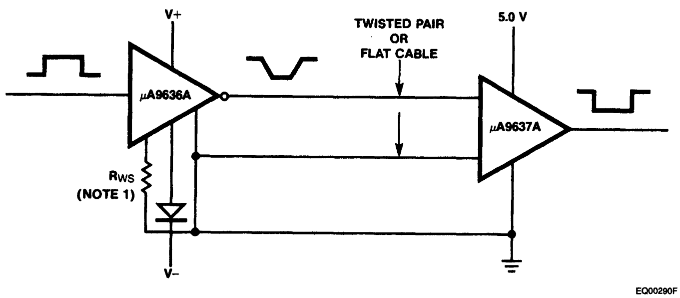




Note
C_L includes jig and probe capacitance

V_I
Amplitude: 3.0 V
Offset: 0 V
Pulse Width: 500 μs
PRR: 1.0 kHz
$t_r = t_f \leqslant 10$ ns

RS-423 System Application



Note
1. Use Fairchild's 1N4448.

FAIRCHILD

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μA9637A Dual Differential Line Receiver

Linear Division Interface Products

Description

The μA9637A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the μA9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The μA9637A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5.0 V power supply and has Schottky TTL compatible outputs. The μA9637A has an operational input common mode range of ±7.0 V either differentially or to ground.

- **Dual Channels**
- **Single 5.0 V Supply**
- **Satisfies EIA Standards RS-422 And RS-423**
- **Built-In ±35 mV Hysteresis**
- **High Common Mode Range**
- **High Input Impedance**
- **TTL Compatible Output**
- **Schottky Technology**
- **Extended Temperature Range**

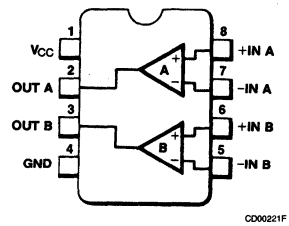
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	
Extended (μA9637AM)	-55°C to +125°C
Commercial (μA9637AC)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 30 s)	300°C
Molded DIP and SO Package (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
V_{CC} Lead Potential to Ground	-0.5 V to 7.0 V
Input Potential to Ground	±15 V
Differential Input Voltage	±15 V
Output Potential to Ground	-0.5 V to +5.5 V
Output Sink Current	50 mA

Notes

1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C, the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.

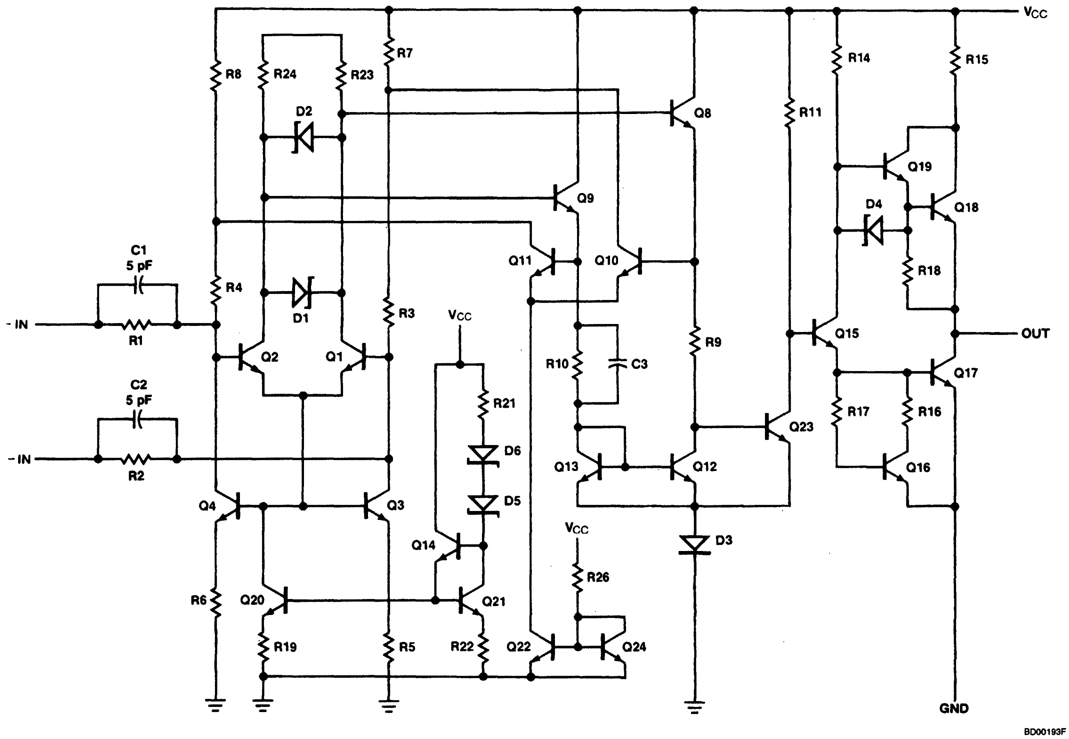
Connection Diagram
8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA9637ARM	6T	Ceramic DIP
μA9637ARC	6T	Ceramic DIP
μA9637ATC	9T	Molded DIP
μA9637ASC	KC	Molded Surface Mount

Equivalent Circuit



Recommended Operating Conditions

Symbol	Characteristic	μA9637A			μA9637AC			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating Temperature	−55	25	125	0	25	70	°C

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μA9637A
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

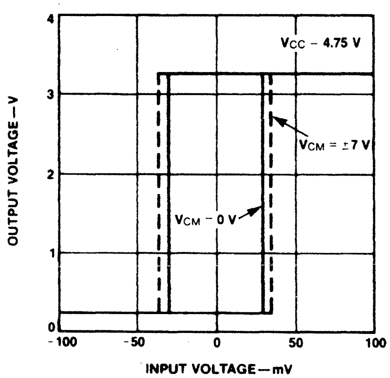
Symbol	Characteristic	Condition[1]	Min	Typ[2]	Max	Unit
V_{TH}	Differential Input Threshold Voltage[3]	$-7.0\ V \leq V_{CM} \leq +7.0\ V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage[4]	$-7.0\ V \leq V_{CM} \leq +7.0\ V$	−0.4		+0.4	V
I_I	Input Current[5]	$V_I = 10\ V,\ 0\ V \leq V_{CC} \leq +5.5\ V$		1.1	3.25	mA
		$V_I = -10\ V,\ 0\ V \leq V_{CC} \leq +5.5\ V$	−3.25	−1.6		
V_{OL}	Output Voltage LOW	$I_{OL} = 20\ mA,\ V_{CC} = Min$		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0\ mA,\ V_{CC} = Min$	2.5	3.5		V
I_{OS}	Output Short Circuit Current[6]	$V_O = 0\ V,\ V_{CC} = Max$	−40	−75	−100	mA
I_{CC}	Supply Current	$V_{CC} = Max,\ V_I+ = 0.5\ V,\ V_I- = GND$		35	50	mA
V_{HYST}	Input Hysteresis	$V_{CM} = \pm 7.0\ V$ (See Curves)		70		mV

AC Characteristics $V_{CC} = 5.0\ V,\ T_A = 25°C$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		15	25	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		13	25	ns

Notes
1. Use Min/Max values specified in recommended operating conditions.
2. Typical limits are at $V_{CC} = 5.0\ V$ and $T_A = 25°C$.
3. V_{DIFF} (Differential Input Voltage) = $(V_I+) - (V_I-)$. V_{CM} (Common Mode Input Voltage) = V_I+ or V_I-.
4. 500 Ω ±1% in series with inputs.
5. The input not under test is tied to ground.
6. Only one output should be shorted at a time.

Typical Input/Output Transfer Characteristics



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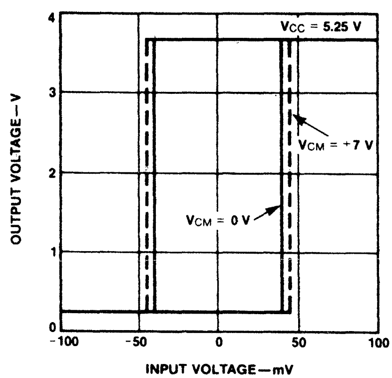

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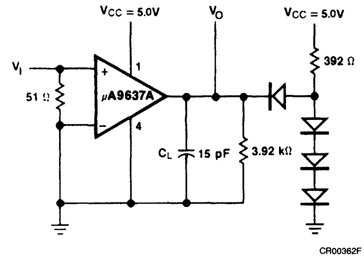
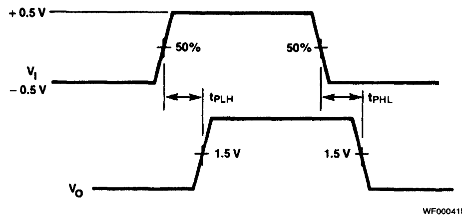
AC Test Circuit and Waveforms





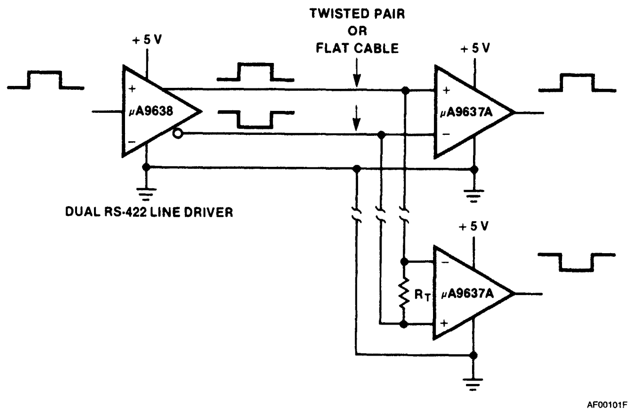
Notes

C_L includes jig and probe capacitance.
All diodes are FD700 or equivalent.

V_I
Amplitude: 1.0 V
Offset: 0.5 V
Pulse Width: 100 ns
PRR: 5.0 MHz
$t_r = t_f \leqslant 5.0$ ns

Typical Applications

RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission



Notes

$R_T \geqslant 50\ \Omega$ for RS-422 operation
R_T combined with input impedance of receivers must be greater than 90 Ω.

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μA9638
RS-422 Dual High Speed Differential Line Driver

Linear Division Interface Products

Description

The μA9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50 Ω transmission lines at high speed. The mini-DIP provides high package density.

- **Single 5.0 V Supply**
- **Schottky Technology**
- **TTL And CMOS Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Complementary Outputs**
- **Minimum Output Skew (< 1.0 ns Typical)**
- **50 mA Output Drive Capability For 50 Ω Transmission Lines**
- **Meets EIA RS-422 Specifications**
- **Propagation Delay Of Less Than 10 ns**
- **"Glitchless" Differential Output**
- **Delay Time Stable With V_{CC} And Temperature Variations (< 2.0 ns Typical) (Figure 3)**
- **Extended Temperature Range**

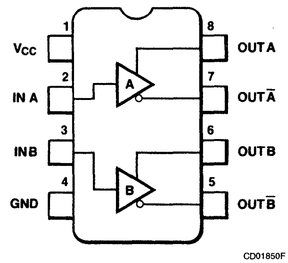
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP and SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA9638M)	−55°C to +125°C
Commercial (μA9638C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO Package (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W
V_{CC} Lead Potential to Ground	−5.0 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, 150°C for the Molded DIP and SO-8.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Ceramic DIP at 8.7 mW/°C; the 8L-Molded DIP at 7.5 mW/°C, and the SO-8 at 6.5 mW/°C.

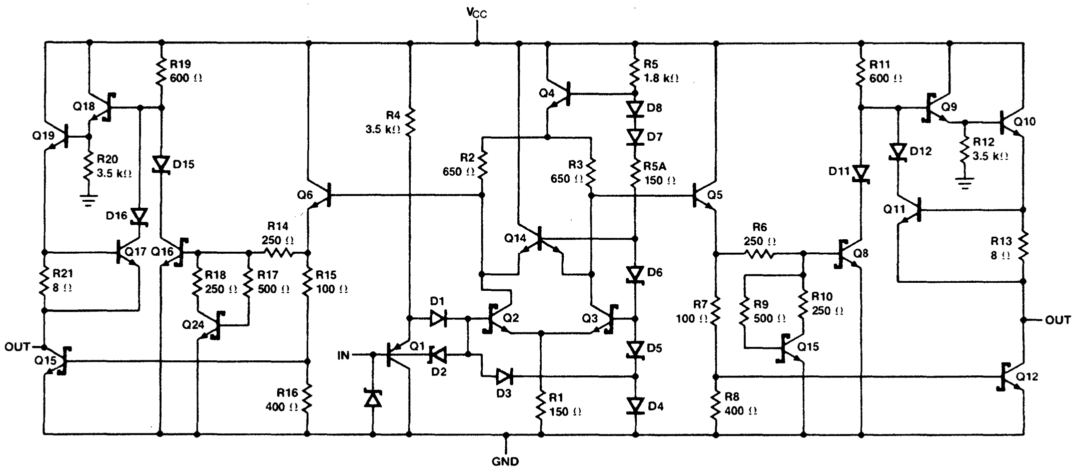
Connection Diagram
8-Lead DIP and SO-8 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA9638RM	6T	Ceramic DIP
μA9638RC	6T	Ceramic DIP
μA9638TC	9T	Molded DIP
μA9638SC	KC	Molded Surface Mount

Equivalent Circuit



Recommended Operating Conditions

Symbol	Characteristic	μA9638			μA9638C			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
I_{OH}	Output Current HIGH			−50			−50	mA
I_{OL}	Output Current LOW			50			50	mA
T_A	Operating Temperature	−55	25	125	0	25	70	°C

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μA9638
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW	Commercial				0.8	V
		Extended				0.5	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.0	−1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $V_{IH} = V_{IH\ Min}$, $V_{IL} = V_{IL\ Max}$	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2.0			
V_{OL}	Output Voltage LOW	V_{CC} = Min, $V_{IH} = V_{IH\ Min}$, $V_{IL} = V_{IL\ Max}$, I_{OL} = 40 mA				0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_{I\ Max}$ = 5.5 V				50	μA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IH} = 2.7 V				25	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_{IL} = 0.5 V				−200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0 V		−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See *Figure 1*		2.0			V
$V_T - \overline{V}_T$	Output Balance					0.4	V
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage					3.0	V
$V_{OS} - \overline{V}_{OS}$	Output Offset Balance					0.4	V
I_X	Output Leakage Current	T_A = 25°C, −0.25 V < V_X < 6.0 V				100	μA
I_{CC}	Supply Current (both drivers)	V_{CC} = 5.5 V, All Input at 0 V, No Load			45	65	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition	Min	Typ[2]	Max	Unit
t_{PHL}	Propagation Delay	C_L = 15 pF, R_L = 100 Ω, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90% − 10%			10	20	ns
t_r	Rise Time, 10% − 90%			10	20	ns
$t_{PO} - t_{\overline{PO}}$	Skew Between Outputs A/$\overline{A}$ and B/$\overline{B}$			1.0		ns

Notes
1. Use minimum and maximum values specified in recommended operating conditions.
2. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.

DC Test Circuit

Figure 1 Terminated Output Voltage and Output Balance

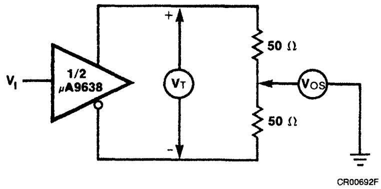
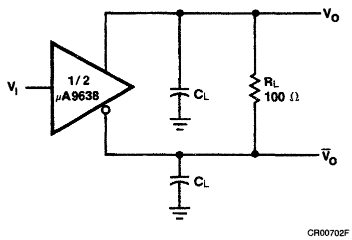
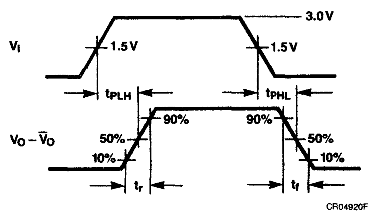


Figure 2 AC Test Circuit and Voltage Waveform

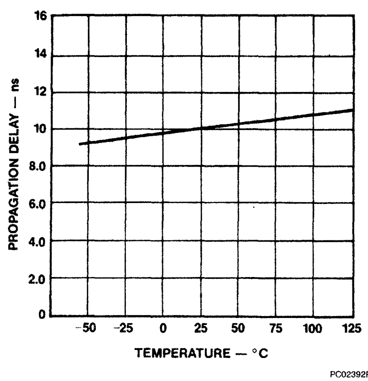


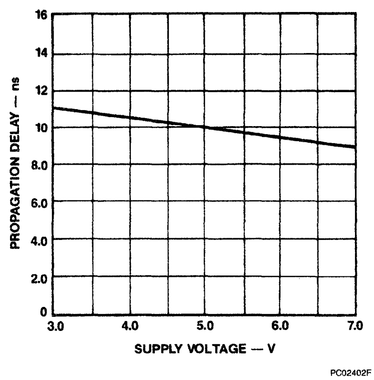


Notes

The pulse generator has the following characteristics:
PRR = 500 kHz t_W = 100 ns,
$t_r \leq 5.0$ ns, $Z_O = 50\ \Omega$.
C_L includes probe and jig capacitance

Figure 3 Typical Delay Characteristics





FAIRCHILD

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μA9639A Dual Differential Line Receiver

Linear Division Interface Products

Description

The μA9639A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422, RS-423, and RS-232C. In addition, the μA9639A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The μA9639A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5.0 V power supply and has Schottky TTL compatible outputs. The μA9639A has an operational input common mode range of ±7.0 V either differentially or to ground.

- **Dual Channels**
- **Single 5.0 V Supply**
- **Satisfies EIA Standards RS-422, RS-423, And RS-232C**
- **Built-In ±35 mV Hysteresis**
- **High Common Mode Range**
- **High Input Impedance**
- **TTL Compatible Output**
- **Schottky Technology**

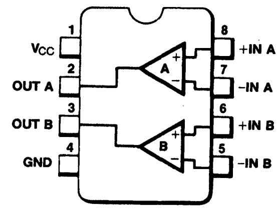
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	0.93 W
V_{CC} Lead Potential to Ground	-0.5 V to +7.0 V
Input Potential to Ground Lead	±25 V
Differential Input Voltage	±25 V
Output Differential to Ground Lead	-0.5 V to 5.5 V
Output Sink Current	50 mA

Note

1. $T_{J\ Max}$ = 150°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 7.5 mW/°C.

Connection Diagram
8-Lead DIP
(Top View)

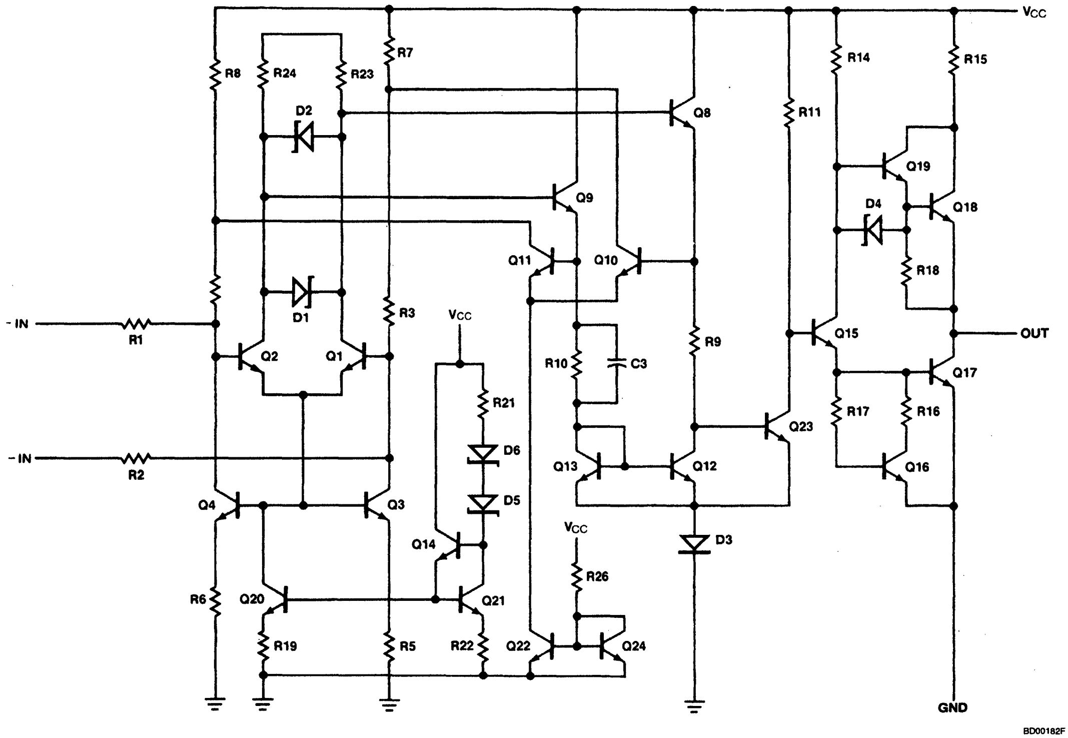


CD00221F

Order Information

Device Code	Package Code	Package Description
μA9639ATC	9T	Molded DIP

Equivalent Circuit



Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Temperature	0	25	70	°C

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μA9639A
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

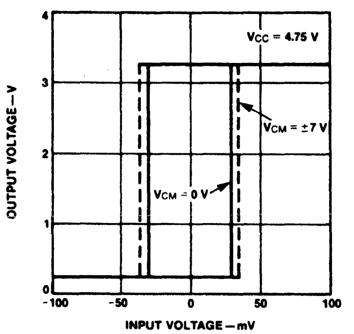
Symbol	Characteristic	Condition[1]	Min	Typ[2]	Max	Unit
V_{TH}	Differential Input Threshold Voltage[3]	$-7.0\ V \leqslant V_{CM} \leqslant +7.0\ V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage[4]	$-7.0\ V \leqslant V_{CM} \leqslant +7.0\ V$	−0.4		+0.4	V
I_I	Input Current[5]	$V_I = 10\ V,\ 0\ V \leqslant V_{CC} \leqslant 5.5\ V$		1.1	3.25	mA
		$V_I = -10\ V,\ 0\ V \leqslant V_{CC} \leqslant 5.5\ V$	−3.25	−1.6		
V_{OL}	Output Voltage LOW	$I_{OL} = 20$ mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0$ mA, V_{CC} = Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current[6]	$V_O = 0$ V, V_{CC} = Max	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, $V_I+ = 0.5$ V, $V_I- =$ GND		35	50	mA
V_{HYST}	Input Hysteresis	$V_{CM} = \pm 7.0$ V (See Curves)		70		mV

AC Characteristics $V_{CC} = 5.0$ V, $T_A = 25°C$

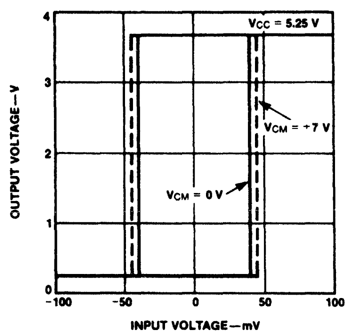
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		55	85	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		50	75	ns

1. Use Min/Max values specified in recommended operating conditions.
2. Typical limits are at $V_{CC} = 5.0$ V and $T_A = 25°C$.
3. V_{DIFF} (Differential Input Voltage) = $(V_{I+}) - (V_{I-})$.
   V_{CM} (Common Mode Input Voltage) = V_{I+} or V_{I-}.
4. 500 Ω ±1% in series with inputs.
5. The input not under test is tied to ground.
6. Only one output should be shorted at a time.

Typical Input/Output Transfer Characteristics

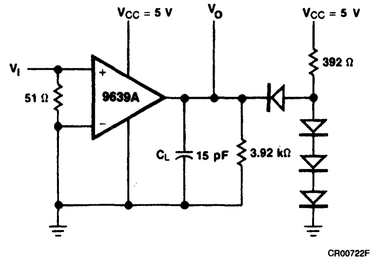


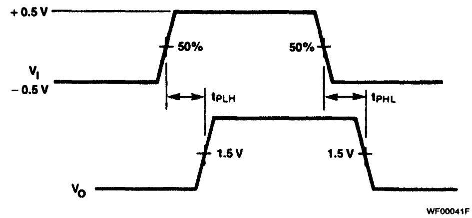
PC01942F



PC01952F

AC Test Circuit and Waveforms





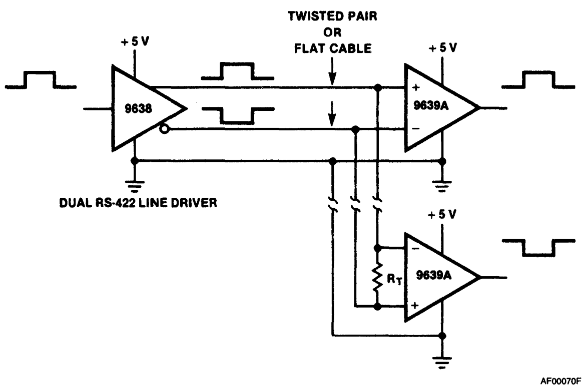
Notes
C_L includes jig and probe capacitance.
All diodes are FD700 or equivalent.

V_I
Amplitude: 1.0 V
Offset: 0.5 V
Pulse Width: 500 ns
PRR: 1 MHz
$t_r = t_f \leqslant 5.0$ ns

9

Typical Applications

RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission



Notes
$R_t \geqslant 50\ \Omega$ for RS-422 operation
R_t combined with input impedance of receivers must be greater than 90 Ω.

FAIRCHILD

A Schlumberger Company

μA9640(26S10) Quad General Purpose Bus Transceiver

Linear Division Interface Products

Description

The μA9640(26S10) is a high speed quad bus transceiver. Each driver output, which is capable of sinking 100 mA at 0.8 V, is connected internally to the high speed bus receiver in addition to being connected to the package lead. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads. The bus output is capable of driving lines having 100 Ω impedance.

The line can be terminated at both ends and still give considerable noise margin at the receiver. The typical switching point of the receiver is 2.0 V.

The μA9640(26S10) features advanced Schottky processing to minimize propagation delay. The device package also has two ground leads to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

The μA9640(26S10) is a lead for lead replacement for the AM26S10.

- **Input To Bus Is Inverting**
- **Quad High Speed Open Collector Bus Transceivers**
- **Driver Outputs Can Sink 100 mA At 0.8 V Maximum**
- **Advanced Schottky Processing**
- **PNP Input To Reduce Input Loading**

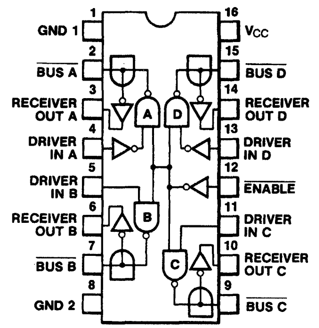
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA9640M)	−55°C to +125°C
Commercial (μA9640C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V_{CC} Lead Potential to Ground	−0.5 V to +7.0 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to V_{CC} Max
Input Voltage	−0.5 V to +5.5 V
Output Current, into Bus	200 mA
Output, into Outputs (except Bus)	30 mA
Input Current	−30 mA to +5.0 mA

Notes

1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



Order Information

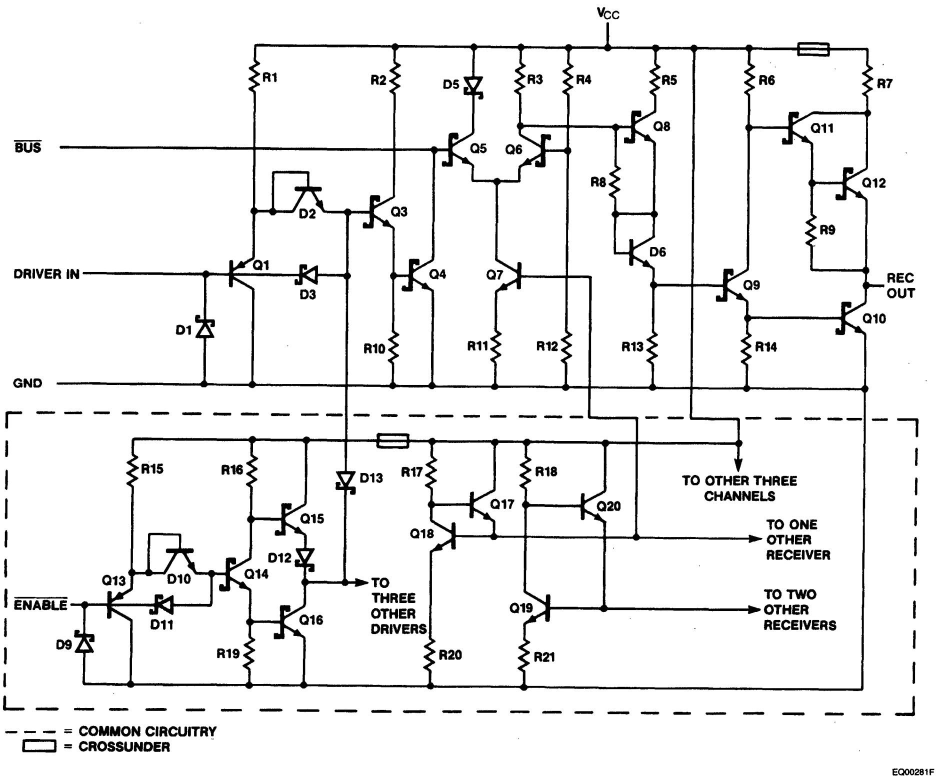
Device Code	Package Code	Package Description
μA9640DM(26S10)	6B	Ceramic DIP
μA9640DC(26S10)	6B	Ceramic DIP
μA9640PC(26S10)	9B	Molded DIP

Truth Table

Inputs		Outputs	
$\overline{ENABLE}$	Driver IN_{A-D}	$\overline{BUS}_{A-D}$	Receiver Out_{A-D}
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes control by another bus transceiver.)

Equivalent Circuit (1/4 of Circuit - Except Strobe)



Recommended Operating Conditions

Symbol	Characteristic	Extended[4] Min	Extended[4] Typ	Extended[4] Max	Commercial[5] Min	Commercial[5] Typ	Commercial[5] Max	Unit
V_{CC}	Supply Voltage	4.50	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating Temperature	−55	25	125	0	25	70	°C

μA9640(26S10)
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]		Min	Typ[2]	Max	Unit
V_{OH}	Output Voltage HIGH (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1.0 mA, $V_I = V_{IL}$ or V_{IH}	Extended[4]	2.5	3.4		V
			Comm[5]	2.7	3.4		
V_{OL}	Output Voltage LOW (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, $V_I = V_{IL}$ or V_{IH}				0.5	V
V_{IH}	Input Voltage HIGH (Except Bus)	Guaranteed Input Logic HIGH for All Inputs		2.0			V
V_{IL}	Input Voltage LOW (Except Bus)	Guaranteed Input Logic LOW for All Inputs				0.8	V
V_{IC}	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4 V	ENABLE			−0.36	mA
			DATA			−0.54	
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7 V	ENABLE			20	μA
			DATA			30	
		V_{CC} = Max, V_I = 5.5 V				100	
I_{OS}	Output Short Circuit Current (Except Bus)[3]	V_{CC} = Max	Extended[4]	−20		−55	mA
			Comm[5]	−18		−60	
I_{CC}	Supply Current	V_{CC} = Max, $V_I = V_{IH}$, Enable = GND			45	70	mA

AC Characteristics V_{CC} = 5.0 V, T_A = 25°C

Symbol	Characteristic	Condition[6]	Min	Typ[2]	Max	Unit
t_{PD}	Data Input to Bus	R_B = 50 Ω, C_B = 50 pF		10	15	ns
	Enable Input to Bus			14	18	
	Bus to Receiver Out	R_B = 50 Ω, R_L = 280 Ω, C_B = 50 pF, C_L = 15 pF		10	15	
t_r	Rise Time Bus	R_B = 50 Ω, C_B = 50 pF	4.0	10		ns
t_f	Fall Time Bus		2.0	4.0		ns

μA9640(26S10) (Cont.)

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

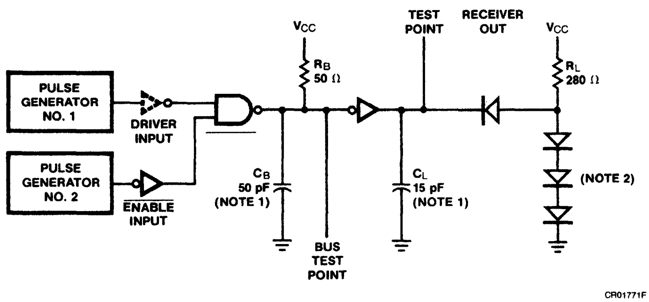
Bus Input/Output Characteristics

Symbol	Characteristic	Condition[1]			Min	Typ[2]	Max	Unit
V_{OL}	Output Voltage LOW	V_{CC} = Min	Extended[4]	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Comm[5]	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_{CEX} (ON)	Bus Leakage Current	V_{CC} = Max		V_O = 0.8 V			−50	μA
			Extended[4]	V_O = 4.5 V			200	
			Comm[5]	V_O = 4.5 V			100	
I_{CEX} (OFF)	Bus Leakage Current	V_O = 4.5 V, V_{CC} = 0 V					100	μA
$V_{TH}+$	Receiver Input Threshold HIGH	Bus Enable = 2.4 V, V_{CC} = Max	Extended[4]			2.0	2.4	V
			Comm[5]			2.0	2.25	
$V_{TH}-$	Receiver Input Threshold LOW	Bus Enable = 2.4 V, V_{CC} = Min	Extended[4]		1.6	2.0		V
			Comm[5]		1.75	2.0		

Notes

1. For conditions shown as Min or Max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Extended temperature range, ceramic DIP.
5. Commercial temperature range, ceramic or molded DIP.
6. C_B and C_L include probe and jig capacitance.

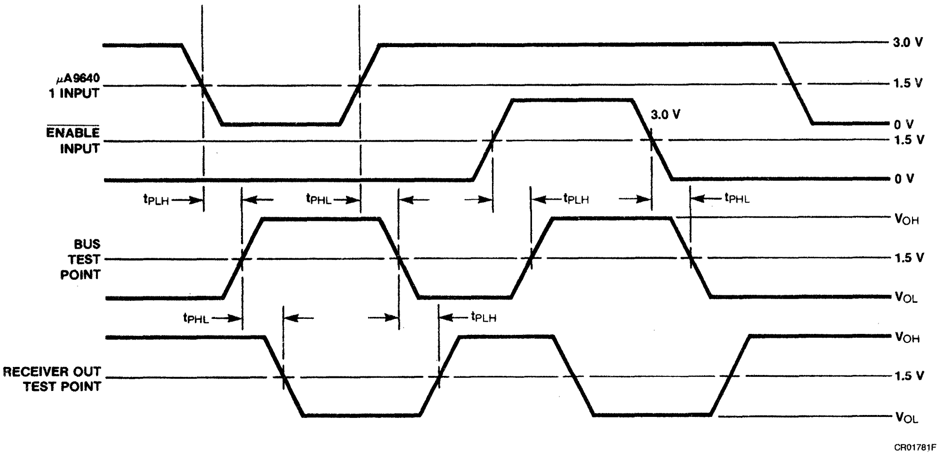
Figure 1 AC Test Circuit



Note

1. Includes probe and jig capacitance.
2. All Diodes 1N916 or equivalent.

Figure 2 Waveforms



FAIRCHILD

A Schlumberger Company

μA9643
Dual TTL To MOS/CCD Driver

Linear Division Interface Products

Description

The μA9643 is a dual positive logic "AND" TTL-to-MOS driver. The μA9643 is a functional replacement for the SN75322 with one important exception: the two external PNP transistors are no longer needed for operation. The μA9643 is also a functional replacement for the 75363 with the important exception that the V_{CC3} supply is not needed. The lead connections normally used for the external PNP transistors are purposely not internally connected to the μA9643.

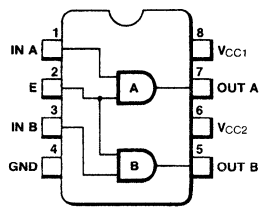
- **Satisfies CCD Memory And Delay Line Requirements**
- **Dual Positive Logic TTL To MOS Driver**
- **Operates From Standard Bipolar And MOS Supply Voltages**
- **High Speed Switching**
- **TTL And DTL Compatible Inputs**
- **Separate Drivers Address Inputs With Common Strobe**
- **V_{OH} And V_{OL} Compatible With Popular MOS RAMs**
- **Does Not Require External PNP Transistors Or V_{CC3}**
- **V_{OH} Minimum Is $V_{CC2} - 0.5$ V**

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	0.93 W
Supply Voltage Range of V_{CC1} [3]	-0.5 V to +7.0 V
Supply Voltage Range of V_{CC2}	-0.5 V to +15 V
Input Voltage	5.5 V
Inter-Input Voltage[4]	5.5 V

Notes
1. $T_{J\ Max} = 150°C$
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 7.5 mW/°C.
3. Voltage values are with respect to network ground terminals unless otherwise noted.
4. This rating applies between any two inputs of any one of the gates.

Connection Diagram
8-Lead DIP
(Top View)



CD00890F

Order Information

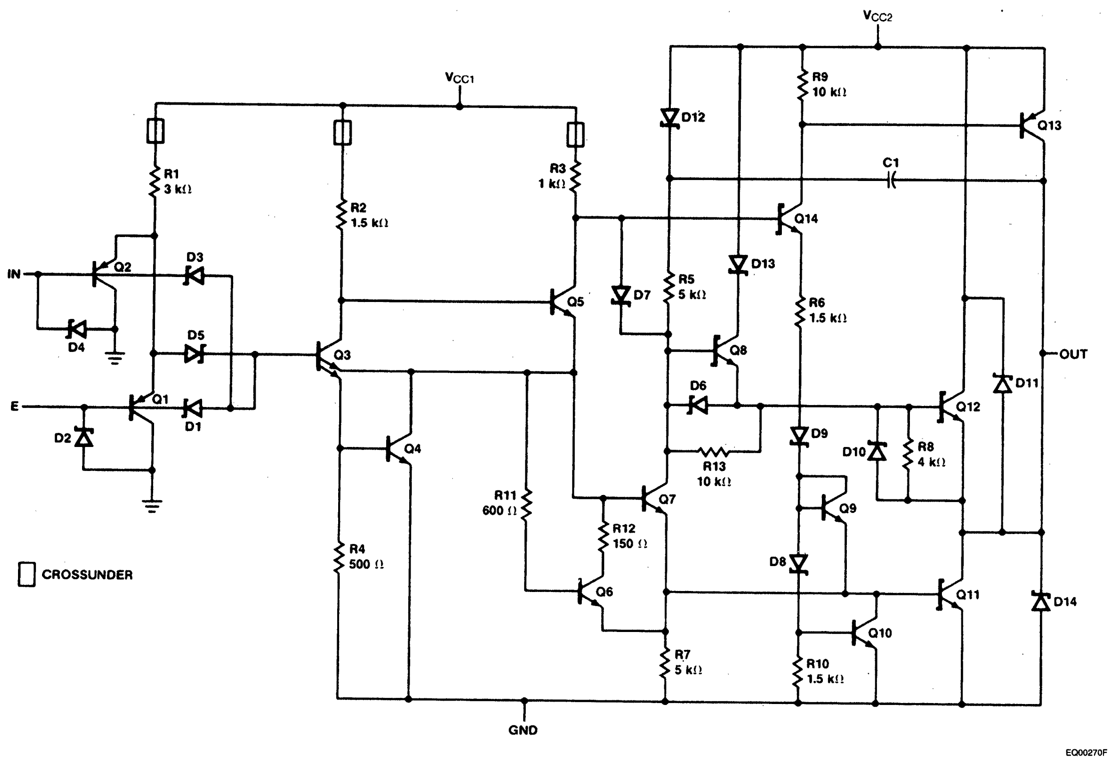
Device Code	Package Code	Package Description
μA9643TC	9T	Molded DIP

Truth Table

INPUT	ENABLE	OUTPUT
L	L	L
L	H	L
H	L	L
H	H	H

9

Equivalent Circuit (1/2 of Circuit)



Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Unit
V_{CC1}	Supply Voltage	4.75	5.0	5.25	V
V_{CC2}	Supply Voltage	11.4	12	12.6	V
T_A	Operating Temperature	0	25	70	°C

μA9643
Electrical Characteristics Over recommended operating temperature and V_{CC1}, V_{CC2} ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -400$ μA		$V_{CC2} - 0.5$	$V_{CC2} - 0.2$		V
V_{OL}	Output Voltage LOW	$I_{OL} = 10$ mA			0.4	0.5	V
		$I_{OL} = 1.0$ mA			0.2	0.3	
I_I	Input Current at Maximum Input Voltage	$V_{CC1} = 5.25$ V, $V_{CC2} = 11.4$ V $V_I = 5.25$ V				0.1	mA
I_{IH}	Input Current HIGH	$V_I = 2.4$ V	A Inputs			40	μA
			E Inputs			80	
I_{IL}	Input Current LOW	$V_I = 0.4$ V	A Inputs			−0.5	mA
			E Inputs			−1.0	
$I_{CC1(L)}$	Supply Current from V_{CC1} All Outputs LOW	$V_{CC1} = 5.25$ V, $V_{CC2} = 12.6$ V			15	19	mA
$I_{CC2(L)}$	Supply Current from V_{CC2} All Outputs LOW	$V_{CC1} = 5.25$ V, $V_{CC2} = 12.6$ V			5.5	9.5	mA
$I_{CC1(H)}$	Supply Current from V_{CC1} All Outputs HIGH	$V_{CC1} = 5.25$ V, $V_{CC2} = 12.6$ V			9.0	13	mA
$I_{CC2(H)}$	Supply Current from V_{CC2} All Outputs HIGH	$V_{CC1} = 5.25$ V, $V_{CC2} = 12.6$ V			5.5	9.5	mA

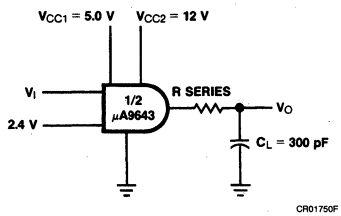
AC Characteristics $V_{CC1} = 5.0$ V, $V_{CC2} = 12$ V, $T_A = 25°C$

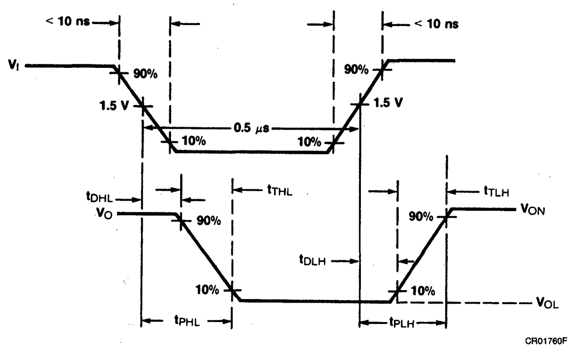
Symbol	Characteristic	Condition		Min	Typ	Max	Unit
t_{DLH}	Delay Time		$C_L = 300$ pF	5.0	9.0	17	ns
t_{DHL}	Delay Time			5.0	9.0	17	ns
t_{TLH}	Rise Time	$R_{SERIES} = 0$	$C_L = 300$ pF	6.0	11	17	ns
t_{THL}	Fall Time			6.0	11	17	ns
t_{TLH}	Rise Time	$R_{SERIES} = 10\ \Omega$	$C_L = 300$ pF	8.0	14	20	ns
t_{THL}	Fall Time			8.0	14	20	ns
t_{PLHA-} t_{PLHB} t_{PHLA-} t_{PHLB}	Skew between outputs A and B				0.5		ns

Note
1. All typical values are at $V_{CC1} = 5.0$ V, $V_{CC2} = 12.0$ V, and $T_A = 25°C$ unless otherwise noted.

9

AC Test Circuit and Waveforms





Notes
The pulse generator has the following characteristics:
PRR = 1.0 MHz, Z_0 = 50 Ω
C_L includes probe and jig capacitance.

μA9645(3245) Quad TTL To MOS/CCD Driver

Linear Division Interface Products

Description

The μA9645(3245) is a high speed driver intended to be used as a clock (high level) driver for 18 or 22-lead dynamic NMOS RAMs. It also satisfies the non-overlapping 2-phase clock drive requirements for CCD memories like the F464 (64K) RAM.

The circuit is designed to operate on nominal +5.0 V and +12 V power supplies and contains input and output clamp diodes to minimize line reflections.

The device features two common enable inputs, a refresh select input and a clock control input. Internal gating structure is organized so that all four drivers may be deactivated for standby operation, or a single driver may be activated for read/write operation or all four drivers may be activated for refresh operation.

The μA9645(3245) is a lead for lead replacement of the Intel 3245 Quad TTL-to-MOS Driver, with substantially reduced DC power dissipation.

- **Interchangeable With Intel 3245**
- **Four High Speed, High Current Drivers**
- **Control Logic Optimized For MOS RAMs**
- **Satisfies CCD Memory And Delay Line Drive Requirements**
- **TTL And DTL Compatible Inputs**
- **High Voltage Schottky Technology**

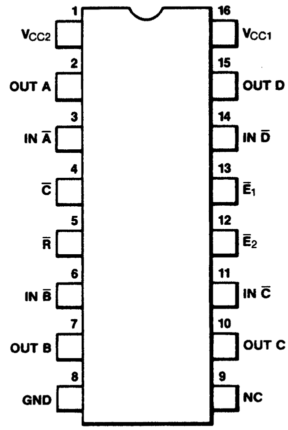
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage, V_{CC1}	−0.5 V to +7.0 V
Supply Voltage, V_{CC2}	−0.5 V to +14.0 V
All Input Voltages	−1.0 V to V−
Outputs For Clock Driver	−1.0 V to (V−) +1.0 V
Temperature Under Bias	−10°C to +70°C

Notes

1. $T_{J\,Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram
16-Lead DIP
(Top View)



CD00311F

Order Information

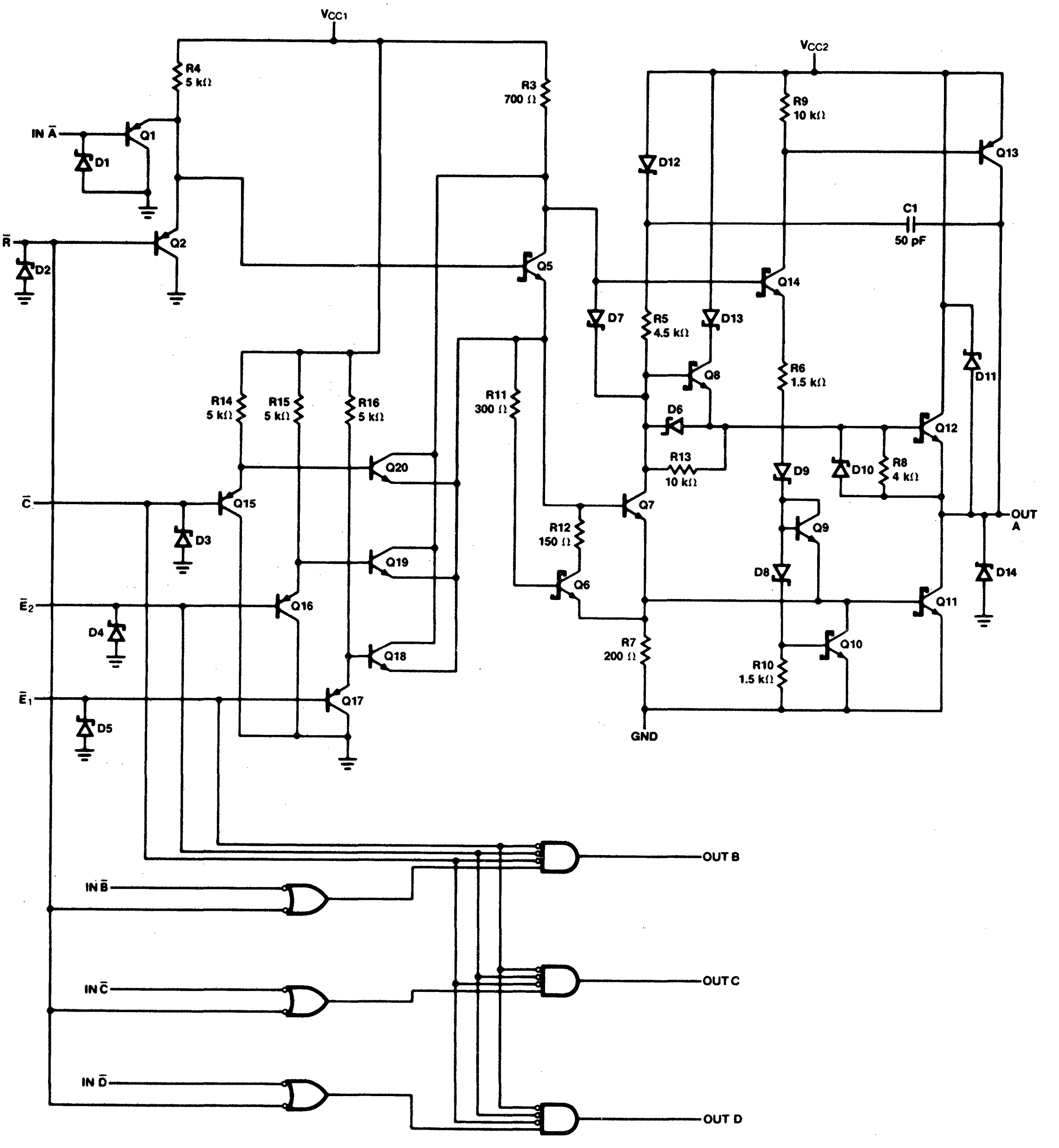
Device Code	Package Code	Package Description
μA9645DC(3245)	7B	Ceramic DIP
μA9645PC(3245)	9B	Molded DIP

Truth Table

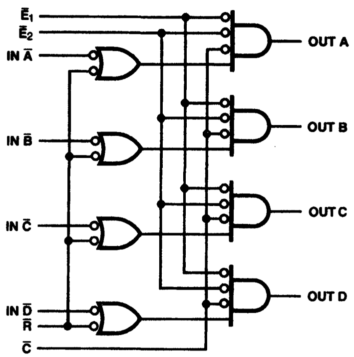
Inputs					Output
Control			Address		
$\overline{C}$	$\overline{E}_2$	$\overline{E}_1$	$\overline{\text{INPUT}}$	$\overline{\text{REFRESH}}$	
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	H	L
L	L	L	L	X	H
L	L	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

Equivalent Circuit



Logic Diagram



CD00320F

μA9645(3245)
Electrical Characteristics V_{CC1} = 5.0 V ±5%, V_{CC2} = 12 V ±5%, T_A = 0°C to 70°C, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{FD}	Input Load Current, IN ($\overline{A}$,$\overline{B}$,$\overline{C}$,$\overline{D}$)	V_F = 0.45 V			−0.25	mA
I_{FE}	Input Load Current, $\overline{R}$, $\overline{C}$, $\overline{E}_1$, $\overline{E}_2$	V_F = 0.45 V			−1.0	mA
I_{RD}	Data Input Leakage Current	V_R = 5.0 V			10	μA
I_{RE}	Enable Input Leakage Current	V_R = 5.0 V			40	μA
V_{OL}	Output Voltage LOW	I_{OL} = 5.0 mA, V_{IH} = 2.0 V			0.45	V
		I_{OL} = −5.0 mA	−1.0			
V_{OH}	Output Voltage HIGH	I_{OH} = −1.0 mA, V_{IL} = 0.8 V	V_{CC2}−0.50			V
		I_{OH} = 5.0 mA			V_{CC2} + 1.0	
V_{IL}	Input Voltage LOW, All Inputs				0.8	V
V_{IH}	Input Voltage HIGH, All Inputs		2.0			V
$I+_H$	Positive Supply Current HIGH	V_{CC1} = 5.25 V		13	20	mA
$I-_H$	Negative Supply Current HIGH	V_{CC2} = 12.6 V		14	20	mA
$P_{C(H)}$	Power Consumption HIGH	All Outputs HIGH		248	357	mW
	Power Per Channel			62	90	mW
$I+_L$	Positive Supply Current LOW	V_{CC1} = 5.25 V		27	35	mA
$I-_L$	Negative Supply Current LOW	V_{CC2} = 12.6 V		12	15	mA
$P_{C(L)}$	Power Consumption LOW	All Outputs LOW		296	373	mW
	Power Per Channel			74	94	mW

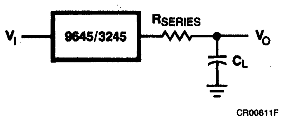
μA9645(3245) (Cont.)
Electrical Characteristics V_{CC1} = 5.0 V ±5%, V_{CC2} = 12 V ±5%, T_A = 0°C to 70°C, unless otherwise specified.

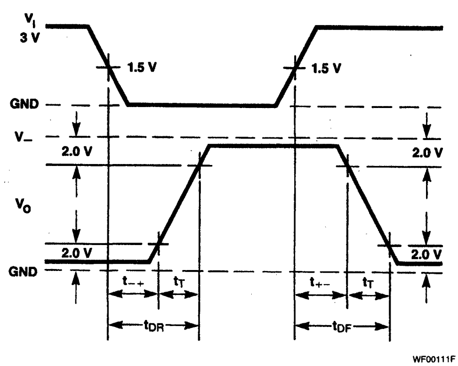
AC Characteristics

Symbol	Characteristic	Condition	Min[1]	Typ[2,4]	Max[3]	Unit
t−(+)	Input to Output Delay	R_{SERIES} = 0	5.0	11		ns
t_{DR1}	Delay Plus Rise Time	R_{SERIES} = 0		18	32	ns
t+(−)	Input to Output Delay	R_{SERIES} = 0	3.0	7.0		ns
t_{DF1}	Delay Plus Fall Time	R_{SERIES} = 0		18	32	ns
t_T	Output Transition Time	R_{SERIES} = 20 Ω	10	13	20	ns
t_{DR2}	Delay Plus Rise Time	R_{SERIES} = 20 Ω		27	38	ns
t_{DF2}	Delay Plus Fall Time	R_{SERIES} = 20 Ω		24	38	ns

Notes
1. C_L = 150 pF
2. C_L = 200 pF
3. C_L = 250 pF
4. Typical values are measured at T_A = 25°C

AC Test Circuit and Waveforms





Note
AC Test Conditions:
Input Pulse Amplitude = 3.0 V
Input Pulse Rise and Fall Times = 5.0 ns Between 1.0 V and 2.0 V

FAIRCHILD

A Schlumberger Company

μA9665 • μA9666 μA9667 • μA9668 High Current/Voltage Darlington Drivers

Linear Division Interface Products

Description

The μA9665, μA9666, μA9667, and μA9668 are comprised of seven high voltage, high current NPN Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter base resistors for leakage.

The μA9665 is a general purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. Input current limiting is done by connecting an appropriate discrete resistor to each input.

The μA9666 version does away with the need for any external discrete resistors, since each unit has a resistor and a Zener diode in series with the input. The μA9666 was specifically designed for direct interface from PMOS logic (operating at supply voltages from 14 V to 25 V) to solenoids or relays.

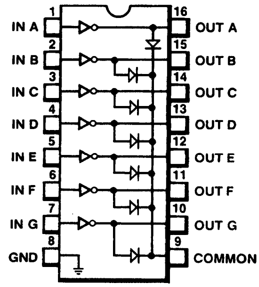
The μA9667 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0 V.

The μA9668 has an appropriate input resistor to allow direct operation from CMOS or PMOS outputs operating from supply voltages of 6.0 V to 15 V.

The μA9665, μA9666, μA9667, and μA9668 offer solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

- **Seven High Gain Darlington Pairs**
- **High Output Voltage (V_{CE} = 50 V)**
- **High Output Current (I_C = 350 mA)**
- **DTL, TTL, PMOS, CMOS Compatible**
- **Suppression Diodes For Inductive Loads**
- **2 Watt Molded DIP On Copper Lead Frame**
- **Extended Temperature Range**

Connection Diagram
16-Lead DIP
(Top View)



CD00940F

Order Information

Device Code	Package Code	Package Description
μA9665DC	6B	Ceramic DIP
μA9665PC	9B	Molded DIP
μA9666DM	6B	Ceramic DIP
μA9666DC	6B	Ceramic DIP
μA9666PC	9B	Molded DIP
μA9667DM	6B	Ceramic DIP
μA9667DC	6B	Ceramic DIP
μA9667PC	9B	Molded DIP
μA9668DM	6B	Ceramic DIP
μA9668DC	6B	Ceramic DIP
μA9668PC	9B	Molded DIP

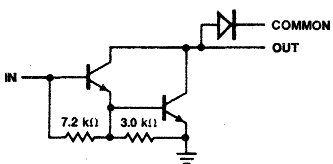
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA9666/7/8M)	−55°C to +125°C
Commercial (μA9665/6/7/8C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Input Voltage	30 V
Output Voltage	55 V
Emitter-Base Voltage	6.0 V
Continuous Collector Current	500 mA
Continuous Base Current	25 mA

Notes
1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.
3. Under normal operating conditions, these units will sustain 350 mA per output with $V_{CE(Sat)}$ = 1.6 V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

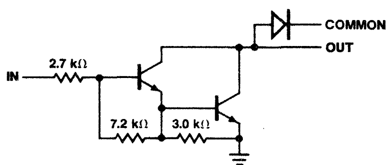
Equivalent Circuits

μA9665



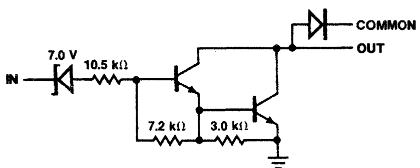
EQ00321F

μA9667



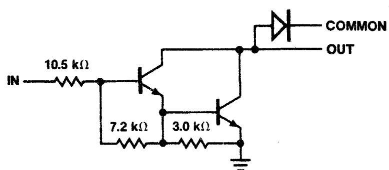
EQ00341F

μA9666



EQ00331F

μA9668



EQ00351F

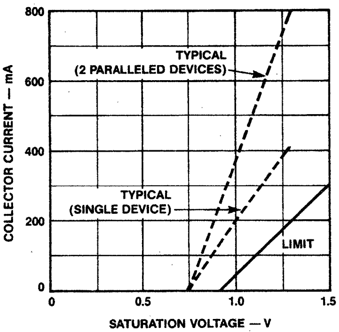
μA9665/6/7/8
Electrical Characteristics $T_A = 25°C$, unless otherwise specified.

Symbol	Characteristic	Conditions[1]		Test Figure	Min	Typ	Max	Unit
I_{CEX}	Output Leakage Current	$T_A = 70°C$ for Commercial $V_{CE} = 50$ V		1a			100	μA
		$V_{CE} = 50$ V, $V_I = 6.0$ V	μA9666	1b			500	
		$V_{CE} = 50$ V, $V_I = 1.0$ V	μA9668	1b			500	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 350$ mA, $I_B = 500$ μA		2		1.25	1.6	V
		$I_C = 200$ mA, $I_B = 350$ μA		2		1.1	1.3	
		$I_C = 100$ mA, $I_B = 250$ μA		2		0.9	1.1	
$I_{I(ON)}$	Input Current	$V_I = 17$ V	μA9666	3		0.85	1.3	mA
		$V_I = 3.85$ V	μA9667	3		0.93	1.35	
		$V_I = 5.0$ V	μA9668	3		0.35	0.5	
		$V_I = 12$ V		3		1.0	1.45	
$I_{I(OFF)}$	Input Current[2]	$T_A = 70°C$ for Commercial $I_C = 500$ μA		4	50	65		μA
$V_{I(ON)}$	Input Voltage[3]	$V_{CE} = 2.0$ V, $I_C = 300$ mA	μA9666	5			13	V
		$V_{CE} = 2.0$ V, $I_C = 200$ mA	μA9667	5			2.4	
		$V_{CE} = 2.0$ V, $I_C = 250$ mA		5			2.7	
		$V_{CE} = 2.0$ V, $I_C = 300$ mA		5			3.0	
		$V_{CE} = 2.0$ V, $I_C = 125$ mA	μA9668	5			5.0	
		$V_{CE} = 2.0$ V, $I_C = 200$ mA		5			6.0	
		$V_{CE} = 2.0$ V, $I_C = 275$ mA		5			7.0	
		$V_{CE} = 2.0$ V, $I_C = 350$ mA		5			8.0	
h_{FE}	DC Forward Current Transfer Ratio	$V_{CE} = 2.0$ V, $I_C = 350$ mA	μA9665	2	1000			
C_I	Input Capacitance					15	30	pF
t_{PLH}	Turn-On Delay	0.5 V_I to 0.5 V_O				1.0	5.0	μs
t_{PHL}	Turn-Off Delay	0.5 V_I to 0.5 V_O				1.0	5.0	μs
I_R	Clamp Diode Leakage Current	$V_R = 50$ V		6			50	μA
V_F	Clamp Diode Forward Voltage	$I_F = 350$ mA		7		1.7	2.0	V

Notes
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{I(OFF)}$ current limit guaranteed against partial turn-on of the output.
3. The $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

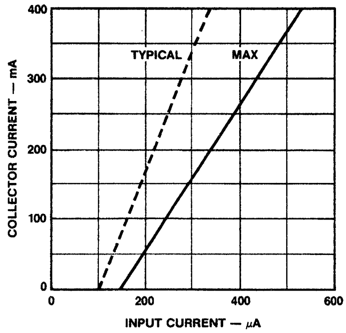
Typical Performance Curves

Collector Current vs Saturation Voltage



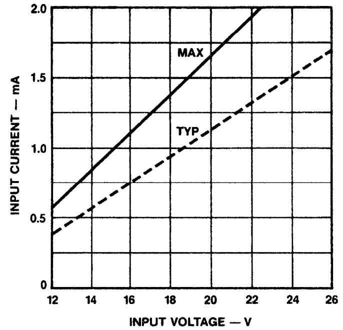
PC06231F

Collector Current vs Input Current



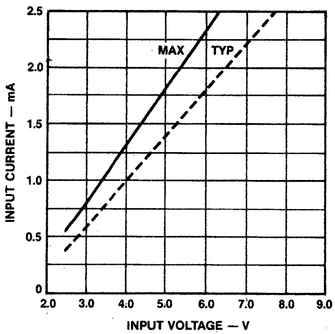
PC06241F

μA9666 Input Current vs Input Voltage



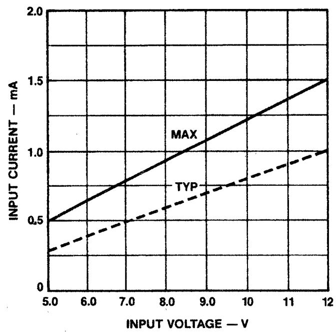
PC06251F

μA9667 Input Current vs Input Voltage



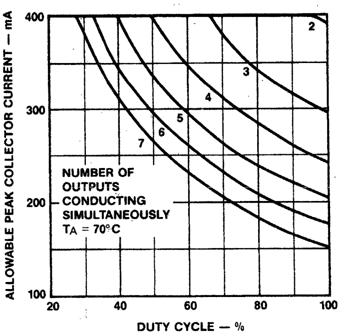
PC06261F

μA9668 Input Current vs Input Voltage



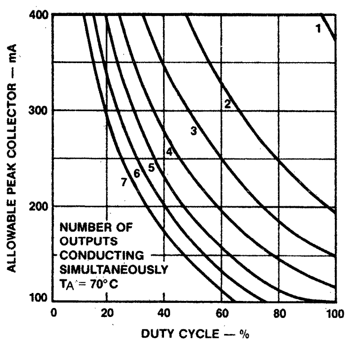
PC06271F

Peak Collector Current vs Duty Cycle and Number of Outputs (Molded Package)



PC06291F

Peak Collector Current vs Duty Cycle and Number of Outputs (Ceramic Package)



PC06301F

Test Circuits

Figure 1a

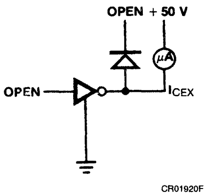


Figure 1b

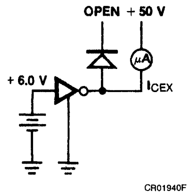


Figure 2

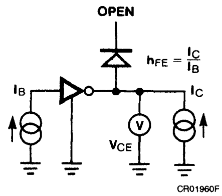


Figure 3

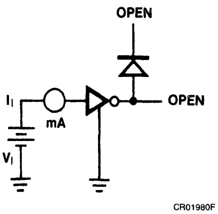


Figure 4

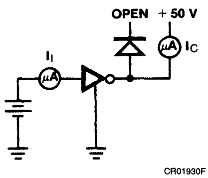


Figure 5

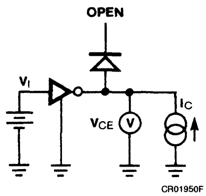


Figure 6

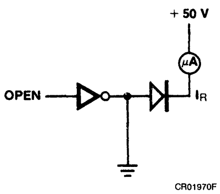
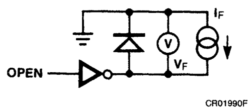


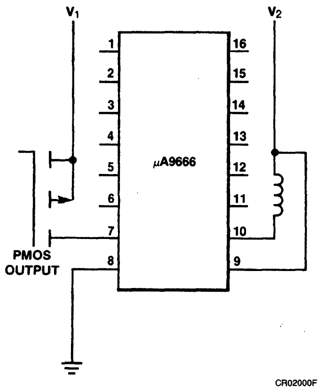
Figure 7



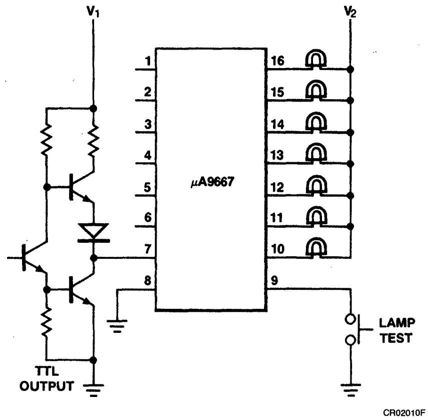
9

Typical Applications

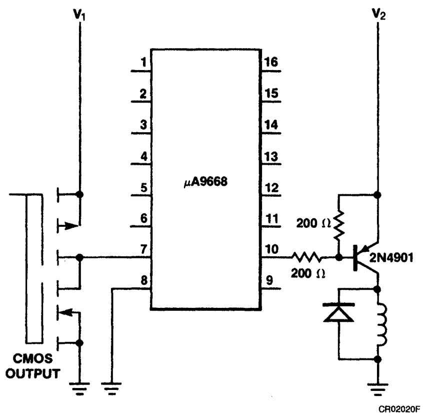
PMOS to Load



Buffer for Higher Current Loads



TTL to Load



µA9679 Differential Bus Repeater

Description

The µA9679 Differential Bus Repeater is a monolithic integrated circuit designed for bidirectional data communication on balanced bus transmission lines. The repeater meets EIA Standard RS-422A.

The µA9679 combines a three-state differential line driver and a differential input line receiver, both of which operate from a single 5.0 volt power supply. The driver and receiver are operated from a single enable lead. When one device is active, the other device is disabled. This feature allows for complete isolation of the driver from the receiver function.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown protection for line fault conditions. Thermal shutdown is designed to occur at a junction temperature of ≈ 160°C. The receiver features a typical input impedance of 12 kΩ, an input sensitivity of ±200 mV and a typical input hysteresis of 50 mV.

- **Meets EIA Standard RS-422A**
- **Three-State Control**
- **Common Enable For Isolation**
- **Driver Output Capability ±60 mA**
- **Thermal Shutdown Protection**
- **Positive And Negative Current Limiting**
- **High Impedance Receiver Input**
- **Receiver Input Sensitivity Of ±200 mV**
- **Receiver Input Hysteresis Of 50 mV Typical**
- **Operates From Single 5.0 V Supply**
- **Low Power Requirements**

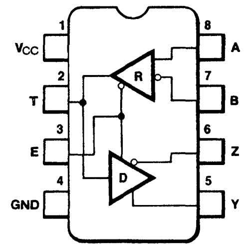
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	0.93 W
Supply Voltage[3]	7.0 V
Input Voltage	5.5 V

Notes

1. $T_{J\,Max} = 150°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 7.5 mW/°C.
3. All voltage values are with respect to network ground terminal.

Connection Diagram
8-Lead DIP
(Top View)



CD01430F

Order Information

Device Code	Package Code	Package Description
µA9679TC	9T	Molded DIP

Function Table Receiver

Differential Inputs	Enable	Output	Driver
A-B	E	T	
$V_{ID} \geqslant 0.2$ V	L	H	Z
$-0.2\ V \leqslant V_{ID} < 0.2$ V	L	?	Z
$V_{ID} \leqslant -0.2$ V	L	L	Z
X	H	Z	See Function Table Driver

Function Table Driver

Driver Input	Enable	Output	Receiver
A-B	E	Y Z	
H	H	H L	Z
L	H	L H	Z

H = High Level
L = Low Level
? = Indeterminate
X = Immaterial
Z = High Impedance (off)

Recommended Operating Conditions

Symbol	Characteristic		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{ID}	Differential Input Voltage[1]				± 12	V
I_{OH}	Output Current HIGH	Driver			−60	mA
		Receiver			−400	μA
I_{OL}	Output Current LOW	Driver			60	mA
		Receiver			16	
T_A	Operating Temperature		0	25	70	°C

Note
1. The algebraic convention where the less positive (more negative) limit is designated minimum is used in this data sheet for common mode input voltage and threshold voltage levels only.

μA9679
Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

Driver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	$I_O = 0$ V				4.0	V
$\|V_{OD2}\|$	Differential Output Voltage	$R_L = 100\ \Omega$		2.0	2.25		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage					± 0.2	V
I_O	Output Current with Power Off	$V_{CC} = 0$ V, $V_O = -0.25$ V to 6.0 V				± 100	μA
I_{OZ}	High Impedance State Output Current	$V_O = -0.25$ V to 6.0 V			± 50	± 100	μA
I_{IH}	Input Current HIGH	$V_I = 2.7$ V				20	μA
I_{IL}	Input Current LOW	$V_I = 0.5$ V				−100	μA
I_{OS}	Output Short Circuit Current	$V_O = V_{CC}$				150	mA
		$V_O = 0$ V				−150	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

μA9679 (Cont.)

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

Driver Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DD}	Differential Output Delay Time	R_L = 100 Ω		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 100 Ω		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27 Ω		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27 Ω		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110 Ω		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110 Ω		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110 Ω		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110 Ω		29	35	ns

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Receiver Section

Symbol	Characteristic	Condition		Min	Typ[1]	Max	Unit
V_{TH+}	Differential Input High Threshold Voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TH-}	Differential Input Low Threshold Voltage[2]	V_O = 0.5 V, I_O = 8.0 mA		−0.2			V
$(V_{TH+}) - (V_{TH-})$	Hysteresis[3]				50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA		2.7			V
V_{OL}	Output Voltage LOW	I_{OL} = 8.0 mA				0.45	V
		I_{OL} = 16 mA				0.50	
I_{OZ}	High-Impedance State Output Current	V_O = 0.4 V				±100	μA
		V_O = 2.4 V					
I_I	Line Input Current[4]	V_I = 12 V	Other Input = 0 V			1.0	mA
		V_I = −7.0 V				−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7 V				100	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4 V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Output Short Circuit Current			−15		−85	mA
I_{CC}	Supply Current (total package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

μA9679 (Cont.)

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

Receiver Switching Characteristics, V_{CC} = 5.0 V, T_A = 25°C.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Notes
1. All Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
3. Hysteresis is the difference between the positive going input threshold voltage, V_T+, and the negative going input, V_T-.
4. Refer to EIA Standard RS-422A for exact conditions.

Parameter Measurement Information

Figure 1 Driver V_{OD2} and V_{OC}

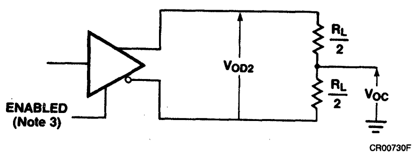


Figure 2 Driver V_{OD2} with Varying Common Mode Voltage

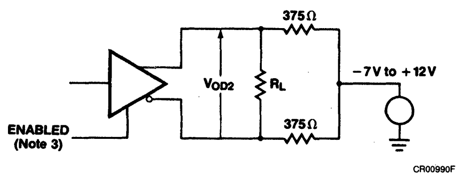
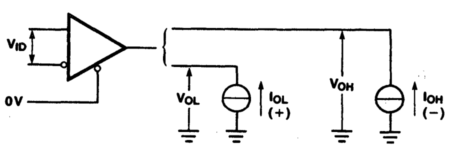


Figure 3 Receiver V_{OH} and V_{OL}



Parameter Measurement Information (Cont.)

Figure 4 Driver Differential Output Delay and Transition Times

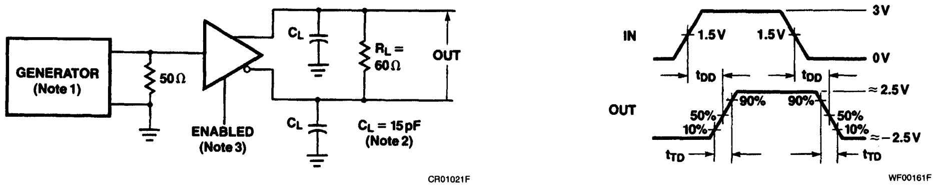


Figure 5 Drive Propagation Times

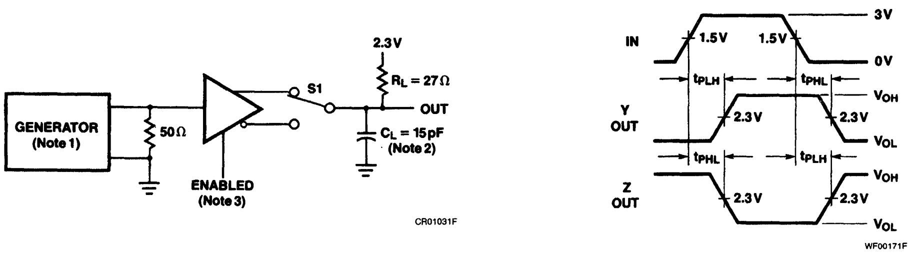


Figure 6 Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

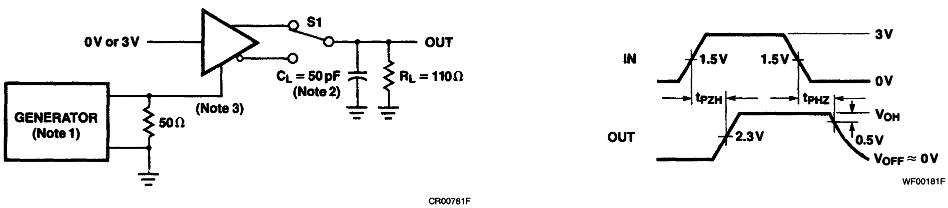
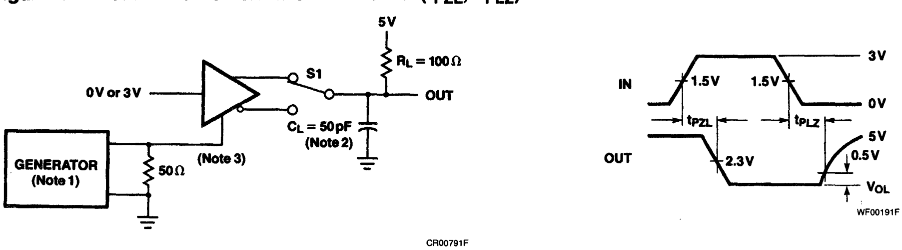


Figure 7 Driver Enable and Disable Times (t_{PZL}, t_{PLZ})



9

Parameter Measurement Information (Cont.)

Figure 8 Receiver Propagation Delay Times

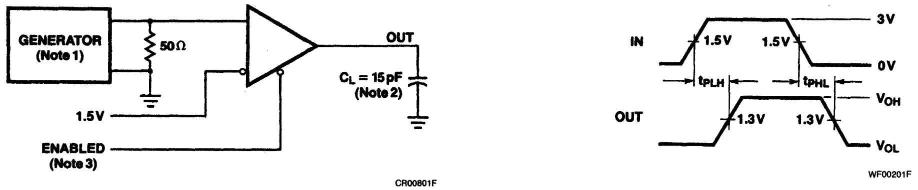
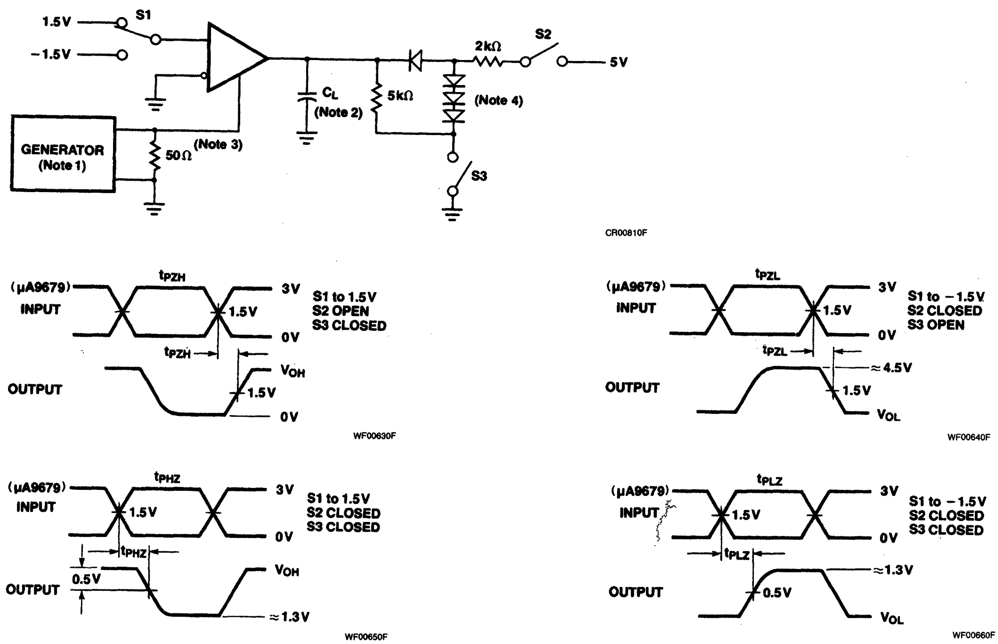


Figure 9 Receiver Enable and Disable Times



Notes

1. The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle≈50%, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\ \Omega$.
2. C_L includes probe and stray capacitance.
3. µA96178 Enable is active low, µA96177 Enable is active high.
4. All diodes are 1N916 or equivalent.

FAIRCHILD

A Schlumberger Company

DAC08
8-Bit Multiplying D/A Converter

Linear Division Data Acquisition

Description

The DAC08 is an 8-bit multiplying digital-to-analog converter constructed using the Fairchild Planar Epitaxial process. Advanced circuit design achieves very high speed performance with outstanding applications capability and low cost.

- **Fast Settling Time To 1/2 LSB 85 ns**
- **Full Scale Current Prematched To ±1 LSB**
- **Direct Interface To TTL, CMOS, ECL, HTL, PMOS, DTL**
- **Linearity To ±0.19% Max Over Temperature Range**
- **High Output Compliance −10 V To +18 V**
- **True And Complemented Outputs**
- **Wide Range Multiplying Capability**
- **Low Full Scale Current Drift +10 ppm/°C TYP**
- **Wide Power Supply Range ±4.5 V To ±18 V**
- **Low Power Consumption 33 mW at ±5 V**
- **External Compensation For Max Bandwidth**
- **Low Cost**

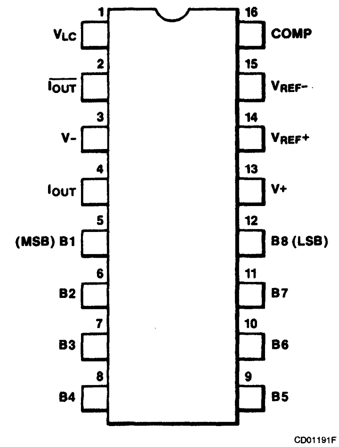
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (DAC08M)	−55°C to +125°C
Commercial (DAC08C)	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V+ to V−	36 V
Logic Inputs	V− to (V−) + 36 V
V_{LC}	V− to V+
Reference Inputs (V_{14}, V_{15})	V− to V+
Reference Input Differential	
Voltage (V_{14}, V_{15})	±18 V
Reference Input Current I_{REF} (14)	5.0 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Molded DIP at 8.3 mW/°C, the 16L-Ceramic DIP at 10 mW/°C.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
DAC08DM	7B	Ceramic DIP
DAC08EDC	7B	Ceramic DIP
DAC08EPC	9B	Molded DIP
DAC08CDC	7B	Ceramic DIP
DAC08CPC	9B	Molded DIP

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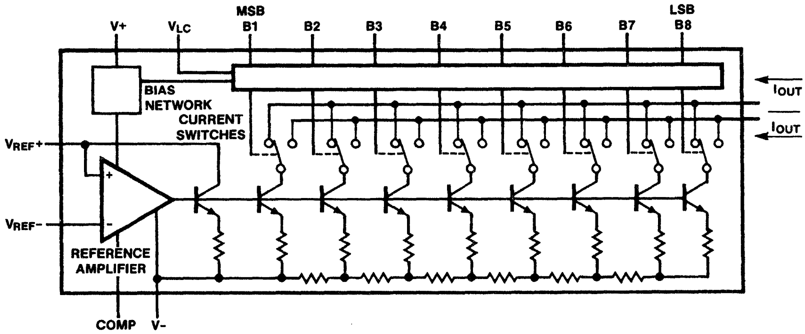
Block Diagram



EQ00470F

DAC08, DAC08E, and DAC08C

Electrical Characteristics T_A = 0°C to 70°C for the DAC08E and DAC08C, −55°C to +125°C for the DAC08; V_{CC} = ±15 V, I_{REF} = 2.0 mA. Output characteristics refer to both $\overline{I_{OUT}}$ and I_{OUT}.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
RESO	Resolution			8.0	8.0	8.0	bits
MONO	Monotonicity			8.0	8.0	8.0	bits
NL	Nonlinearity	DAC08, DAC08E				±0.19	% FS
		DAC08C				±0.39	
t_s	Settling Time	To ± ½ LSB, all bits switched, ON or OFF T_A = 25°C	DAC08		85	135	ns
			DAC08E/C		85	150	
t_{PLH}	Propagation Delay	T_A = 25°C	Each bit		35	60	ns
t_{PHL}			All bits switched		35	60	
TCI_{FS}	Full Scale Temperature Coefficient				±10		ppm/°C
V_{OC}	Output Voltage Compliance	Full scale current change < ½ LSB, R_O > 20 mΩ		−10		+18	V
I_{FS4}	Full Scale Current	V_{REF} = 10.000 V, R_{14}, R_{15} = 5.000 kΩ, T_A = 25°C		1.940	1.990	2.040	mA
I_{FSS}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$	DAC08/E		±1.0	±8.0	μA
			DAC08C		±2.0	±16	
I_{ZS}	Zero Scale Current		DAC08/E		0.2	2.0	μA
			DAC08C		0.2	4.0	
I_{FSR}	Output Current Range	$R_{14, 15}$ = 5.000 kΩ					mA
		V_{REF} = +15.000 V, V− = −10 V		2.1			
		V_{REF} = +25.000 V, V− = −12 V		4.2			
V_{IL}	Logic Input Voltage LOW	V_{LC} = 0 V				0.8	V
V_{IH}	Logic Input Voltage HIGH			2.0			
I_{IL}	Logic Input Current LOW	V_{LC} = 0 V, V_I = −10 V to +0.8 V			−2.0	−10	μA

DAC08 Series (Cont.)

Electrical Characteristics T_A = 0°C to 70°C for the DAC08E and DAC08C, −55°C to +125°C for the DAC08; V_{CC} = ±15 V, I_{REF} = 2.0 mA. Output characteristics refer to both $\overline{I_{OUT}}$ and I_{OUT}.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Logic Input Current HIGH	V_I = +2.0 V to +18 V		0.002	10	μA
V_{IS}	Logic Input Swing	V− = −15 V	−10		+18	V
V_{THR}	Logic Threshold Range	V_{CC} = ±15 V	−10		+13.5	V
I_{15}	Reference Input Bias Current			−1.0	−3.0	μA
dI/dt	Reference Current Slew Rate		4.0	8.0		mA/μS
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +4.5 V to +18 V, I_{REF} = 1.000 mA		0.0003	0.01	%/%
$PSSI_{FS-}$		V− = −4.5 V to −18 V, I_{REF} = 1.000 mA		0.002	0.01	
I+	Power Supply Current	V_{CC} = ±5.0 V, I_{REF} = 1.000 mA		2.3	3.8	mA
I−				−4.3	−5.8	
I+		V+ = +5.0 V, I_{REF} = 2.000 mA, V− = −15 V		2.4	3.8	
I−				−6.4	−7.8	
I+		V_{CC} = ±15 V, I_{REF} = 2.000 mA		2.5	3.8	
I−				−6.4	−7.8	
P_c	Power Consumption	V_{CC} = ±5.0 V, I_{REF} = 1.000 mA		33	48	mW
		V+ = +5.0 V, V− = −15 V, I_{REF} = 2.000 mA		108	136	
		V_{CC} = ±15 V, I_{REF} = 2.000 mA		135	174	

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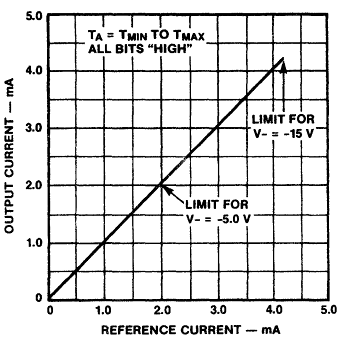
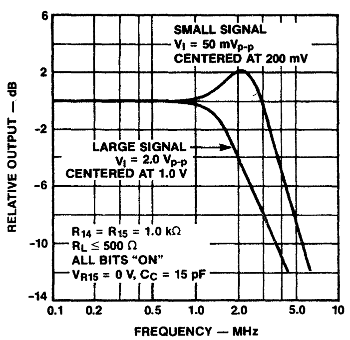
Typical Performance Curves

Full Scale Current vs Reference Current



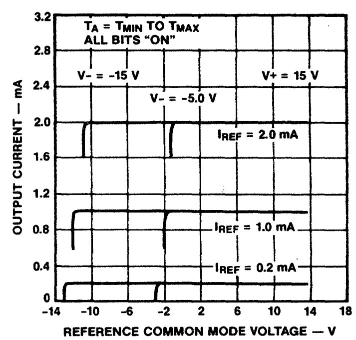
PC7540F

Reference Input Frequency Response



PC07550F

Reference AMP Common Mode Range (Note 1)



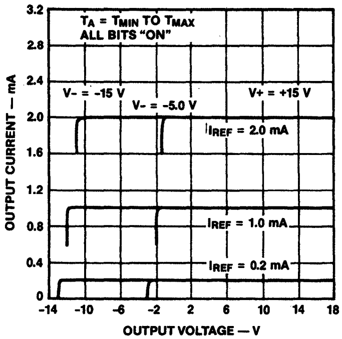
PC07560F

Note

1. Positive common mode range is always (V+) −1.5 V

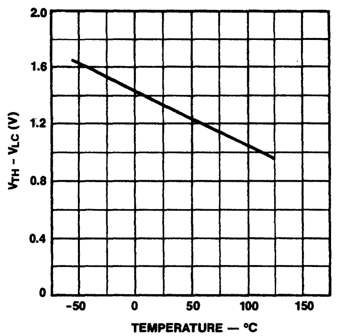
Typical Performance Curves (Cont.)

Output Current vs Output Voltage (Output Voltage Compliance)



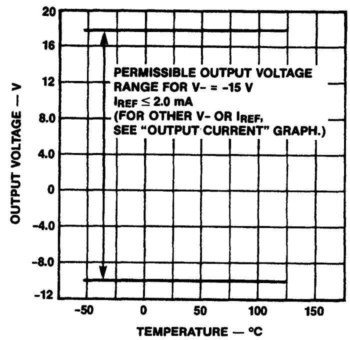
PC07570F

$V_{TH} - V_{LC}$ vs Temperature



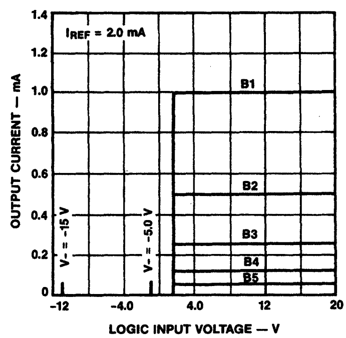
PC07580F

Output Voltage Compliance vs Temperature



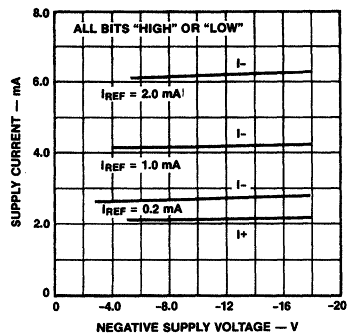
PC07590F

Bit Transfer Characteristics (Note 1)



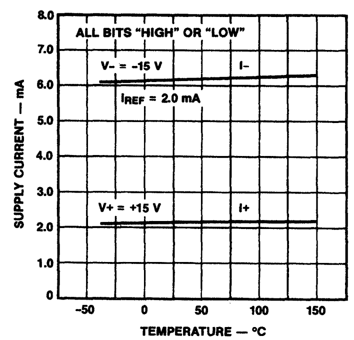
PC07600F

Supply Current vs Negative Supply Voltage



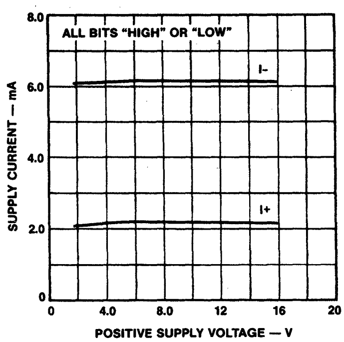
PC07610F

Supply Current vs Temperature



PC07620F

Supply Current vs Positive Supply Voltage



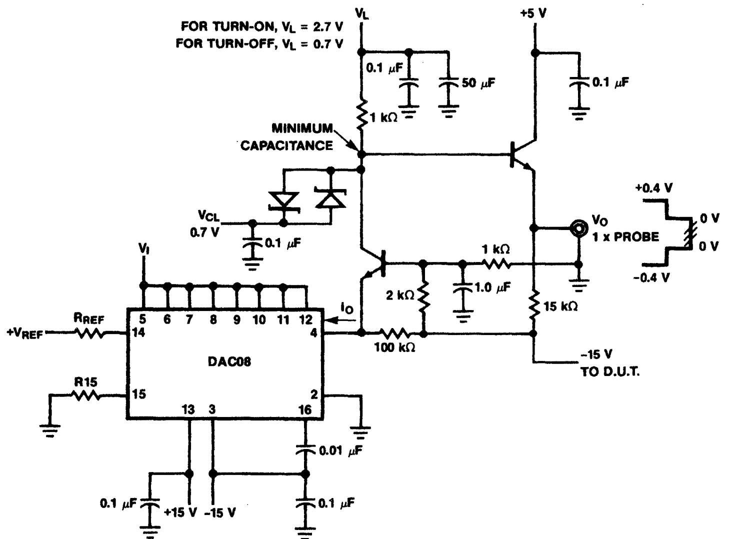
PC07630F

Note

1. B1 through B8 have identical transfer characteristics. Bits are fully switched, with less than 1/2 LSB error. At less than ± 100 mV from actual threshold, these switching points are guaranteed to lie between 0.8 and 2.0 V over the operating temperature range (V_{LC} = 0.0 V).

Test Circuits

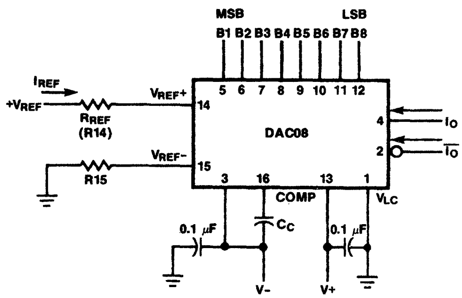
Figure 1 Settling Time Measurement



CR02681F

Typical Applications

Figure 2 Basic Positive Reference Operation



$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$
For all logic states

For fixed reference, TTL operation, typical values are:
V_{REF} = +10.000 V
R_{REF} = 5.000 k
$R_{15} \approx R_{REF}$
C_C = 0.01 µF
V_{LC} = 0 V (GROUND)

CR02691F

Typical Applications (Cont.)

Figure 3 Recommended Full Scale Adjustment Circuit

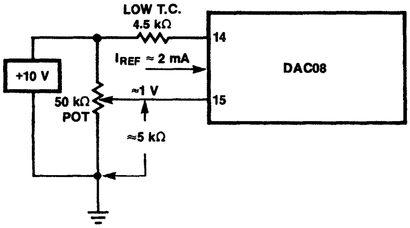
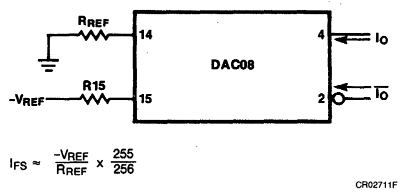


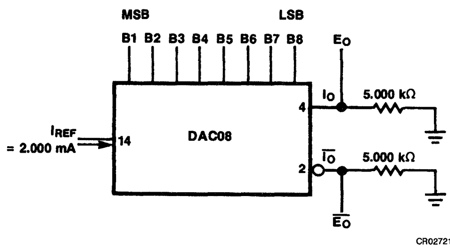
Figure 4 Basic Negative Reference Operation



$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

Note
R_{REF} sets I_{FS}; R15 is for bias current cancellation.

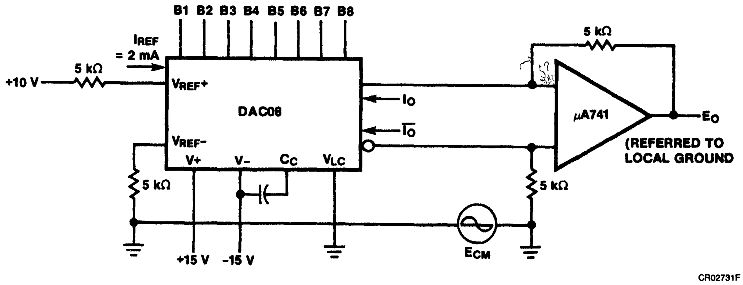
Figure 5 Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	.000	−9.960	.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	.008	−9.920	− .040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	− .040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	.000	1.992	.000	−9.960

Typical Applications (Cont.)

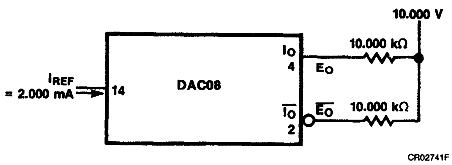
Figure 6 High Noise Immunity Current To Voltage Conversion



Provides isolation from ground loops
Symmetrical ± 10 V output
Useful within systems between boards
True complementary/differential current transmission
High speed analog signal transmission

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos Full Scale - LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-) Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	-9.920

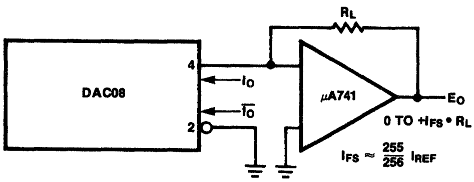
Figure 7 Basic Bipolar Output Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\bar{E}_O$
Pos Full Scale	1	1	1	1	1	1	1	1	- 9.920	+10.000
Pos Full Scale - LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+ 0.080
Zero Scale - LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
Neg Full Scale + LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	- 9.920

Typical Applications (Cont.)

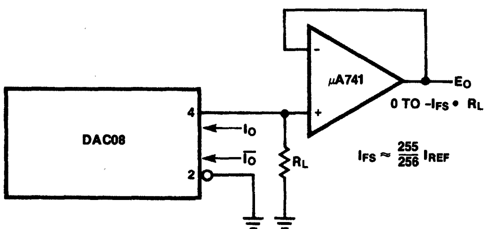
Figure 8 Positive Low Impedance Output Operation



For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Lead 2); connect I_O (Lead 4) to ground.

CR02751F

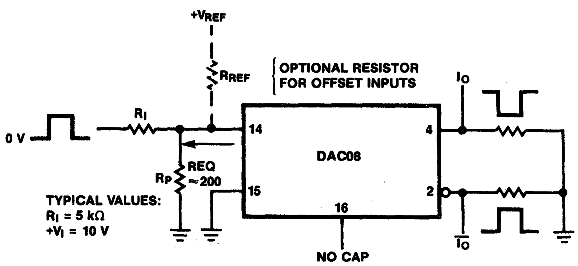
Figure 9 Negative Low Impedance Output Operation



For complementary output (operation as negative logic DAC), connect inverting input of Op-Amp to $\overline{I_O}$ (Lead 2); connect I_O (Lead 4) to ground.

CR02761F

Figure 10 Pulsed Reference Operation



CR02771F

Typical Applications (Cont.)

Figure 11 Accommodating Bipolar References

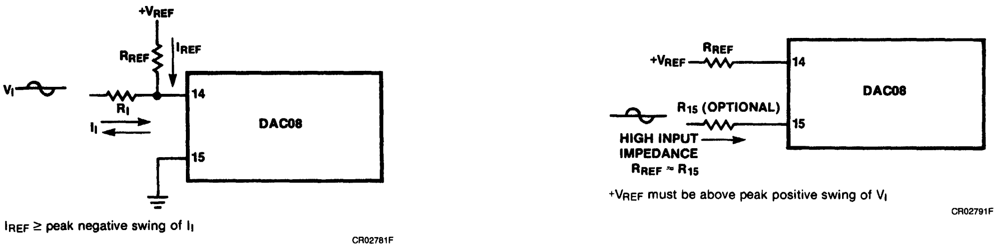
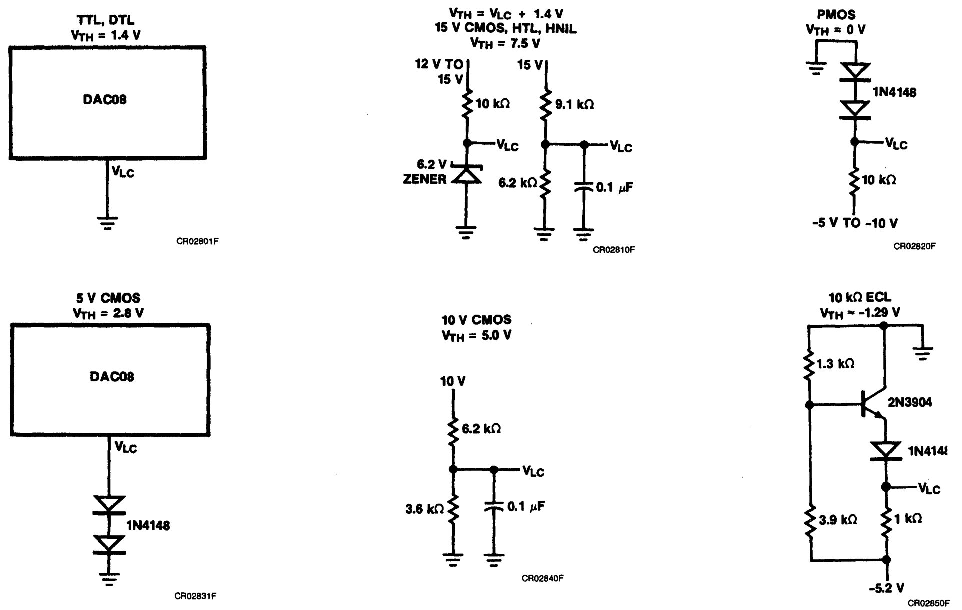


Figure 12 Interfacing With Various Logic Families



Note
Do not exceed negative logic input range of DAC

FAIRCHILD
A Schlumberger Company

DAC1408/1508 Series 8-Bit Multiplying D/A Converters

Linear Division Data Acquisition

Description

The DAC1408/1508 Series are monolithic 8-bit multiplying digital-to-analog converters constructed using the Fairchild Planar Epitaxial process. It is designed for use where the output current is a linear product of an 8-bit digital word and an analog input voltage. The DAC1408/1508 Series are lead-for-lead replacements for the MC 1408 and SSS 1408 devices.

- **Relative Accuracy ±0.19% Error Maximum DAC1408A**
- **7 And 6-Bit Accuracy Available DAC1408B, DAC1408C**
- **Fast Settling Time To 1/2 LSB — 85 ns**
- **Non-inverting Digital Inputs are TTL And CMOS Compatible**
- **Output Voltage Swing +0.5 V to −5.0 V**
- **High-speed Multiplying Input Slew Rate 4.0 mA/μs**
- **Standard Supply Voltages +5.0 V And −5.0 V To −15 V**
- **Low Full Scale Current Drift +10 ppm/°C Typically**
- **Low Power Consumption 33 mW at ±5 V**
- **Low Cost**

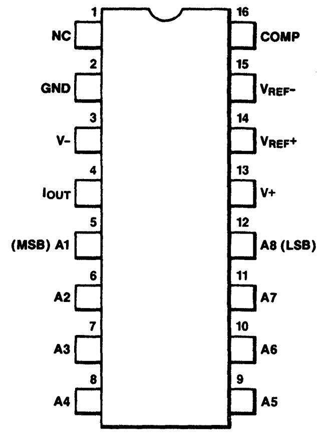
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (DAC1508M)	−55°C to +125°C
Commercial (DAC1408C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
V+	5.5 V
V−	−16.5 V
Digital Input Voltage (5 V to 12 V)	5.5 V
Applied Output Voltage	0.5 V to −5.2 V
Reference Current (I14)	5.0 mA
Reference Amplifier Inputs (V_{14}, V_{15})	5.5 V, −16.5 V

Notes

1. $T_{J\,Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Molded DIP at 8.3 mW/°C, the 16L-Ceramic DIP at 10 mw/°C.

Connection Diagram
16-Lead DIP
(Top View)

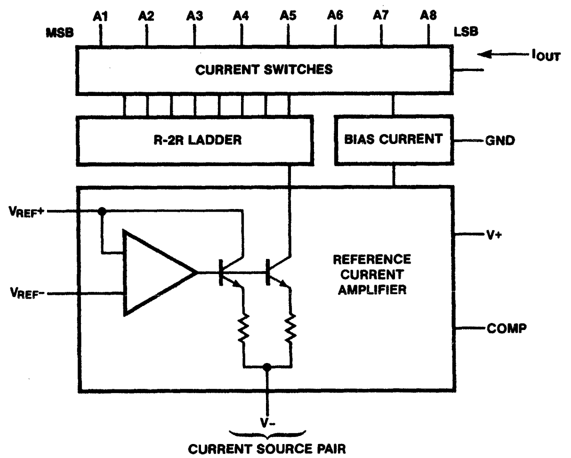


CD01180F

Order Information

Device Code	Package Code	Package Description
DAC1408ADC	7B	Ceramic DIP
DAC1408APC	9B	Molded DIP
DAC1408BDC	7B	Ceramic DIP
DAC1408BPC	9B	Molded DIP
DAC1408CDC	7B	Ceramic DIP
DAC1408CPC	9B	Molded DIP
DAC1508DM	7B	Ceramic DIP

Equivalent Circuit



EQ00461F

DAC1408/1508 Series

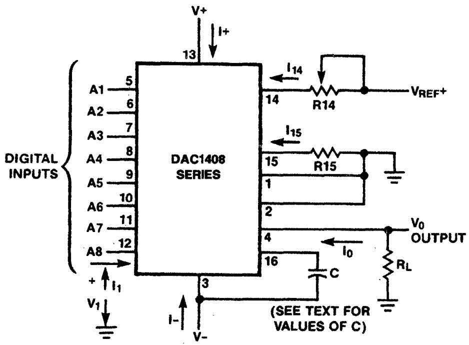
Electrical Characteristics T_A = 0°C to 70°C for the DAC1408, −55°C to +125°C for the DAC1508; V+ = +5.0 V, V− = −15 V, $V_{REF}/R14$ = 2.0 mA. All digital inputs at HIGH logic level.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	DAC1408A/DAC1508				±0.19	%
		DAC1408B[1]				±0.39	
		DAC1408C[1]				±0.78	
t_S	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C[2]			85	135	ns
t_{PLH}, t_{PHL}	Propagation Delay	T_A = 25°C			30	100	ns
TCI_O	Output Full Scale Current Drift				±20		ppm/°C
V_{IH}	Logic Input Voltage HIGH			2.0			V
V_{IL}	Logic Input Voltage LOW					0.8	
I_{IH}	Logic Input Current HIGH	V_{IH} = 5.0 V			0	0.04	mA
I_{IL}	Logic Input Current LOW	V_{IL} = 0.8 V			−0.4	−0.8	
I_{15}	Reference Input Bias Current				−1.0	−5.0	μA
I_{OR}	Output Current Range	V− = −5.0 V		0	2.0	2.1	mA
		V− = −6.0 to −15 V		0	2.0	4.2	
I_O	Output Current	V_{REF} = 2.000 V, R14 = 1.0 kΩ		1.9	1.99	2.1	mA
$I_{O\ Min}$	Output Current	All bits LOW			0	4.0	μA
V_{OC}	Output Voltage Compliance	$E_r \leqslant$ 0.19% at T_A = 25°C	V− = −5.0 V			−0.55, +0.4	V
			V− below −10 V			−5.0, +0.5	
dI/dt	Reference Current Slew Rate				4.0		mA/μs
PSRR (−)	Output Current Supply Sensitivity				0.5	2.7	μA/V
I+	Supply Current	All bits LOW			+13.5	+22	mA
I−					−7.5	−13	
V_R+	Power Supply Voltage Range	T_A = 25°C		+4.5	+5.0	+5.5	V
V_R−				−4.5	−15	−16.5	
P_c	Power Consumption	All bits LOW, V− = −5.0 V			105	170	mW
		All bits LOW, V− = −15 V			190	305	
		All bits HIGH, V− = −5.0 V			90		
		All bits HIGH, V− = −15 V			160		

Notes
1. All current switches are tested to guarantee at least 50% of rated output current.
2. All bits switched.

Test Circuits

Figure 1 Notation Definitions



Typical values: R14 = R15 = 1 k
V_{REF} = +20 V
C = 15 pF

V_1 and I_1 apply to inputs A1 thru A8

The resistor tied to lead 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

where $K \approx \frac{V_{REF}}{R14}$

and A_n = "1" if A_n is at HIGH level
A_n = "0" if A_n is at LOW level

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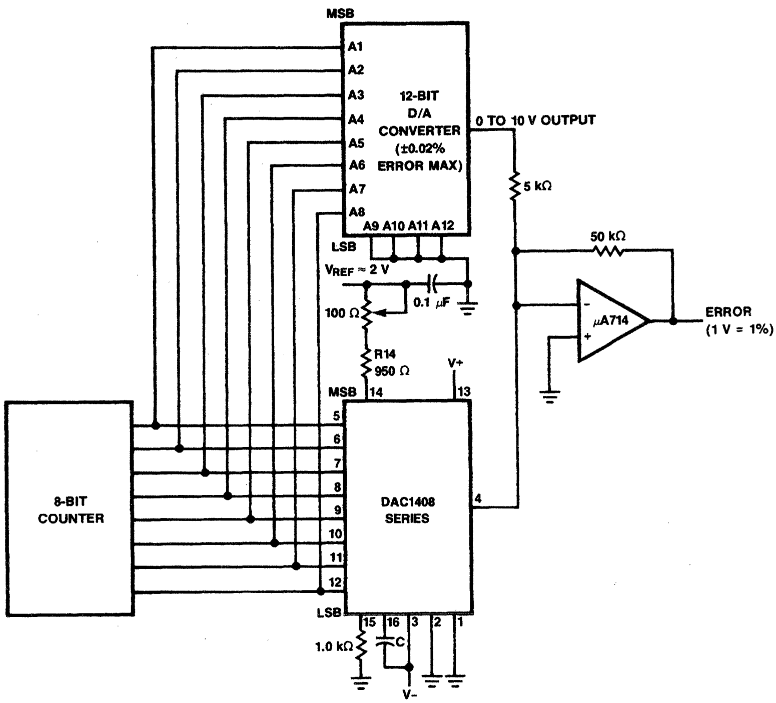
Figure 2 Relative Accuracy Test Circuit



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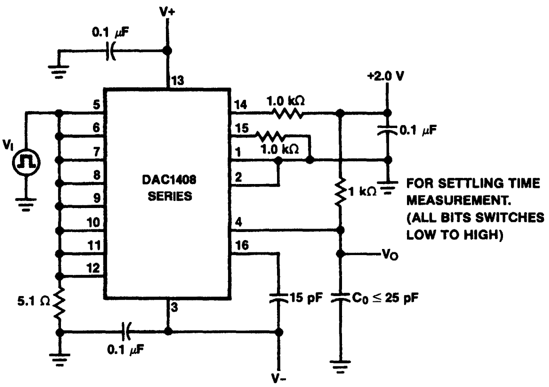
Test Circuits (Cont.)

Figure 3 Transient Response and Settling Time



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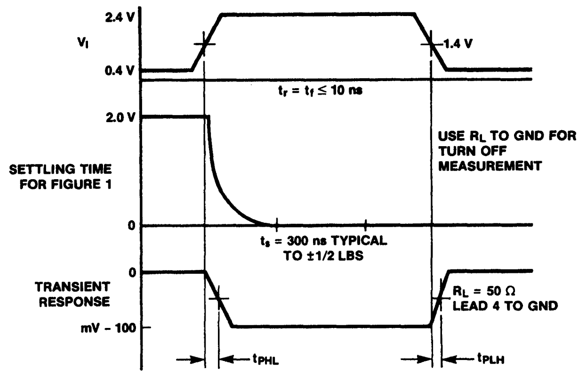

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Applications

- Tracking a/d Converters
- Successive Approximation a/d Converters
- 2 1/2 Digit Panel Meters and DVMs
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

Applications (Cont.)

Figure 4 Positive V_{REF}

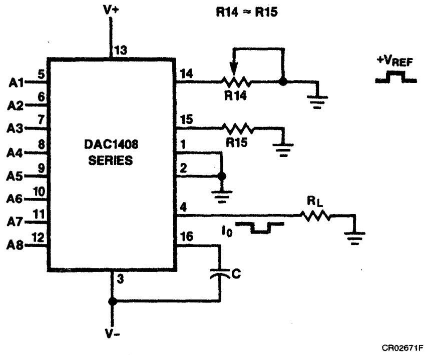


Figure 5 Negative V_{REF}

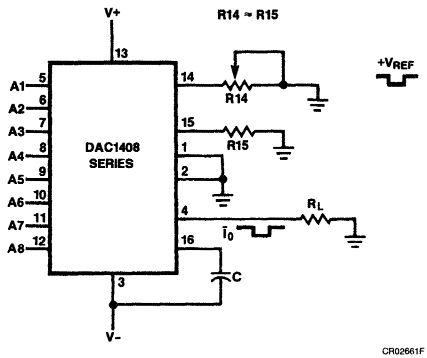
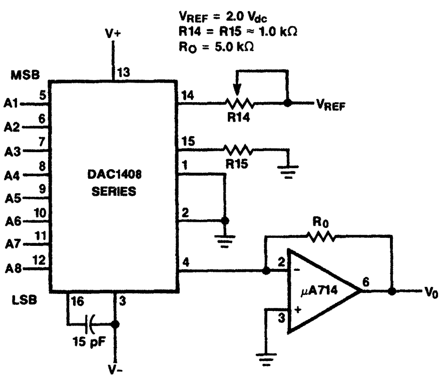


Figure 6 Use with Current-to-Voltage Converting OP AMP



Theoretical V_O

$$V_O = \frac{V_{REF}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{REF} R14 or R_O so that V_O with all digital inputs at HIGH level is equal to 9.961 Volts.

$$V_O = \frac{2\,V}{1\,k}(5\,k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\,V\,\frac{255}{256} = 9.961\,V$$

CR02861F

FAIRCHILD
A Schlumberger Company

μA565
Digital to Analog Converter

Description

The μA565 is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The μA565 chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried zener voltage reference to produce a high accuracy analog output current.

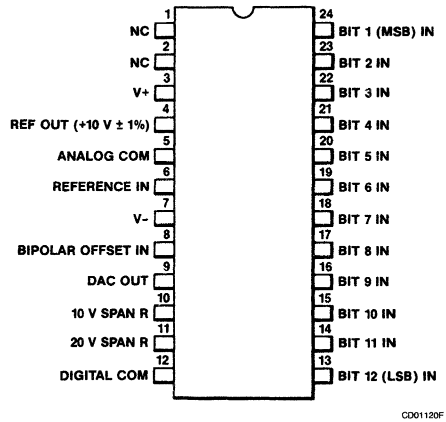
The internally buried zener reference is laser-trimmed to 10 V with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5 mA beyond that required for the reference and bipolar offset resistors.

The chip also contains additional SiCr thin film resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.

The μA565 is available in four performance grades. The μA565J and μA565K are specified for use over the 0 to 70°C temperature range, and the μA565S and μA565T are specified for the -55°C to +125°C range.

- **Single Chip Construction**
- **Very High Speed, Settles To 1/2 LSB In 200 ns**
- **Full Scale Switching Time — 30 ns**
- **High Stability Buried Zener Reference On Chip**
- **Monotonicity Guaranteed Over Temperature**
- **Linearity Guaranteed Over Temperature — 1/2 LSB Max (μA565K)**
- **Low Power, 225 mW Including Reference**

Connection Diagram
24-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA565SJM	7R	Ceramic (Side Brazed)
μA565TJM	7R	Ceramic (Side Brazed)
μA565JJC	7R	Ceramic (Side Brazed)
μA565KJC	7R	Ceramic (Side Brazed)

Absolute Maximum Ratings

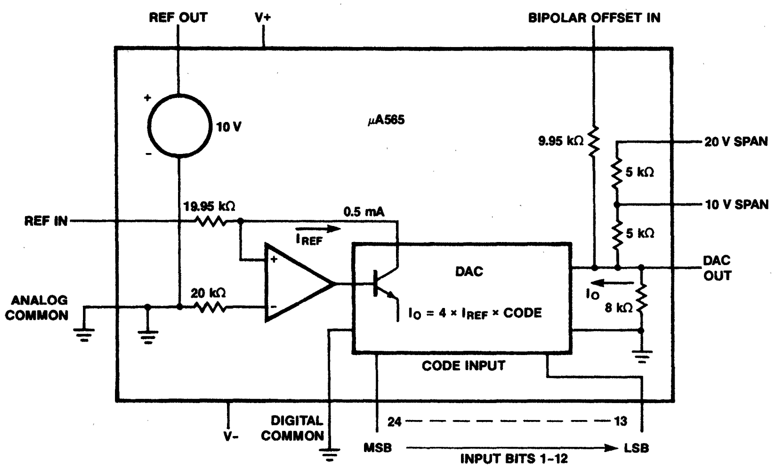
Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	
Extended (μA565M)	-55°C to +125°C
Commercial (μA565C)	0°C to +70°C
Lead Temperature	
Ceramic (Side Brazed)	
(soldering, 60s)	300°C
Internal Power Dissipation[1, 2]	
24L-Ceramic (Side Brazed)	2.50 W
V+ to Digital Common	0 V to +18 V
V– to Digital Common	0 V to –18 V

Analog Common to Digital Common	±1.0 V
Voltage on DAC Output (Lead 9)	-3.0 V to +12 V
Digital Inputs (Leads 13 to 24) to Digital Common	-1.0 V to +7.0 V
Ref In to Analog Common	±12 V
Bipolar Offset to Analog Common	±12 V
10 V Span R to Analog Common	±12 V
20 V Span R to Analog Common	±12 V
Ref Out	Indefinite Short to either Common Momentary Short to V+

Notes

1. $T_{J\,Max}$ = 175°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 16.7 mW/°C.

Block Diagram



μA565S/J and μA565T/K
Electrical Characteristics $T_A = +25°C$, V+ = +15 V, V− = −15 V, unless otherwise specified.[1]

Symbol	Characteristic		Condition	μA565S/J[1]			μA565T/K[1]			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	Data Input Voltage	Logic "1"	Bit ON	2.0		5.5	2.0		5.5	V
V_{IL}		Logic "0"	Bit OFF			0.8			0.8	
I_{IH}	Data Input Current	Logic "1"	Bit ON		120	260		120	260	μA
I_{IL}		Logic "0"	Bit OFF		35	75		35	75	
RESO	Resolution					12			12	Bits
I_{FS}	Output Current	Unipolar	All bits ON (Fig 1)	−1.6	−2.0	−2.4	−1.6	−2.0	−2.4	mA
		Bipolar	All bits ON or OFF (Fig 2)	± 0.8	± 1.0	± 1.2	± 0.8	± 1.0	± 1.2	
R_O	Output Resistance (exclusive of span resistors)			6.0	8.0	10	6.0	8.0	10	kΩ
I_{ZS}	Output Offset	Unipolar	(Fig 1)		0.01	0.05		0.01	0.02	% of FS
		Bipolar	$R_2 = 50\ \Omega$ fixed (Fig 2)		0.05	0.15		0.05	0.1	
C_O	Output Capacitance				25			25		pF
V_{OC}	Output Compliance Voltage		I_{Min} to I_{Max}	−1.5		+10	−1.5		+10	V
E_A	Accuracy (error relative to full scale)				± 1/4	± 1/2		± 1/8	± 1/4	LSB
					(0.006)	(0.012)		(0.003)	(0.006)	% of FS
			$T_{A\ Min}$ to $T_{A\ Max}$		± 1/2	± 3/4		± 1/4	± 1/2	LSB
					(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DNL	Differential Nonlinearity				± 1/2	± 3/4		± 1/4	± 1/2	LSB
			$T_{A\ Min}$ to $T_{A\ Max}$	Monotonicity Guaranteed			Monotonicity Guaranteed			
TC_{IZS}	Temperature Coefficient of Unipolar Zero		$T_{A\ Min}$ to $T_{A\ Max}$		1.0	2.0		1.0	2.0	ppm/°C
TC_{IZS}	Temperature Coefficient of Bipolar Zero		$T_{A\ Min}$ to $T_{A\ Max}$		5.0	10		5.0	10	ppm/°C
TC_{IFS}	Temperature Coefficient of Gain (Full Scale)		$T_{A\ Min}$ to $T_{A\ Max}$		15	30		10	20	ppm/°C
TC_{DNL}	Temperature Coefficient of Differential Nonlinearity		$T_{A\ Min}$ to $T_{A\ Max}$		2.0			2.0		ppm/°C
t_S	Settling Time to 1/2 LSB		All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns

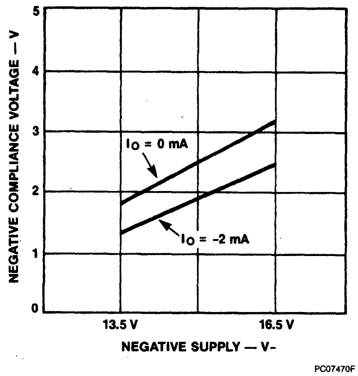
μA565S/J and μA565T/K (Cont.)
Electrical Characteristics $T_A = +25°C$, V+ = +15 V, V− = −15 V, unless otherwise specified.[1]

Symbol	Characteristic	Condition	μA565S/J[1]			μA565T/K[1]			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Full Scale Transition	10% to 90% Delay plus Rise Time		15	30		15	30	ns
t_{PHL}		90% to 10% Delay plus Fall Time		30	50		30	50	
I+	Power Requirements	V+ = +13.5 V to +16.5 V		3.0	5.0		3.0	5.0	mA
I−		V− = −13.5 V to −16.5 V		−12	−18		−12	−18	
PSS_{IFS}	Power Supply Sensitivity	V+ = +15 V, ± 10%		3.0	10		3.0	10	ppm of FS/%
		V− = −15 V, ± 10%		15	25		15	25	
POR	Programmable Output Range		0 to +5.0			0 to +5.0			V
			−2.5 to +2.5			−2.5 to +2.5			V
			0 to +10			0 to +10			V
			−5.0 to +5.0			−5.0 to +5.0			V
			−10 to +10			−10 to +10			V
I_{FS} R2	External Adjustments	Gain Error with Fixed 50 Ω Resistor for R2		± 0.1	± 0.25		± 0.1	± 0.25	% of FS
I_{ZS} R1		Bipolar Zero Error with Fixed 50 Ω Resistor for R1		± 0.05	± 0.15		± 0.05	± 0.1	
I_{FS} R2		Gain Adjustment Range	± 0.25			± 0.25			
I_{ZS} R1		Bipolar Zero Adjustment Range	± 0.15			± 0.15			
Z_I	Reference Input Impedance		15	20	25	15	20	25	kΩ
V_{REF}	Reference Output	Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
I_{REF}		Current (avail. for external loads)	1.5	2.5		1.5	2.5		mA
P_c	Power Consumption			225	345		225	345	mW

Note
1. $T_{A\,Min}$ and $T_{A\,Max}$ are 0°C and 70°C for J and K grade, and −55°C to +125°C for S and T grade.

Typical Performance Curve

Typical Negative Compliance Range vs Negative Supply



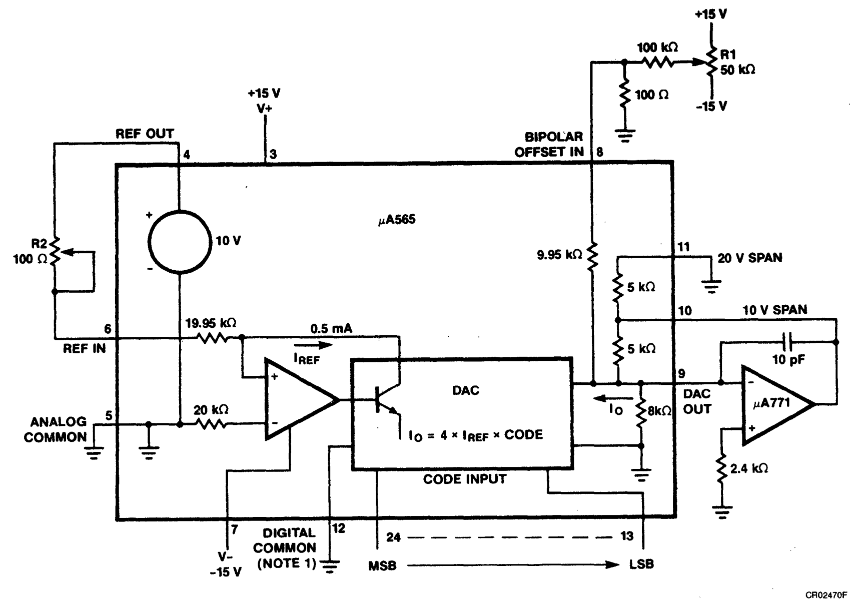
Typical Applications

Buffered Voltage

The standard current-to-voltage conversion connections using an operational amplifier are shown in *Figure 1* with the preferred trimming techniques. If a low offset operational amplifier (μA714L, μA725A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below ½ LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, typically the unipolar zero will be within ± ½ LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer will give a bipolar zero error typically within ± 2 LSB (0.05%).

The μA771 is recommended for buffered voltage output applications which require a settling time to ± ½ LSB of two microseconds. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

Figure 1 0 V to +10 V Unipolar Voltage Output



Note 1
Digital and analog common must have a common current return path.
*See typical applications continued for proper connections.

This unipolar configuration *(Figure 1)* will provide a unipolar 0 to +10 V output range. In this mode, the bipolar terminal, lead 8, should be grounded if not used for trimming.

Step I, Zero Adjust
Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1 LSB = 2.44 mV). In most cases this trim is not needed, but lead 8 should then be connected to lead 5.

Step II, Gain Adjust
Turn all bits ON and adjust 100 Ω gain trimmer, R2, until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a 120 Ω resistor in series with the gain resistor at lead 10 to the op amp output.

Figure 2 bipolar configuration, will provide a bipolar output voltage from −5.000 V to +4.9976 V, with positive full scale occurring with all bits ON (all "1"s).

Step I, Offset Adjust
Turn OFF all bits. Adjust 100 Ω trimmer R1, to give −5.000 V output.

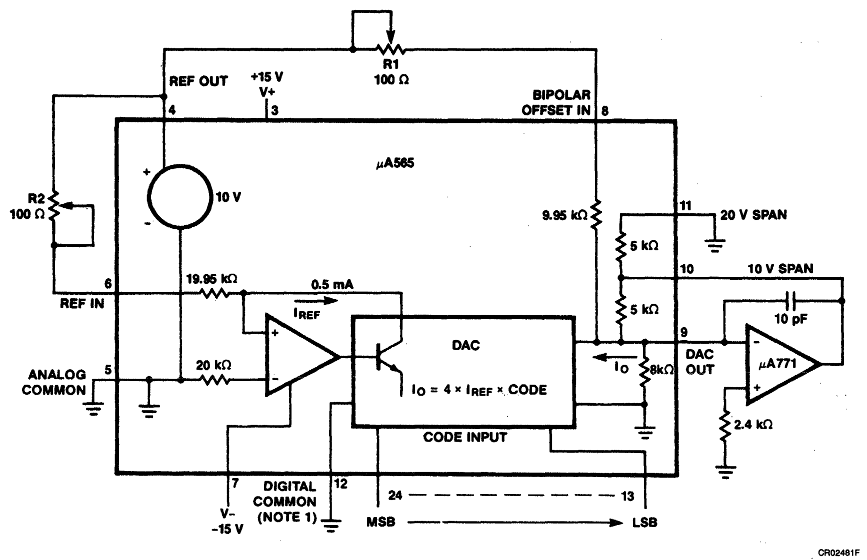
Step II, Gain Adjust
Turn ON all bits, adjust 100 Ω gain trimmer, R2, to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

The μA565 can also be easily configured for a unipolar 0 V to +5 V range or ±2.5 V and ±10 V bipolar ranges by using the additional 5 kΩ application resistor provided at the 20 V span R terminal, lead 11. For a 5 V span (0 to +5 or ±2.5), the two 5 kΩ resistors are used in parallel by shorting lead 11 to lead 9 and connecting lead 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 V range (20 V span) use the 5 kΩ resistors in series by connecting only lead 11 to the op amp output and the bipolar offset connected as shown. The ±10 V option is shown in *Figure 3*.

Internal/External Reference Use
The μA565 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the μA565 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) are done in this configuration.

Figure 2 ±5 V Bipolar Voltage Output



The μA565 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5 mA to REF IN and 1.0 mA to BIPOLAR OFFSET IN, if used). A minimum of 1.5 mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

Digital Input Considerations
The μA565 uses a standard positive true straight binary code for unipolar outputs (all "1"s give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all "0"s on the inputs, the output will go to negative full scale; with 100. . .00 (only the MSB on), the output will be 0.00 V; with all "1"s, the output will go to positive full scale.

The threshold of the digital input circuitry is set at 1.4 V and does not vary with supply voltage. The input lines can interface with any type of 5 V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4.* The input line can be modelled as a 30 kΩ resistance connected to −0.7 V rail.

Application of Analog and Digital Commons
The μA565 brings out separate analog and digital grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. Up to ±1.0 V can be tolerated between the ground lines without damage to the device. If the μA565 is to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog common at lead 5 is the ground reference point for the internal reference and is thus the "high quality" ground for the μA565: it should be connected directly to the analog reference point of the system. The digital common at lead 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If digital common contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

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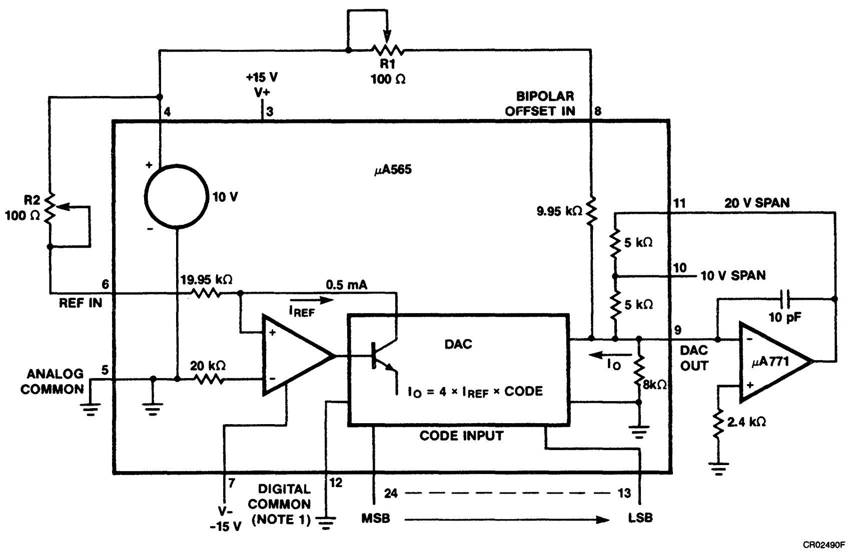
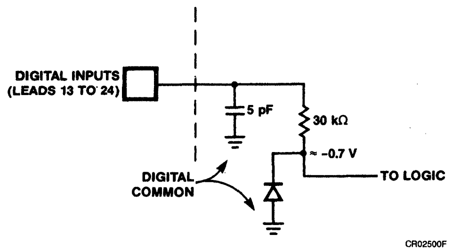
Figure 3 ±10 V Bipolar Voltage Output



Output Voltage Compliance

The μA565 has a typical output compliance range from −2 V to +10 V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply.

Figure 4 Equivalent Digital Input Circuit



μA571
Analog to Digital Converter

Linear Division Data Acquisition

Description

The μA571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers — all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25 μs.

The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.

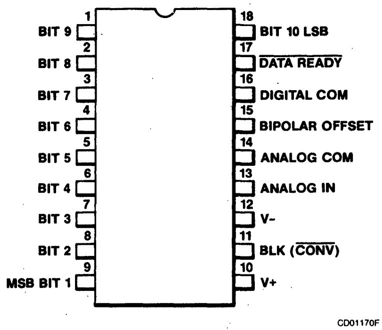
Operation is guaranteed with −15 V and +5 V to +15 V supplies. The device will also operate with a −12 V supply.

Operating on supplies of +5 V to ±15 V, the μA571 will accept analog inputs of 0 V to +10 V unipolar, or ±5 V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven LOW, the 3-state outputs will be open and a conversion starts. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go LOW and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input HIGH blanks the outputs and readies the device for the next conversion. The μA571 executes a true 10-bit conversion with no missing codes in approximately 25 μs.

The μA571 is available in two versions for the 0°C to +70°C temperature range, the μA571J and K. The μA571S guarantees 10-bit accuracy and no missing codes from −55°C to +125°C. All three grades are packaged in an 18-lead ceramic side brazed package.

- **Complete A/D Converter With Reference And Clock**
- **Fast Successive Approximation Conversion — 25 μs**
- **No Missing Codes Over Temperature**
- **Digital Multiplexing — 3-State Outputs**
- **18-Lead Ceramic Side Brazed Package**
- **Low Cost Monolithic Construction**

Connection Diagram
18-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA571SJM	FD	Ceramic (Side Brazed)
μA571JJC	FD	Ceramic (Side Brazed)
μA571KJC	FD	Ceramic (Side Brazed)

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	
Extended (μA571M)	−55°C to +125°C
Commercial (μA571C)	0°C to +70°C
Lead Temperature	
Ceramic (Side Brazed)	
(soldering, 60 s)	300°C
Internal Power Dissipation[1, 2]	
18L-Ceramic (Side Brazed)	1.74 W
V+ to Digital Common	0 to +7 V
V− to Digital Common	0 to −16.5 V
Analog Common to Digital Common	±1 V
Analog Input to Analog Common	±15 V
Control Inputs	0 to V+
Digital Outputs (Blank Mode)	0 to V+

Notes
1. $T_{J\ Max}$ = 175°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 11.6 mW/°C.

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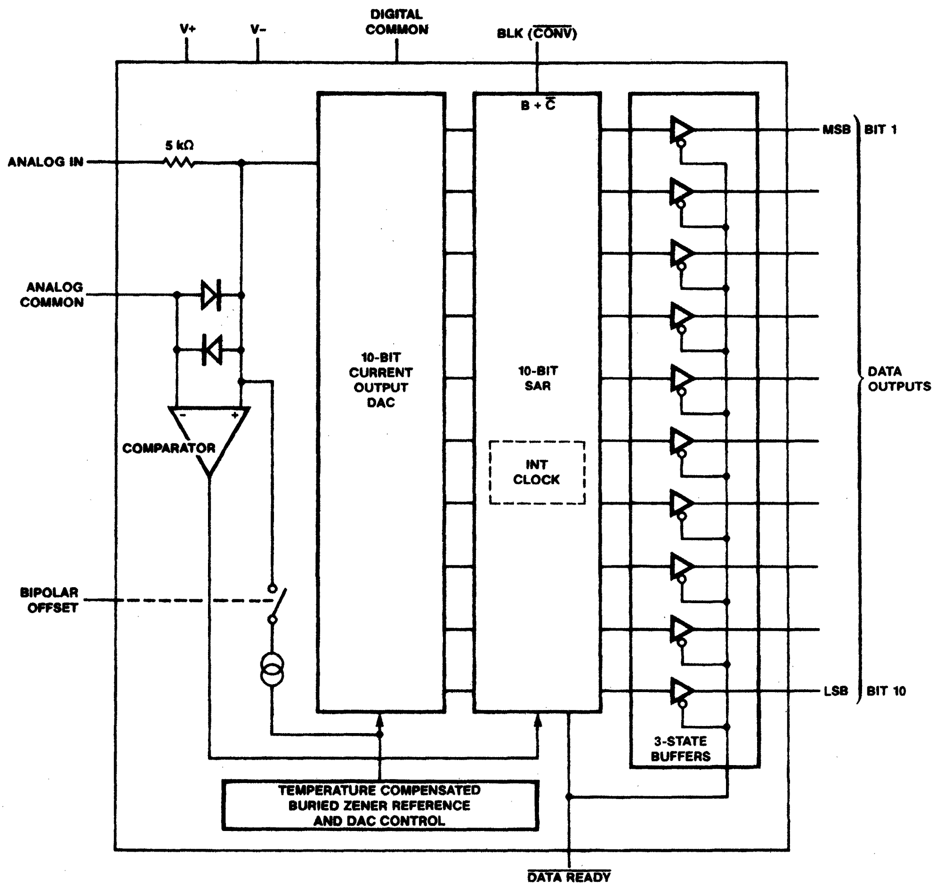
Block Diagram



μA571J and μA571K
Electrical Characteristics $T_A = 25°C$, $T_{A\ Min} = 0°C$, $T_{A\ Max} = 70°C$, V+ = +5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic		Condition	μA571J Min	μA571J Typ	μA571J Max	μA571K Min	μA571K Typ	μA571K Max	Units
RESO	Resolution				10			10		Bits
E_A	Relative Accuracy[1]					±1.0			±½	LSB
			$T_{A\ Min}$ to $T_{A\ Max}$			±1.0			±½	
V_{FS}	Full Scale Calibration[2]		With 15 Ω Resistor in Series with Analog Input		±2.0			±2.0		LSB
V_{ZS}	Unipolar Offset					±1.0			±½	LSB
	Bipolar Offset					±1.0			±½	
DNL	Differential Nonlinearity				10			10		Bits
			$T_{A\ Min}$ to $T_{A\ Max}$		9.0			10		
TC_{VZS}	Temperature Coefficient of Unipolar Offset		25°C to $T_{A\ Min}$ or $T_{A\ Max}$			±2.0			±1.0	LSB
						44			22	ppm/°C
TC_{VZS}	Temperature Coefficient of Bipolar Offset		25°C to $T_{A\ Min}$ or $T_{A\ Max}$			±2.0			±1.0	LSB
						44			22	ppm/°C
TC_{VFS}	Temperature Coefficient of Full Scale Calibration		25°C to $T_{A\ Min}$ or $T_{A\ Max}$, with 15 Ω Resistor or 50 Ω Trimmer			±4.0			±2.0	LSB
						88			44	ppm/°C
PSRR	Power Supply Rejection Ratio	CMOS Pos Supply	±13.5 V ⩽ V+ ⩽ +16.5 V						±1.0	LSB
		TTL Pos Supply	+4.5 V ⩽ V+ ⩽ 5.5 V			±2.0			±1.0	
		Negative Supply	−16.5 V ⩽ V+ ⩽ −13.5 V			±2.0			±1.0	
Z_I	Analog Input Impedance			3.0	5.0	7.0	3.0	5.0	7.0	kΩ
V_{IR}	Analog Input Ranges	Unipolar		0		10	0		10	V
		Bipolar		−5.0		+5.0	−5.0		+5.0	
OC	Output Coding	Unipolar		Positive True Binary			Positive True Binary			
		Bipolar		Positive True Offset Binary			Positive True Offset Binary			
I_{OL}	Output Sink Current		$V_O = 0.4$ V Max, $T_{A\ Min}$ to $T_{A\ Max}$	3.2			3.2			mA
I_{OH}	Output Source Current[3] (Bit Outputs)		$V_O = 2.4$ V Min, $T_{A\ Min}$ to $T_{A\ Max}$	0.5			0.5			mA
$B\overline{C}$ I_{IH}	Output Leakage When Blanked					±40			±40	μA

μA571J and μA571K (Cont.)

Electrical Characteristics $T_A = 25°C$, $T_{A\ Min} = 0°C$, $T_{A\ Max} = 70°C$, V+ = +5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic	Condition	μA571J Min	μA571J Typ	μA571J Max	μA571K Min	μA571K Typ	μA571K Max	Units
$\overline{BC}$ I_{IL}	Blank & Convert Input	$0\ V \leqslant V_I \leqslant V+$			40			40	μA
V_{IH}	Blank-Logic "1"		2.0			2.0			V
V_{IL}	Convert-Logic "0"				0.8			0.8	V
t_{CONV}	Conversion Time		15	25	40	15	25	40	μs
V+	Operating Range		+4.5		+5.5	+4.5		+16.5	V
V−			−12		−16.5	−12		−16.5	
I_{BLK}	Operating Current-Blank Mode	V+ = +5.0 V		2.0	10		2.0	10	mA
		V+ = +15 V		5.0	10		5.0	10	
		V− = −15 V		9.0	15		9.0	15	
I_{CONV}	Operating Current-Convert Mode	V+ = +5.0 V		5.0			5.0		mA
		V+ = +15 V		10			10		
		V− = −15 V		10			10		

μA571S

Electrical Characteristics $T_A = 25°C$, $T_{A\ Min} = -55°C$, $T_{A\ Max} = 125°C$, V+ = +5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic	Condition	μA571S Min	μA571S Typ	μA571S Max	Units
RESO	Resolution			10		Bits
E_A	Relative Accuracy[1]				±1.0	LSB
		$T_{A\ Min}$ to $T_{A\ Max}$			±1.0	
V_{FS}	Full Scale Calibration[2]	With 15 Ω Resistor in Series with Analog Input		±2.0		LSB
V_{ZS}	Unipolar Offset				±1.0	LSB
	Bipolar Offset				±1.0	
DNL	Differential Nonlinearity			10		Bits
		$T_{A\ Min}$ to $T_{A\ Max}$		10		
TC_{VZS}	Temperature Coefficient of Unipolar Offset	25°C to $T_{A\ Min}$ or $T_{A\ Max}$			±2.0	LSB
					20	ppm/°C
TC_{VZS}	Temperature Coefficient of Bipolar Offset	25°C to $T_{A\ Min}$ or $T_{A\ Max}$			±2.0	LSB
					20	ppm/°C

μA571S (Cont.)

Electrical Characteristics $T_A = 25°C$, $T_{A\ Min} = -55°C$, $T_{A\ Max} = 125°C$, V+ = +5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic		Condition	μA571S Min	μA571S Typ	μA571S Max	Units
TC_{VFS}	Temperature Coefficient of Full Scale Calibration		25°C to $T_{A\ Min}$ or $T_{A\ Max}$, with 15 Ω Fixed Resistor or 50 Ω Trimmer			±5.0	LSB
						50	ppm/°C
PSRR	Power Supply Rejection Ratio	TTL Pos Supply	+4.5 V ≤ V+ ≤ 5.5 V			±2.0	LSB
		Neg Supply	−16.5 V ≤ V+ ≤ −13.5 V			±2.0	
Z_I	Analog Input Impedance			3.0	5.0	7.0	kΩ
V_{IR}	Analog Input Ranges	Unipolar		0		10	V
		Bipolar		−5.0		+5.0	
OC	Output Coding	Unipolar		Positive True Binary			
		Bipolar		Positive True Offset Binary			
I_{OL}	Output Sink Current		$V_O = 0.4$ V Max, $T_{A\ Min}$ to $T_{A\ Max}$	3.2			mA
I_{OH}	Output Source Current (Bit Outputs)[3]		$V_O = 2.4$ V Min, $T_{A\ Min}$ to $T_{A\ Max}$	0.5			mA
$B\overline{C}\ I_{IH}$	Output Leakage When Blanked					±40	μA
$B\overline{C}\ I_{IL}$	Blank & Convert Input					±40	μA
V_{IH}	Blank-Logic "1"			2.0			V
V_{IL}	Convert-Logic "0"					0.8	V
t_{CONV}	Conversion Time			15	25	40	μs
V+	Operating Range			+4.5		+5.5	V
V−				−12		−16.5	
I_{BLK}	Operating Current-Blank Mode		V+ = +5.0 V		2.0	10	mA
			V+ = +15 V		5.0	10	
			V− = −15 V		9.0	15	
I_{CONV}	Operating Current-Convert Mode		V+ = +5.0 V		5.0		mA
			V+ = +15 V		10		
			V− = −15 V		10		

Notes

1. Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from zero to the full scale of the device.
2. Full scale calibration is guaranteed trimmable to zero with an external 50 Ω potentiometer in place of the 15 Ω fixed resistor. Full scale is defined as 10 V minus 1 LSB, or 9.990 V.
3. The data output lines have active pull-ups to source 0.5 mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

Typical Applications

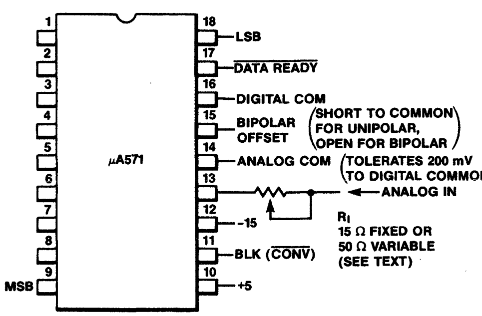
Standard μA571 Operation

The μA571 contains all the active components required to perform a complete A/D conversion. For most situations, all that is necessary is connection of the power supply (+5.0 V and −15 V), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The connection diagram is shown in *Figure 1.*

Full Scale Calibration

The 5.0 kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC — plus about 0.3% — when a full scale analog input voltage of 9.990 V (10 V — 1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 V full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to lead 13. Typical full scale calibration error will then be about ±2 LSB or ±0.2%. If the more precise calibration is desired, a 50 Ω trimmer should be used instead. Set the analog input at 9.990 V, and set their trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766 mV. If a nominal full scale of 10.24 V is desired (which makes the LSB exactly 10.00 mV), a 100 Ω resistor in series with a 100 Ω trimmer (or a 200 Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5 kΩ.

Figure 1 Standard μA571 Connections (Top View)



Bipolar Operation

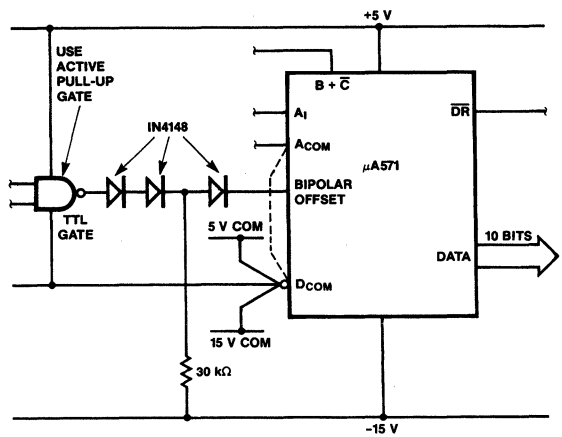
The standard unipolar 0 V to +10 V range is obtained by shorting the bipolar offset control lead to digital common. If the lead is left open, the bipolar offset current will be switched into the comparator summing node, giving a −5 V to +5 V range with an offset binary output code. (−5.00 V_I will give a 10-bit code of 0000000000; an input of 0.00 V results in an output code of 1000000000 and 4.99 V at the input yields the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in *Figure 2.*

Common Mode Range

The μA571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200 mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2.0 mA during a conversion. In addition, a static current of about 2.0 mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1.0 mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

Figure 2 Bipolar Offset Controlled by Logic Gate



Gate output = 1 unipolar 0 to 10 V input range
Gate output = 0 bipolar ±5 V input range

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The absolute maximum voltage rating between the two commons is ±1.0 V. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

Zero Offset

The apparent zero point of the μA571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. *Figure 3* illustrates two methods of providing this offset. *Figure 3A* shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

Figure 4 shows the nominal transfer curve near zero for a μA571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in *Figure 3b.* At balance (after a conversion) approximately 2.0 mA flows into the Analog Common terminal. A 2.7 Ω resistor is series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2.0 mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5.0 Ω potentiometer (connected as a rheostat) can be used as R2. Additional negative offset range may be obtained by using larger values of

Figure 3a Zero Offset ADJ ±3-Bit Range

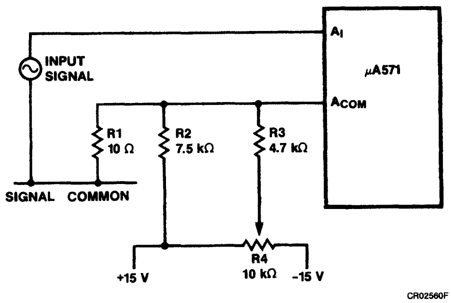
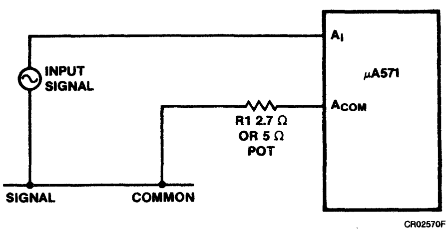


Figure 3b ½-Bit Zero Offset

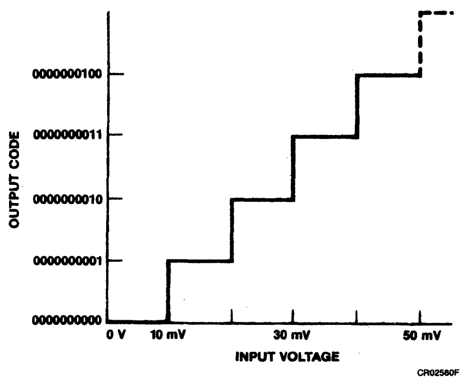


Note

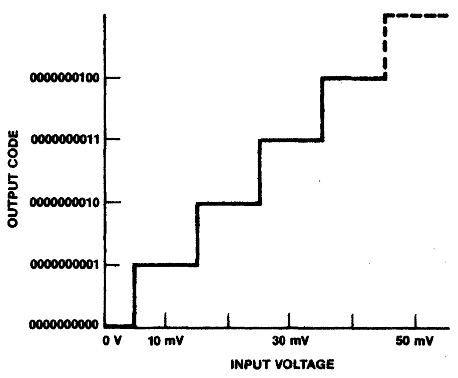
During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.

Figure 4 μA571 Transfer Curve — Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766 mV)

Nominal Characteristics referred to Analog Common



Offset Characteristics with 2.7 in series with Analog Common



R2. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½ LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 V.

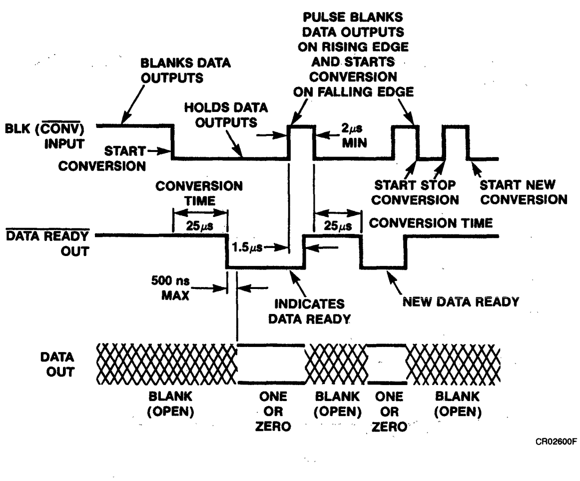
Control and Timing of the μA571

There are several important timing and control features on the μA571 which must be understood precisely to allow optimum interface to microprocessor or other types of control systems. All of these features are shown in the timing diagram in *Figure 5.*

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{C}$) line is held HIGH, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be HIGH. This mode is the lowest power state of the device (typically 150 mW). When the B & $\overline{C}$ line is brought LOW, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete (typically 25 μs), the $\overline{\text{DR}}$ line goes LOW, and within 500 ns, the data lines become active with the new data.

About 1.5 μs after the B & $\overline{C}$ line is again brought HIGH, the $\overline{\text{DR}}$ line will go HIGH and the data lines will go open. When the B & $\overline{C}$ line is again brought LOW, a new conversion will begin. The minimum pulse width for the B & $\overline{C}$ line to blank previous data and start a new conversion is 2.0 μs. If the B & $\overline{C}$ line is brought HIGH during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2.0 μs or longer pulse is applied to the B & $\overline{C}$ line during a conversion, the converter will clear and start a new conversion cycle.

Figure 5 μA571 Timing and Control Sequence



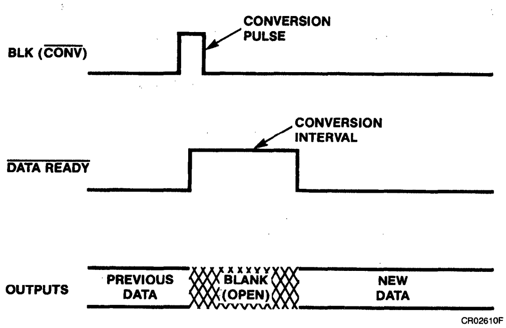
Control Modes with BLANK and $\overline{\text{CONVERT}}$

The timing sequence of the μA571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode

In this mode, data is present at the output of the converter at all times except when conversion is taking place. *Figure 6* illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally LOW and conversions are triggered by a positive pulse.

Figure 6 Convert Pulse Mode

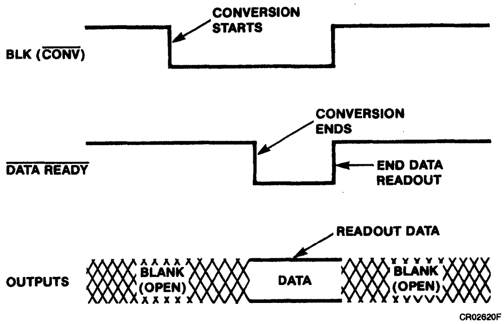


Multiplex Mode

In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing shown in *Figure 7.*

This operating mode allows multiple μA571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held HIGH to keep the outputs blanked. A single μA571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven LOW and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going LOW, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several μA571's are multiplexed in sequence, a new conversion may be started in one μA571 while data is being read from another. As long as the data is read and the first μA571 is cleared within 15 μs after the start of conversion of the second μA571, no data overlap will occur.

Figure 7 Multiplex Mode



FAIRCHILD

A Schlumberger Company

μA9650
4-Bit Current Source

Description

The μA9650 is a high speed 4-bit precision current source, intended for use in D/A and A/D converters with up to 12-bit accuracy. It is constructed on a single silicon chip, using the Fairchild Planar Epitaxial process and consists of a reference transistor and four logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible under all temperature and supply conditions. A clamp circuit is provided to prevent turn-on latch up on the reference input.

- **200 ns Settling Time (12 ± 1/2 LSB)**
- **Variable Bit Currents**
- **Reference Compensation**
- **TTL Compatible**

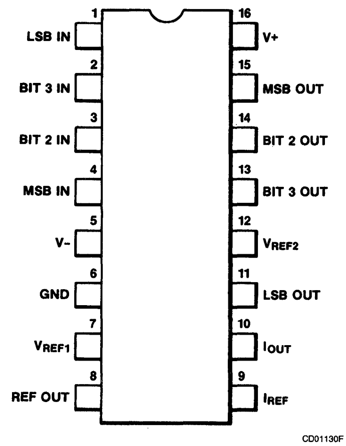
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
Logic Input Voltage	+5.5 V
V+	+7 V
V–	-18 V
MSB Current	2.0 mA
V_{REF} Inputs	+7 V to V–
Output (V_{REF} voltage $\geqslant$-7.0 V)	+18 V to V_{REF}

Notes

1. $T_{J\ MAX}$ = 175°C.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW°C.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA96501DC	6B	Ceramic DIP
μA96502DC	6B	Ceramic DIP
μA96503DC	6B	Ceramic DIP

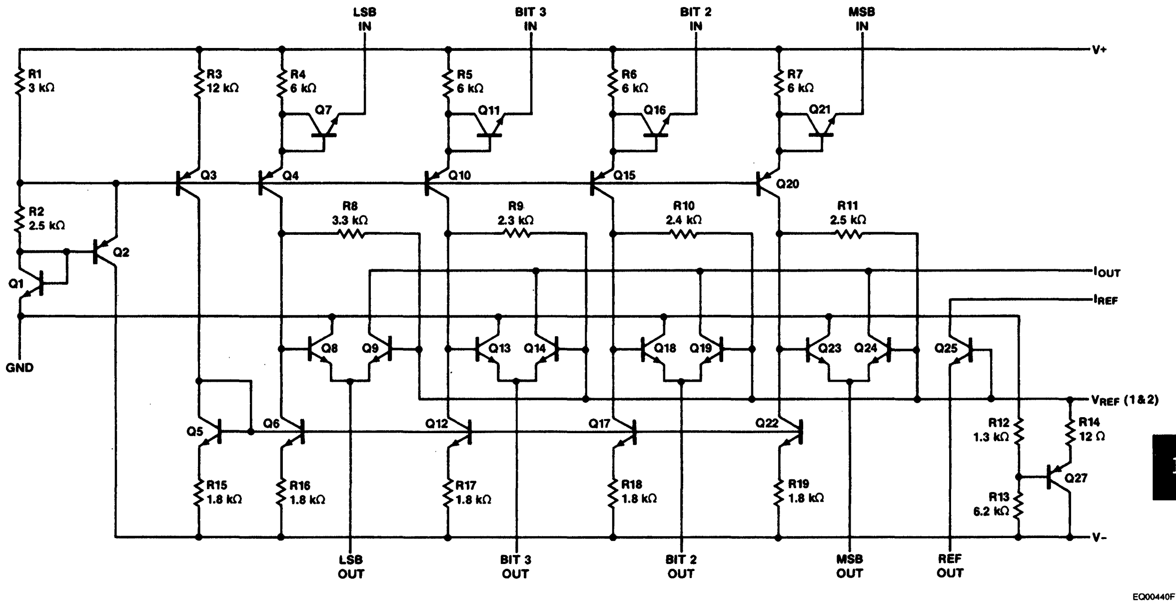
Truth Table

Logic Input	Nominal Output Current (mA)	Logic Input	Nominal Output Current (mA)
0000	1.875	1000	0.875
0001	1.750	1001	0.750
0010	1.625	1010	0.625
0011	1.500	1011	0.500
0100	1.375	1100	0.375
0101	1.250	1101	0.250
0110	1.125	1110	0.125
0111	1.000	1111	0.000

μA9650 Kits Required to Build D/A-A/D Converters

Temperature Range	Type And No. of Unit		
0°C to +70°C	**96501C**	**96502C**	**96503C**
Accuracy to:			
8 Bits	0	0	2
10 Bits	0	1	2
12 Bits	1	1	1

Equivalent Circuit



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μA96501C • μA96502C • μA96503C
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, V− = −15 V, unless otherwise specified.

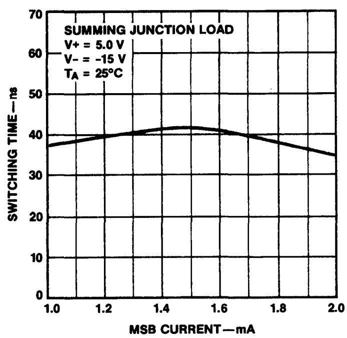
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
E_A	Accuracy	(μA96501C)			±0.01	% of IFS
		(μA96502C)			±0.05	
		(μA96503C)			±0.2	
I_{FSER}	Full Scale Output Current Error	(μA96501C)			±0.1	%
		(μA96502C)			±0.2	
		(μA96503C)			±0.4	
PSC_{IFS}	Power Supply Coefficient of Full Scale Output Current	(μA96501C)			±0.003	%/V
		(μA96502C, μA96503C)			±0.012	
V_{BE}	V_{BE} Range			620		mV
h_{FE}	h_{FE} of Reference Transistor			1000		
Z_O	Output Impedance	All Bits On		5.0		MΩ
The following specifications apply for $0°C \leqslant T_A \leqslant 70°C$						
E_A	Accuracy	(μA96501C)			±0.025	% of IFS
		(μA96502C)			±0.1	
		(μA96503C)			±0.3	
I_{FSER}	Full Scale Output Current Error	(μA96501C)			0.2	%
		(μA96502C)			0.3	
		(μA96503C)			0.6	
PSS_{IFS}	Power Supply Sensitivity of Full Scale Output Current	(μA96501C)			±0.006	%/V
		(μA96502C, μA96503C)			±0.024	
V_{IL}	Input Voltage LOW	Each Bit On			0.8	V
V_{IH}	Input Voltage HIGH	Each Bit Off	2.0			V
I_{IL}	Input Current LOW	$V_{IL} = 0.4$ V			−1.6	mA
I_{IH}	Input Current HIGH	$V_{IH} = 2.4$ V			40	μA
I_O	Output Current	Bit 1 (MSB)		1.0	2.0	mA
		Bit 2		0.5	1.0	
		Bit 3		0.25	0.5	
		Bit 4 (LSB)		0.125	0.25	
I_O	Output Current	All Bits Off				nA
		(μA96501C)		5.0	250	
		(μA96502C, μA96503C)		5.0	500	
V_O	Output Voltage	Feeding Op Amp Summing Junction		0		V
		Resistive Load	−4.0		V+	
I_R	Reference Current	Using Compensation Transistor		1.0		mA

μA96501C • μA96502C • μA96503C (Cont.)
Electrical Characteristics $T_A = 25°C$, V+ = 5.0 V, V− = −15 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{VR}	V_{REF} Current			±1.0	±2.2	mA
I_{LIM}	Reference Limit Current	$V_{REF} = 0$ V	20		75	mA
I+	Positive Supply Current	(μA96501C, μA96502C)			8.0	mA
		(μA96503C)			10	
I−	Negative Supply Current	(μA96501C, μA96502C)			−11	mA
		(μA96503C)			−15	

Typical Performance Curves

Switching Time vs MSB Current (50% In to 10% Out)



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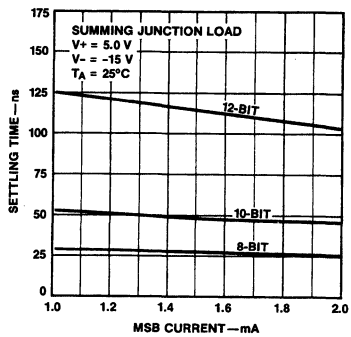
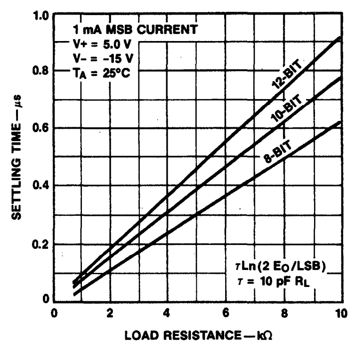
Output Current Settling Time vs MSB Current (0 to FSI Output ± ½ LSB)



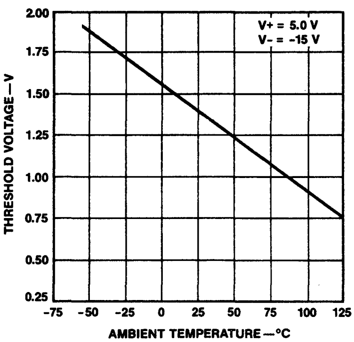
PC07490F

Settling Time vs Load Resistance (0 to FSI Output ± ½ LSB)



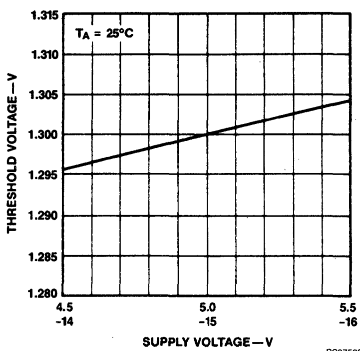
PC07501F

Input Logic Threshold Voltage vs Ambient Temperature



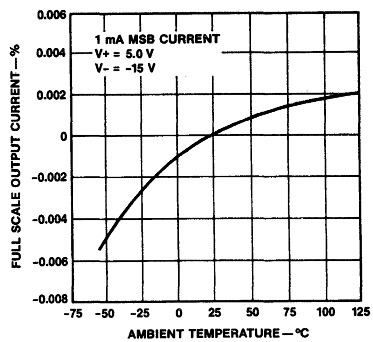
PC07510F

Input Logic Threshold Voltage vs Supply Voltage



PC07520F

Full Scale Output Current Drift vs Ambient Temperature



PC07530F

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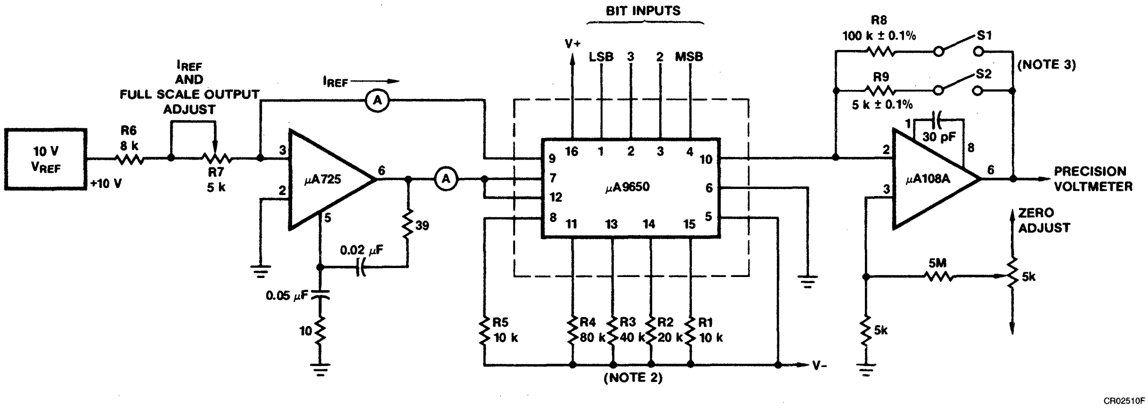
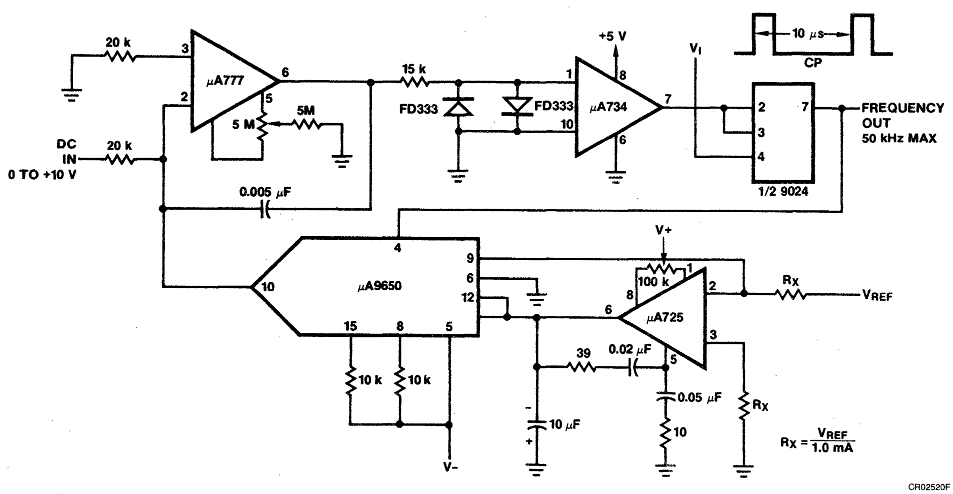
Typical DC Test Circuit (Note 1)



Notes
1. All resistor values in ohms.
2. Required resistor ratio tolerances of R_1–R_5 to test the various grades are as follows: μA96501C, R_5 to R_2 to R_1 — ±0.005%, R_3 to R_1 — ±0.01%, R_4 to R_1 — ±0.02%. μA96502C, R_5 to R_2 to R_1 — ±0.025%, R_3 to R_1 — ±0.05%, R_4 to R_1 — ±0.1%. μA96503C, R_5 to R_2 to R_1 — ±0.1%, R_3 to R_1 — ±0.2%, R_4 to R_1 — ±0.4%.
3. S_1 closed and S_2 open for output current (all Bits off) tests only.

Typical Applications (Note 1)

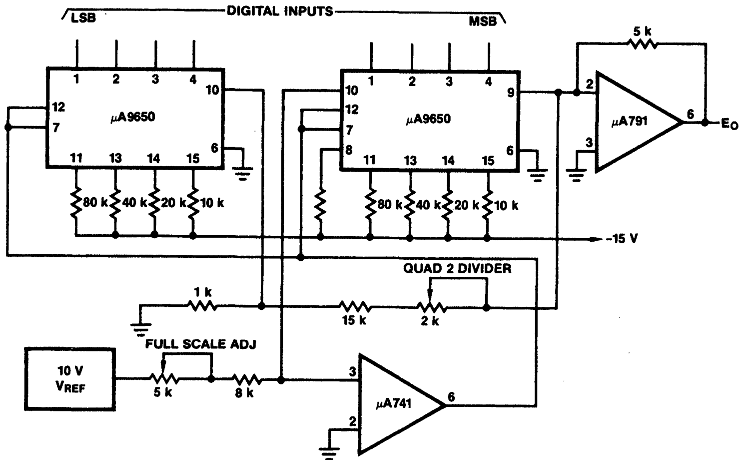
Voltage to Frequency Converter



Note
1. All resistor values in ohms.

Typical Applications (Cont.) (Note 1)

8-Bit D/A Converter



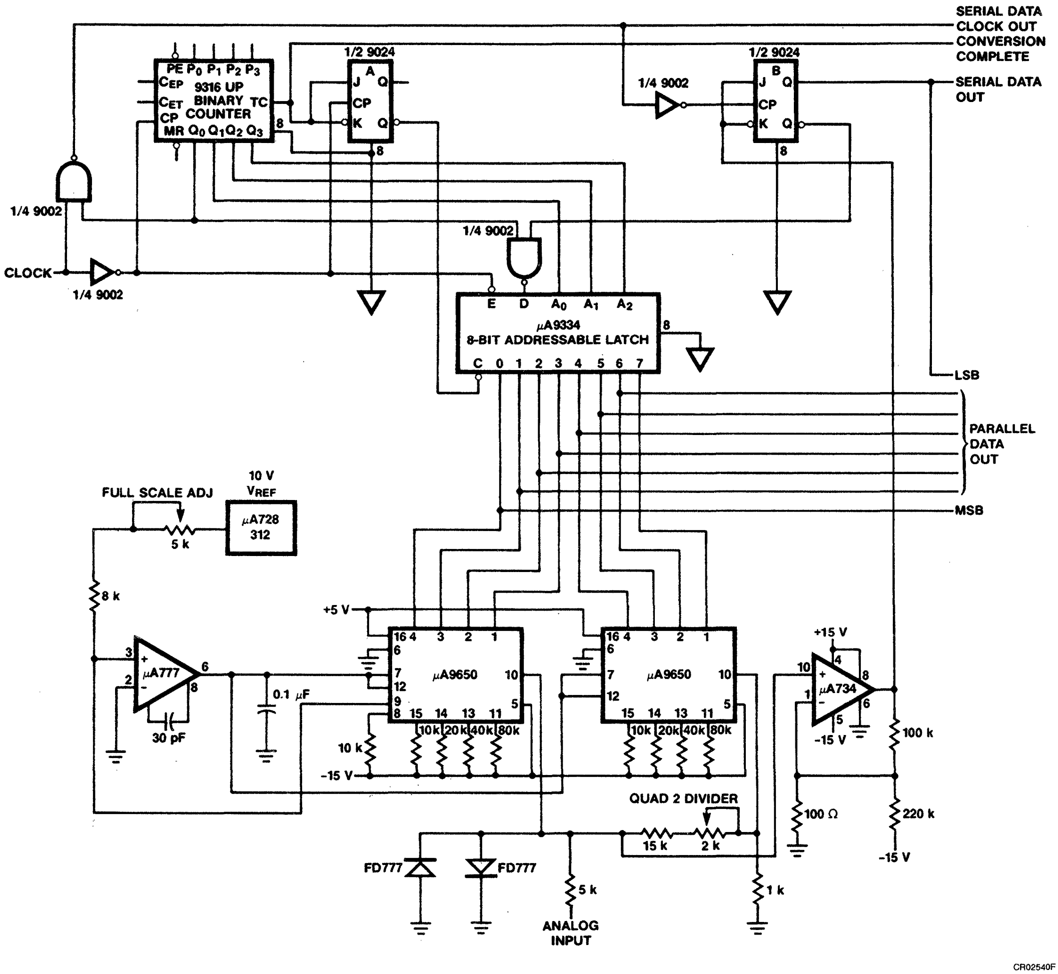
CR02530F

Note

1. All resistor values in ohms.

Typical Applications (Cont.) (Note 1 and 2)

8-Bit A/D Converter



Notes

1. All resistor values in ohms.
2. Digital GND indicated by
   Analog GND indicated by

FAIRCHILD

A Schlumberger Company

μA2240 Programmable Timer/Counter

Linear Division Special Functions

Description

The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital systems. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **Accurate Timing From Microseconds To Days**
- **Programmable Delays From 1 RC To 255 RC**
- **TTL, DTL And CMOS Compatible Outputs**
- **Timing Directly Proportional To RC Time Constant**
- **High Accuracy**
- **External Sync And Modulation Capability**
- **Wide Supply Voltage Range**
- **Excellent Supply Voltage Rejection**

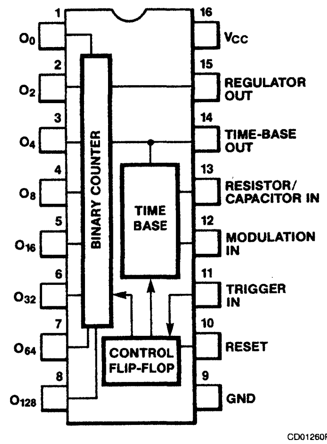
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5.0 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2240DC	7B	Ceramic DIP
μA2240PC	9B	Molded DIP

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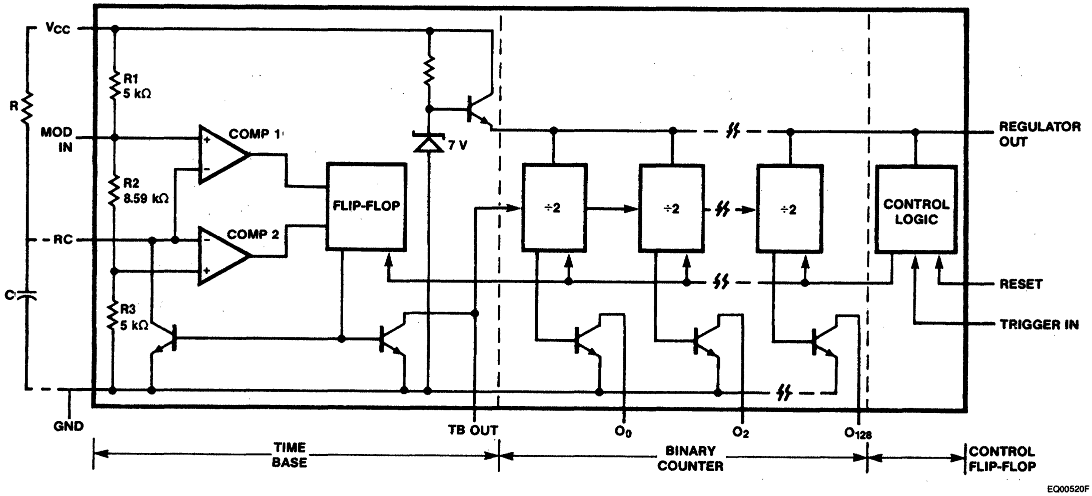
Block Diagram



μA2240C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, R = 10 kΩ, C = 0.1 μF, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
General Characteristic						
V_{CC}	Supply Voltage	For $V_{CC} \leq 4.5$ V, Short Lead 15 to Lead 16	4.0		15	V
I_{CC}	Supply Current, Total Circuit	$V_{CC} = 5.0$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V		4.0	7.0	mA
		$V_{CC} = 15$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V		13	18	
	Supply Current, Counter Only			1.5		
V_{REG}	Regulator Output	Measured at Lead 15, $V_{CC} = 5.0$ V	3.9	4.4		V
		Measured at Lead 15, $V_{CC} = 15$ V	5.8	6.3	6.8	
Time-Base						
t_{ACC}	Timing Accuracy[1]	$V_{RS} = 0$, $V_{TR} = 5.0$ V		3.5	5.0	%
$\Delta t/\Delta T$	Temperature Drift	$0°C \leq T_J \leq 75°C$, $V_{CC} = 5.0$ V		200		ppm/°C
		$0°C \leq T_J \leq 75°C$, $V_{CC} = 15$ V		80		
$\Delta t/\Delta V$	Supply Drift	$V_{CC} \geq 8.0$ V (See Performance Curves)		0.08	0.3	%/V
f_{Max}	Max Frequency	R = 1.0 kΩ, C = 0.007 μF		130		kHz
V_{MOD}	Modulation Voltage Level	Measured at Lead 12, $V_{CC} = 5.0$ V	2.80	3.50	4.20	V
		Measured at Lead 12, $V_{CC} = 15$ V		10.5		
R_T	Recommended Range of Timing Components Timing Resistor	(See Performance Curves)	0.001		10	MΩ

μA2240C (Cont.)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, R = 10 kΩ, C = 0.1 μF, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
C_T	Timing Capacitor		0.01		1000	μF
Trigger/Reset Controls						
V_{TR}	Trigger Threshold	Measured at Lead 11, $V_{RS} = 0$ V		1.4	2.0	V
I_{TR}	Trigger Current	$V_{RS} = 0$ V, $V_{TR} = 2.0$ V		10		μA
Z_T	Trigger Impedance			25		kΩ
t_{RSPT}	Trigger Response Time[2]			1.0		μs
V_{RS}	Reset Threshold	Measured at Lead 10, $V_{TR} = 0$ V		1.4	2.0	V
I_R	Reset Current	$V_{TR} = 0$ V, $V_{RS} = 2.0$ V		10		μA
Z_R	Reset Impedance			25		kΩ
t_{RSPT}	Reset Response Time[2]			0.8		μs
Counter						
TR_{Max}	Max Toggle Rate	Measured at Lead 14 $V_{RS} = 0$ V, $V_{TR} = 5.0$ V		1.5		MHz
Z_I	Input Impedance			20		kΩ
V_{TH}	Input Threshold		1.0	1.4		V
t_r	Output Rise Time	Measured at Leads 1 through 8 $R_L = 3.0$ kΩ, $C_L = 10$ pF		180		ns
t_f	Fall Time			180		
I_{O-}	Sink Current	$V_{OL} \leqslant 0.4$ V	2.0	4.0		mA
I_{CEX}	Leakage Current	$V_{OH} = 15$ V		0.01	15	μA

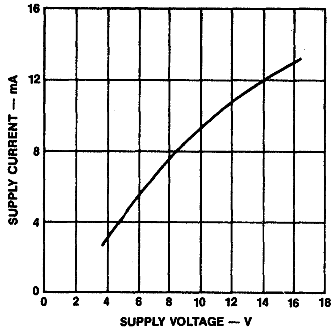
Notes

1. Timing error solely introduced by μA2240 measured as % of ideal time-base period of T = RC.
2. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Lead 1.

11

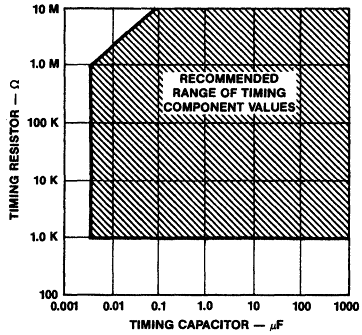
Typical Performance Curves

Supply Current vs Supply Voltage in Reset Condition



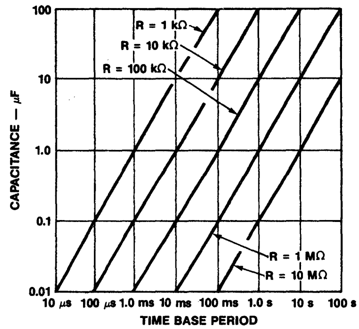
PC08090F

Recommended Range of Timing Component Values



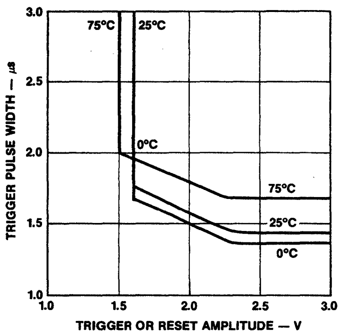
PC08100F

Time-Base Period vs External RC



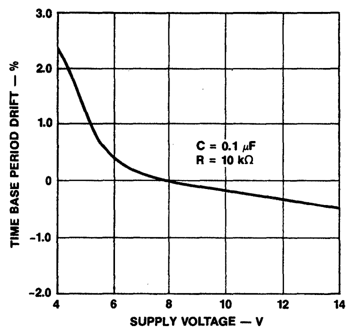
PC08110F

Minimum Trigger Pulse Width vs Trigger and Reset Amplitude



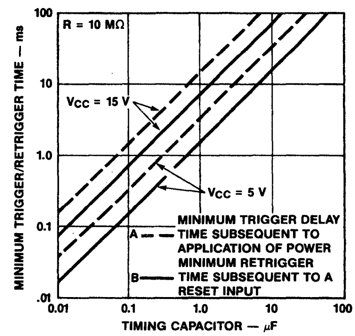
PC08120F

Time-Base Period Drift vs Supply Voltage



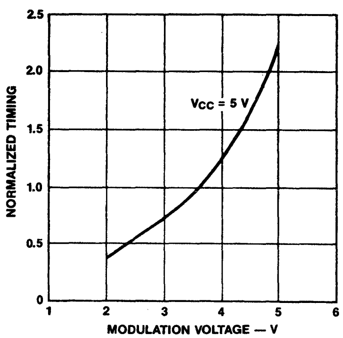
PC08130F

Minimum Trigger/Retrigger Timing vs Timing Capacitor



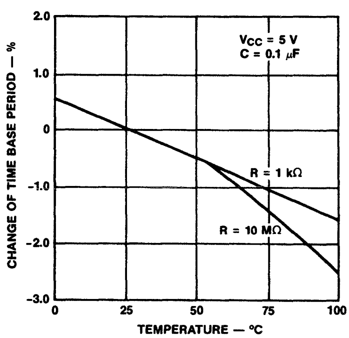
PC08140F

Normalized Change in Time-Base Period vs Modulation Voltage



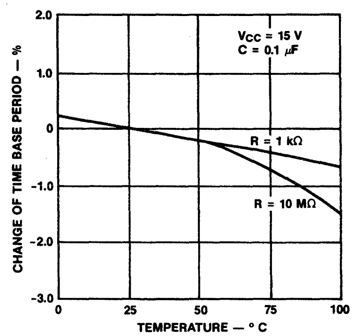
PC08150F

Time-Base Period vs Temperature



PC08160F

Time-Base Period vs Temperature



PC08170F

Functional Description

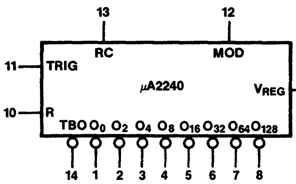
(*Figure 1* and Block Diagram)

When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive going trigger pulse to trigger lead 11, initiates the timing cycle. The trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive going reset pulse is applied to Reset, lead 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

Figure 1 Logic Symbol



V_{CC} = Lead 16
GND = Lead 9

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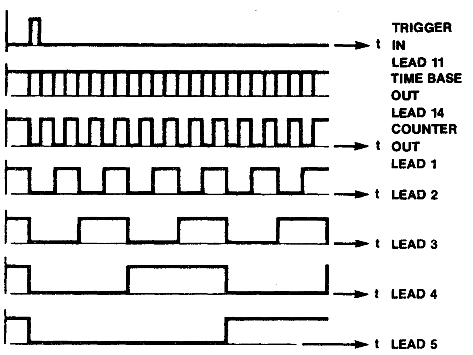
Figure 2 Timing Diagram of Output Waveforms



In most timing applications, one or more of the counter outputs are connected to the reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S1 open), the circuit operates in an astable or free running mode, following a trigger input.

Important Operating Information

Ground connection is lead 9.

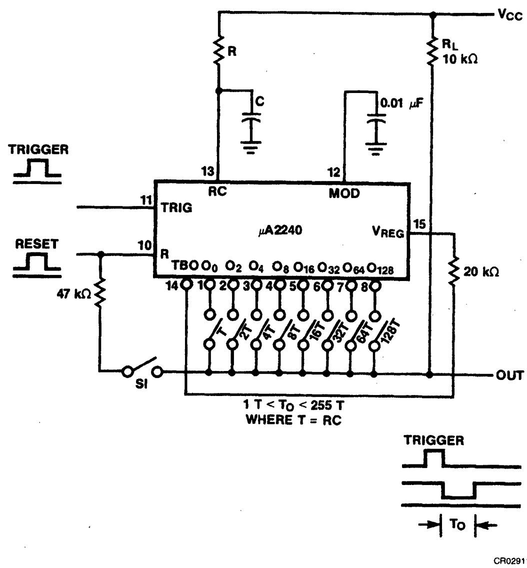
Reset (R) (lead 10) sets all outputs HIGH.

Trigger (TRIG) (lead 11) sets all outputs LOW.

Time-base output (TBO) (lead 14) can be disabled by bringing the RC input (lead 13) LOW via a 1.0 kΩ resistor.

Normal TBO (lead 14) is a negative going pulse greater than 500 ns.

Figure 3 Basic Circuit Connection for Timing Applications Monostable: S1 Closed Astable: S1 Open



Note: Under the conditions of high supply voltages (V_{CC} > 7.0 V) and low values of timing capacitor (C_T < 0.1 μF), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from TBO (lead 14) to ground (lead 9).

Reset (lead 10) stops the time-base oscillator.

Outputs ($O_0 \ldots O_{128}$) (leads 1 – 8) sink 2.0 mA current with $V_{OL} \leqslant 0.4$ V.

For use with external clock, minimum clock pulse amplitude should be 3.0 V, with greater than 1.0 μs pulse duration.

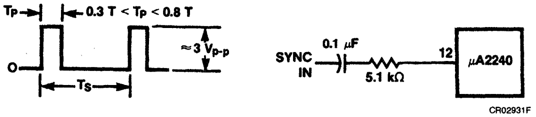
Circuit Controls

Counter Outputs ($O_0 \ldots O_{128}$, leads 1 thru 8)
The binary counter outputs are buffered open collector type stages, as shown in the block diagram. Each output is capable of sinking 2.0 mA at 0.4 V V_{OL}. In the reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2.* The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming segment of this data sheet.

Reset and Trigger Inputs (R and TRIG, 10 and 11)
The circuit is reset or triggered with positive going control pulses applied to leads 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, lead 12)
The oscillator time-base period (T) can be modulated by applying a DC voltage to MOD, lead 12 (see Performance Curves). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, lead 12, as shown in *Figure 4.* Recommended sync pulse widths and amplitudes are also given.

Figure 4 Operation with External Sync Signal



The time-base can be synchronized by setting T to be an integer multiple of the sync pulse period (T_S). This can be done by choosing the timing components R and C at lead 13 such that:

$$T = RC = (T_S/m)$$

where:

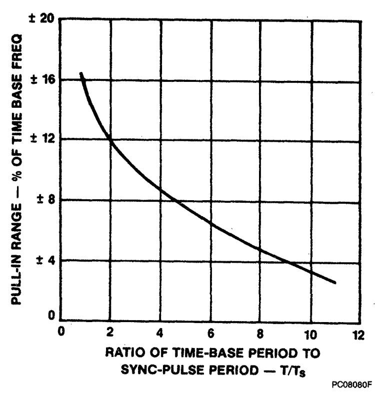
m is an integer, $1.0 \leqslant m \leqslant 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For m < 10, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (lead 13)
The time-base period T is determined by the external RC network connected to RC, lead 13. When the time-base is triggered, the waveform at lead 13 is an exponential ramp with a period T = 1 RC.

Time-Base Output (TBO, lead 14)
The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to lead 15 for proper circuit operation. In the reset state, the time-base output is HIGH. After triggering, it produces a negative going pulse train with a period T = RC, as shown in the diagram of *Figure 2.* The time-base output is internally connected to the binary counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative going edge of the timing or clock pulses generated at TBO, lead 14. The trigger threshold for the counter section is

Figure 5 Typical Pull-in Range for Harmonic Synchronization



≈ +1.4 V. The counter section can be disabled by clamping the voltage level at lead 14 to ground.

When using high supply voltages ($V_{CC} > 7.0$ V) and a small value timing capacitor ($C_T < 0.1$ μF), the pulse width at TBO lead 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from lead 14 to ground.

Regular Output (V_{REG}, lead 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded *(see Figure 6)* to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time-base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, lead 15 should be shorted to lead 16.

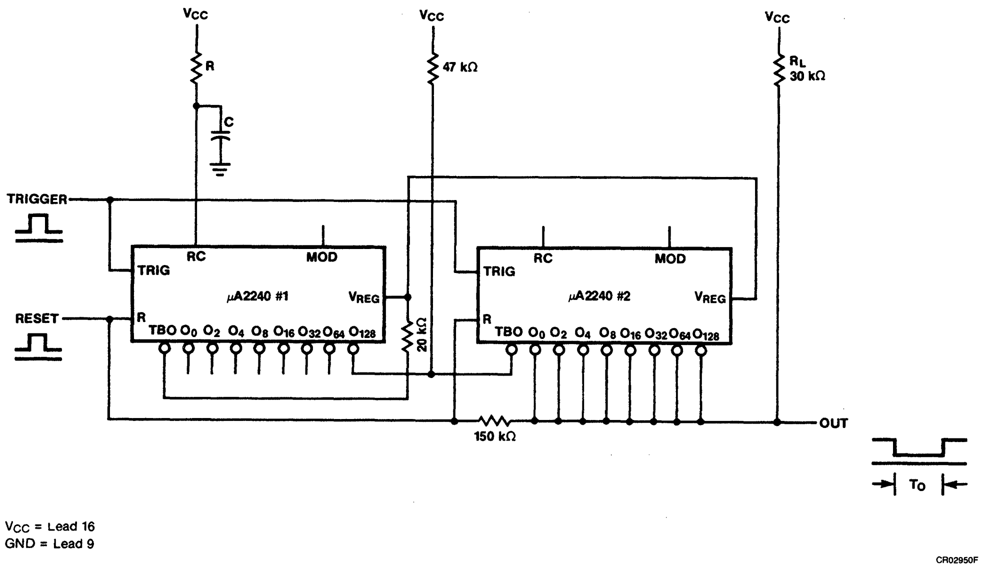
Monostable Operation

Precision Timing
In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3.* The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration (T_O) and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = nT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC lead 13 (see Performance Curves) and n is an integer in the range of $1 \leqslant n \leqslant 255$ as determined by the combination of counter outputs ($O_0 \ldots O_{128}$), leads 1 through 8, connected to the output bus.

Figure 6 Low Power Operation of Cascaded Timers



Counter Output Programming

The binary counter outputs, $O_0 \ldots O_{128}$, leads 1 through 8 are open collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only lead 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if leads 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\ T = 49\ T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\ T \leqslant T_O \leqslant 255\ T$.

Ultra Long Time Delay Application

Two μA2240 units can be cascaded as shown in *Figure 7* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the reset and the trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

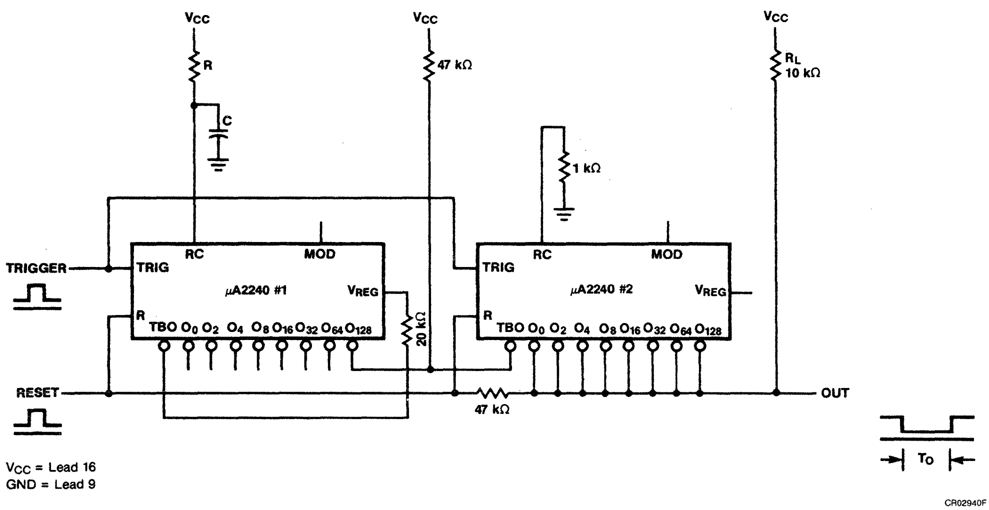
In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{CC} terminal (lead 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (lead 15) of both units together.

Astable Operation

The μA2240 can be operated in its astable or free running mode by disconnecting the reset terminal (lead 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive going reset signal to lead 10, the circuit reverts back to its reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self triggers automatically when the power supply is turned on, and continues to operate in its free running mode indefinitely. In astable or free running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Figure 7 Cascaded Operation for Long Delays



Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

Figure 8 Operation with Trigger and Reset Inputs (Note 1)

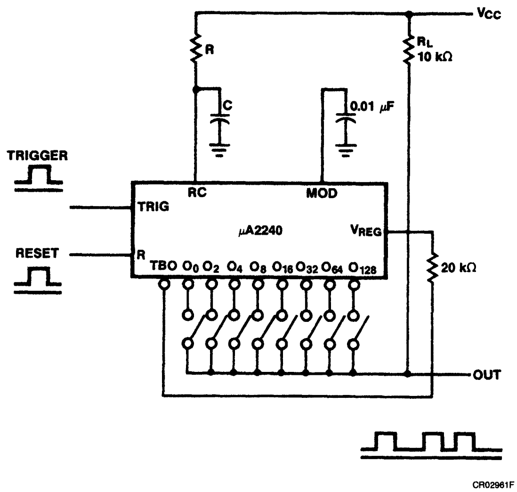


Figure 9 Free Running or Continuous Operation (Note 1)

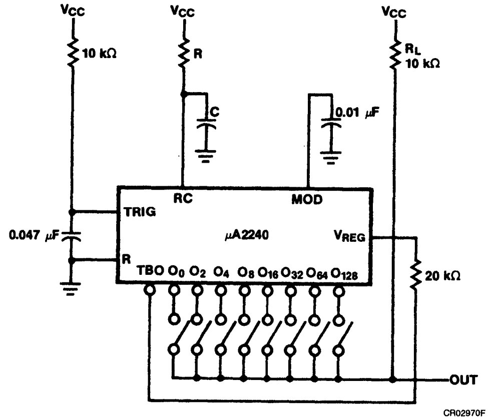
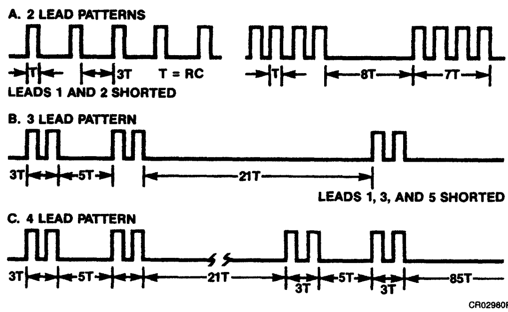


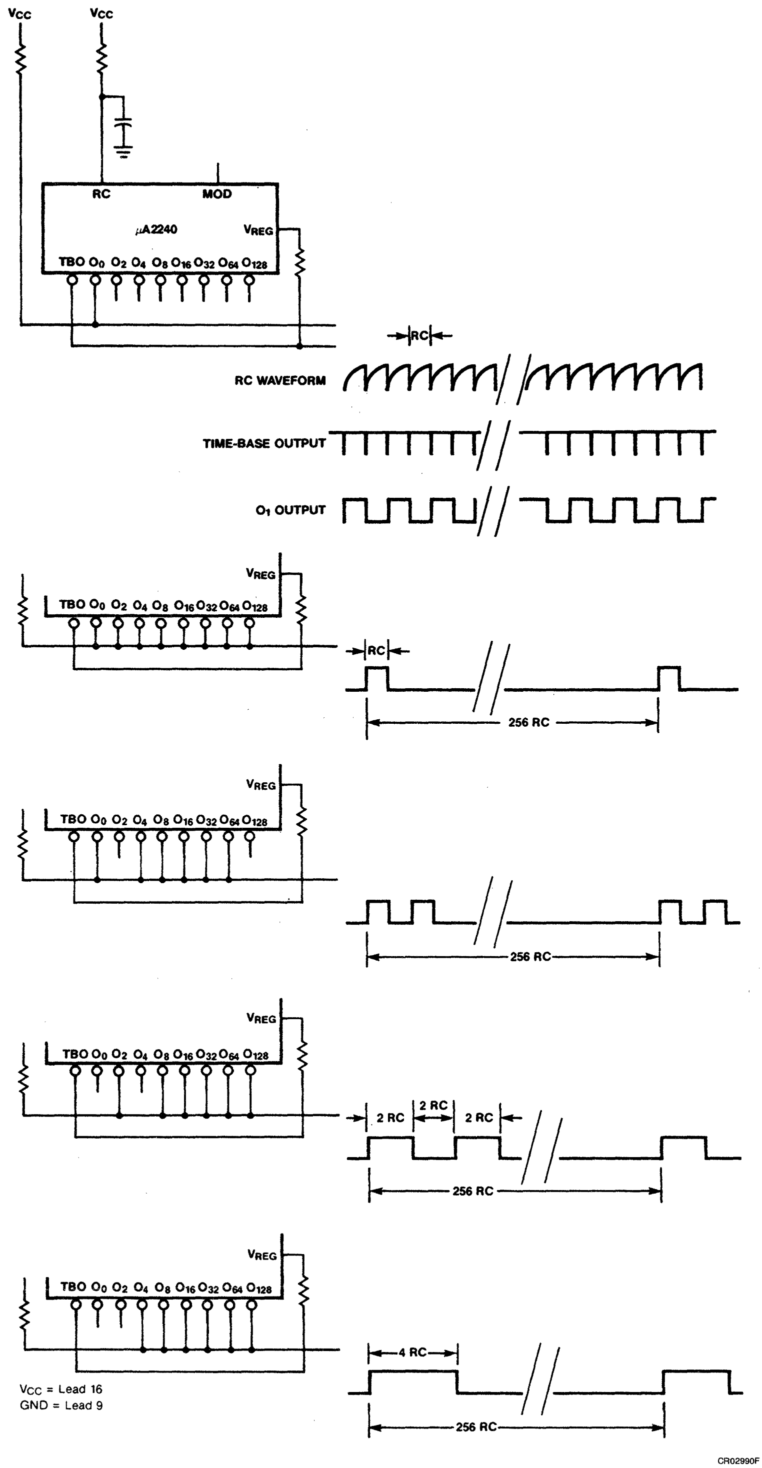
Figure 10 Binary Pulse Patterns Obtained by Shorting Various Counter Outputs



Note

1. V_{CC} = Lead 16
   GND = Lead 9

Figure 11 Continuous Free run Operation Examples of Output



FAIRCHILD

A Schlumberger Company

μA3046 • μA3086 General Purpose Transistor Arrays

Linear Division Special Functions

Description

The μA3046 and μA3086 are general purpose transistor arrays. Each contains a differentially connected pair and three individually isolated transistors. Each part is designed for general purpose, low power applications for consumer and industrial applications.

- **Low Input Offset Voltage**
- **Wideband Operation**
- **Low Noise**
- **Matched Differential Amplifier**

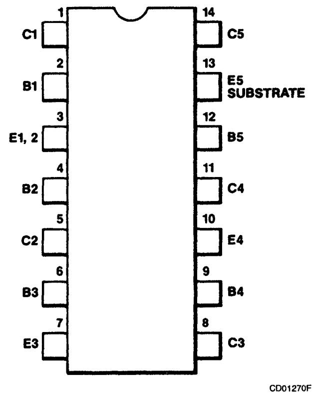
Absolute Maximum Ratings (Each Transistor)

Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
μA3046	0°C to +70°C
μA3086	-40°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Collector-to-Emitter Voltage	15 V
Collector-to-Base Voltage	20 V
Collector-to-Substrate Voltage[3]	20 V
Emitter-to-Base Voltage	5.0 V
Collector Current	50 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C. The 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Substrate must be connected to the most negative voltage to maintain normal operation.

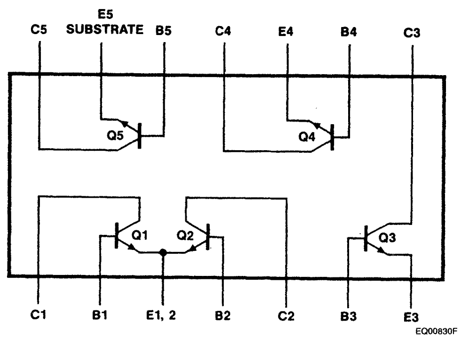
Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



Order Information

Device Code	Package Code	Package Description
μA3046PC	9A	Molded DIP
μA3046SC	KD	Molded Surface Mount
μA3086DV	6A	Ceramic DIP
μA3086PV	9A	Molded DIP
μA3086SV	KD	Molded Surface Mount

Equivalent Circuit



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μA3046

Electrical Characteristics $T_A = 25°C$ unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1.0$ mA, $I_B = 0$		15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10\ \mu A$, $I_C = 0$		20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10\ \mu A$, $I_C = 0$		5.0	7.0		V
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0$			0.002	40	nA
I_{CEO}	Collector Cutoff Current	$V_{CE} = 10$ V, $I_B = 0$			See Curve	0.5	μA
h_{fe}	Static Forward Current-Transfer Ratio (Static Beta)	$V_{CE} = 3.0$ V	$I_C = 10$ mA		100		
			$I_C = 1.0$ mA	40	100		
			$I_C = 10\ \mu A$		54		
ΔI_{IO}	Input Offset Current for Matched Pair Q_1 and Q_2 $\|I_{IO1} - I_{IO2}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			0.3		μA
V_{BE}	Base-to-Emitter Voltage	$V_{CE} = 3.0$ V	$I_E = 1.0$ mA		0.715		V
			$I_E = 10$ mA		0.800		
ΔV_{BE}	Magnitude of Input Offset Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			0.45	5.0	mV
ΔV_{BE}	Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			0.45	5.0	mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base-to-Emitter Voltage	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	$I_B = 1.0$ mA, $I_C = 10$ mA			0.23		V
$\|\Delta V_{IO}\|/\Delta T$	Temperature Coefficient of Magnitude of Input-Offset Voltage	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			1.1		μV/°C
NF	Low Frequency Noise Figure	f = 1.0 kHz, $V_{CE} = 3.0$ V, $I_C = 100\ \mu A$, $R_S = 1.0$ kΩ			3.25		dB

μA3086
Electrical Characteristics T_A = 25°C unless otherwise specified.

Symbol	Characteristic	Condition		Min	Typ	Max	Unit
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	I_C = 10 μA, I_E = 0		20	60		V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0		15	24		V
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	I_C = 10 μA, I_C = 0		20	60		V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	I_E = 10 μA, I_C = 0		5.0	7.0		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10 V, I_E = 0			0.002	100	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10 V, I_B = 0			See Curve	5.0	μA
h_{fe}	Static Forward Current Transfer Ratio (Static Beta)	V_{CE} = 3.0 V	I_C = 10 mA		100		
			I_C = 1.0 mA	40	100		
			I_C = 10 μA		54		
ΔI_{IO}	Input Offset Current for Matched Pair Q_1 and Q_2 $\|I_{IO1} - I_{IO2}\|$	V_{CE} = 3.0 V, I_C = 1.0 mA			0.3		μA
V_{BE}	Base-to-Emitter Voltage	V_{CE} = 3.0 V	I_E = 1.0 mA		0.715		V
			I_E = 10 mA		0.800		
ΔV_{BE}	Magnitude of Input Offset Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$	V_{CE} = 3.0 V, I_C = 1.0 mA			0.45		mV
ΔV_{BE}	Magnitude of Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$	V_{CE} = 3.0 V, I_C = 1.0 mA			0.45		mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base-to-Emitter Voltage	V_{CE} = 3.0 V, I_C = 1.0 mA			−1.9		mV/°C
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	I_B = 1.0 mA, I_C = 10 mA			0.23		V
$\|\Delta V_{IO}\|/\Delta T$	Temperature Coefficient of Magnitude of Input-Offset Voltage	V_{CE} = 3.0 V, I_C = 1.0 mA			1.1		μV/°C
NF	Low Frequency Noise Figure	f = 1.0 kHz, V_{CE} = 3.0 V, I_C = 100 μA, R_S = 1.0 kΩ			3.25		dB

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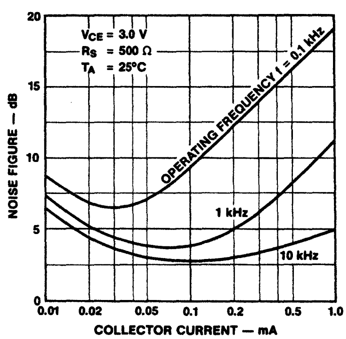
μA3046 and μA3086
Electrical Characteristics $T_A = 25°C$ unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Low Frequency, Small Signal Equivalent Circuit Characteristics						
h_{fe}	Forward Current Transfer Ratio	f = 1.0 kHz, $V_{CE} = 3.0$ V, $I_C = 1.0$ mA		110		
h_{ie}	Short Circuit Input Resistance			3.5		kΩ
h_{oe}	Open Circuit Output Conductance			15.6		μmho
h_{re}	Open Circuit Reverse Voltage Transfer Ratio			1.8×10^{-4}		
Y_{fe}	Admittance Characteristics: Forward Transfer Admittance	f = 1.0 MHz, $V_{CE} = 3.0$ V, $I_C = 1.0$ mA		31 − j1.5		
Y_{ie}	Input Admittance			0.3 + j0.04		
Y_{oe}	Output Admittance			0.001 + j0.03		
Y_{re}	Reverse Transfer Admittance			See Curve		
f_T	Gain Bandwidth Product	V_{CE} = 3.0 V, I_C = 3.0 mA	300	500		MHz
C_{EB}	Emitter-to-Base Capacitance	V_{EB} = 3.0 V, I_E = 0		0.6		pF
C_{CB}	Collector-to-Base Capacitance	V_{CB} = 3.0 V, I_C = 0		0.58		pF
C_{CI}	Collector-to-Substrate Capacitance	V_{CS} = 3.0 V, $I_C = 0$		2.8		pF

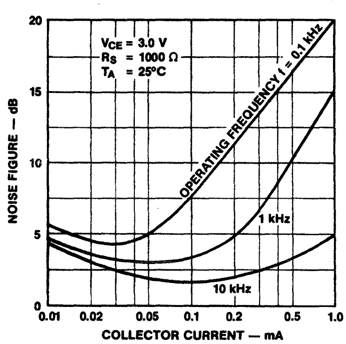
Typical Performance Curves

Noise Figure vs Collector Current



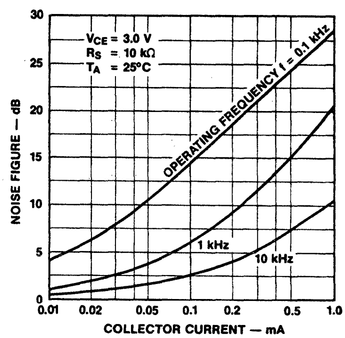
PC08180F

Noise Figure vs Collector Current



PC08190F

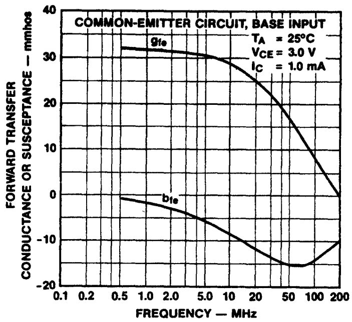
Noise Figure vs Collector Current



PC08200F

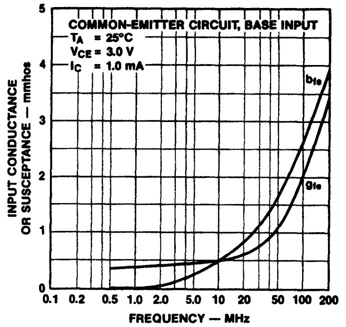
Typical Performance Curves (Cont.)

Forward Transfer Admittance vs Frequency



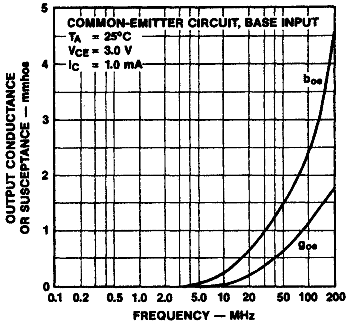
PC08210F

Input Admittance vs Frequency



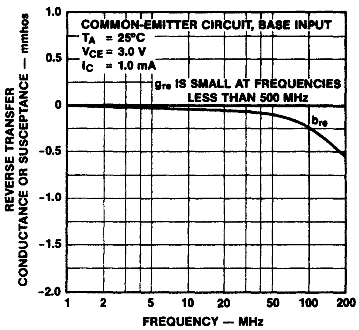
PC08220F

Output Admittance vs Frequency



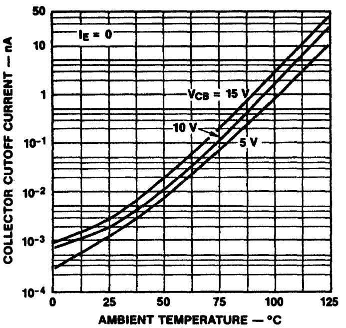
PC08230F

Reverse Transfer Admittance vs Frequency



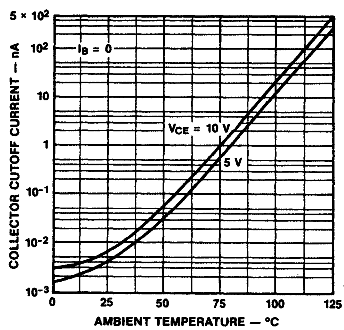
PC08240F

Collector-to-Base Cutoff Current vs Temperature for Each Transistor



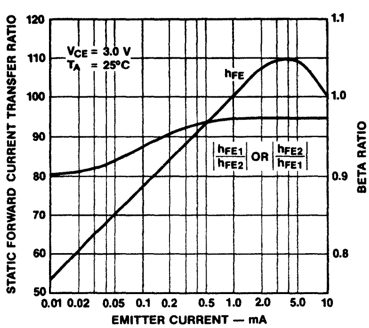
PC08250F

Collector-to-Emitter Cutoff Current vs Temperature for Each Transistor



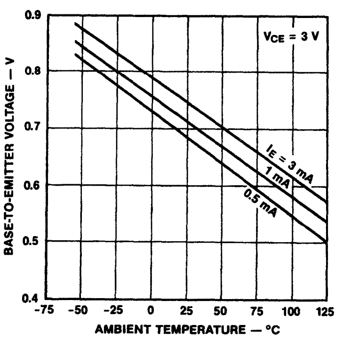
PC08260F

Static Forward Current Transfer and Beta Ratio for Transistors Q1, Q2 vs Emitter Current



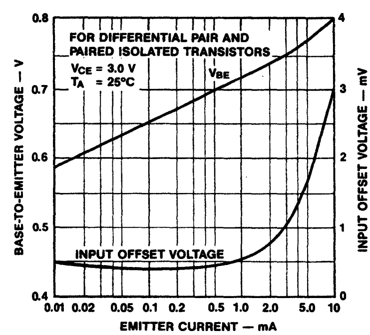
PC08270F

Base-to-Emitter Voltage Characteristic vs Temperature for Each Transistor



PC08280F

Static Base-to-Emitter Voltage and Input Offset Voltage vs Emitter Current



PC08290F

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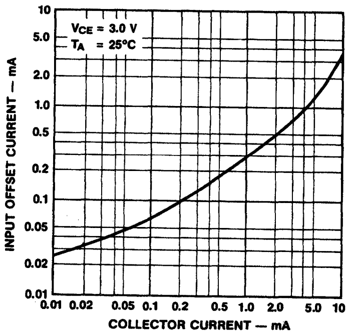
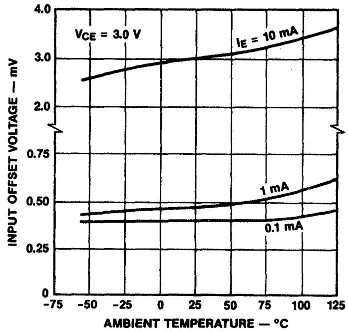
Typical Performance Curves (Cont.)

Input Offset Current for Matched Transistor Pair Q1, Q2 vs Collector Current



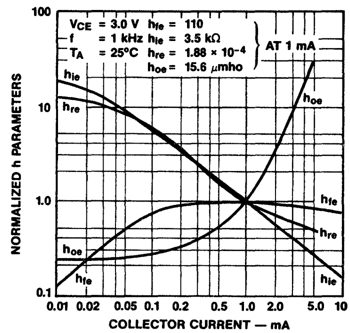
PC08300F

Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Ambient Temperature



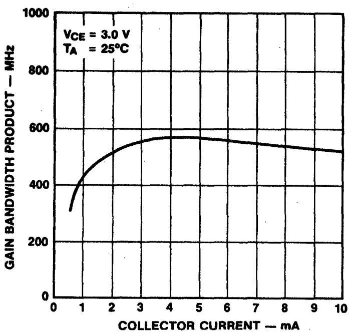
PC08310F

Normalized h Parameters vs Collector Current



PC08320F

Gain Bandwidth Product vs Collector Current



PC08330F

FAIRCHILD

A Schlumberger Company

μA3680 Quad Telephone Relay Driver

Linear Division Special Functions

Description

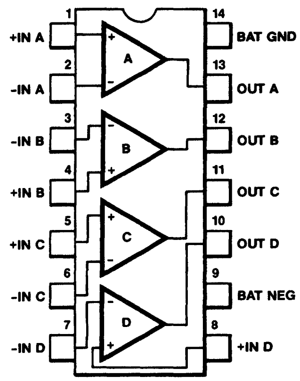
The μA3680 Relay Driver is a monolithic integrated circuit designed to interface −48 V relays to TTL or other logic systems in telephony applications. The device has a 50 mA source capability and operates from −48 V battery power. The quad configuration increases board density in typical line card applications. Since there can be considerable noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a high common mode range (±20 V referenced to battery ground). Also, each driver has common mode range separate from the other drivers in the package. Low differential input current (typically 100 μA) draws low power from the driving circuit. Differential inputs permit either inverting or non-inverting operation. A clamp network is incorporated in the driver outputs, eliminating the need for an external network to quench the high voltage inductive backswing caused when the relay is turned off. A fail-safe feature is incorporated to insure that the driver will be off in the V_I+ input or both inputs are open. Standby power (driver off) is very low, typically 50 μW per driver.

- **−48 V Battery Operation**
- **50 mA Output Capability**
- **TTL/CMOS Compatible Comparator Input**
- **High Common Mode Input Voltage Range**
- **Very Low Input Current**
- **Fail-Safe Disconnect Feature**
- **Built-In Output Clamp Diode**

Absolute Maximum Ratings[1]

Storage Temperature Range		
Ceramic DIP	−65°C to +175°C	
Molded DIP and SO-14	−65°C to +150°C	
Operating Temperature Range	−25°C to +85°C	
Lead Temperature		
Ceramic DIP (soldering, 60 s)	300°C	
Molded DIP and SO-Package (soldering, 10 s)	265°C	
Internal Power Dissipation[2, 3]		
14L-Ceramic DIP	1.36 W	
14L-Molded DIP	1.04 W	
SO-14	0.93 W	
Differential Input Voltage	±20 V	
Output Current ($L_L \leqslant 5.0$ H)	50 mA	
Output Current (R_L)	100 mA	
	Max	Min
BAT NEG	+0.5 V	−70 V
Input Voltage (BAT NEG ⩾ −50 V)	+20 V	BAT NEG −0.5 V

Connection Diagram
14-Lead DIP and SO-14 Package (Top View)



CD01290F

Order Information

Device Code	Package Code	Package Description
μA3680DV	6A	Ceramic DIP
μA3680PV	9A	Molded DIP
μA3680SV	KD	Molded Surface Mount

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Notes

1. All voltages are with respect to BAT GND.
2. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
3. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

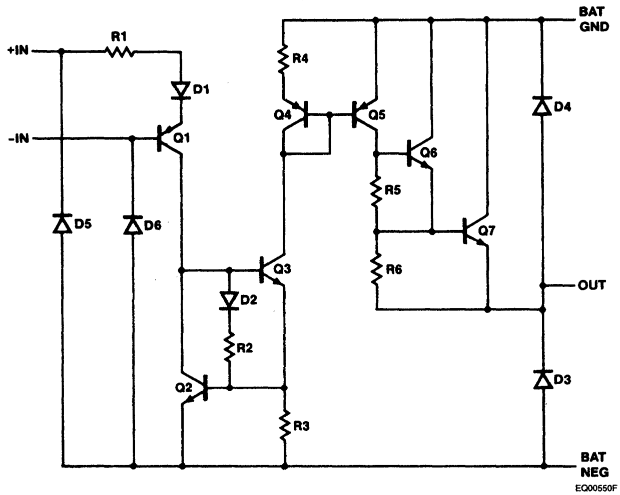
Recommended Operating Conditions

Characteristic	Min	Max	Unit
Battery Voltage (BAT NEG)	-60	-10	V
Input Voltage	-10	+10	V
Logic On Voltage (V_I+-V_I-)	+2	+10	V
Logic Off Voltage (V_I+-V_I-)	-10	+0.8	V
Temperature Range	-25	+85	°C

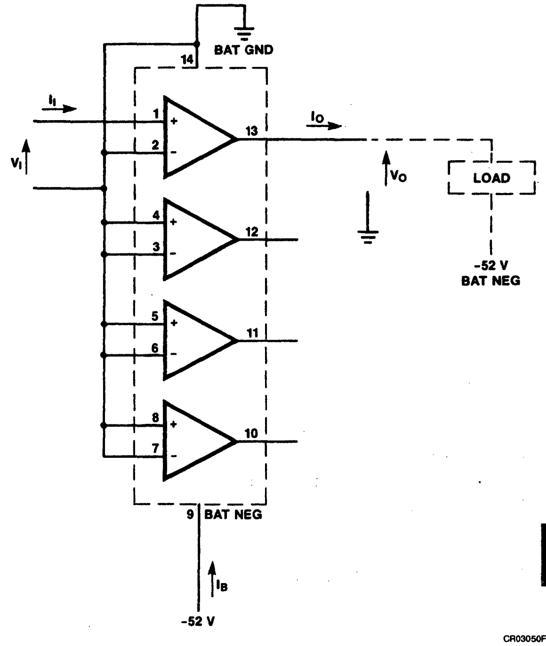
Electrical Characteristics Over Recommended Operating Conditions unless otherwise specified. $T_A = 25°C$, BAT NEG = −52 V.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
V_{IH}	Logic "1" Differential Input Voltage			1.3	2.0	V
V_{IL}	Logic "0" Differential Input Voltage		0.8	1.3		V
I_{INH}	Logic "1" Input Current	$V_I+ = 2.0$ V, $V_I- = 0$ V		40	100	μA
		$V_I+ = 7.0$ V, $V_I- = 0$ V		375	1000	
I_{INL}	Logic "0" Input Current	$V_I+ = 0.4$ V, $V_I- = 0$ V		+0.01	+5.0	μA
		$V_I+ = -7.0$ V, $V_I- = 0$ V	−100	−1.0		
V_{OL}	Output ON Voltage	$I_{OL} = -50$ mA	−2.1	−1.6		V
I_{OFF}	Output Leakage	V_O = BAT NEG	−100	−2.0		μA
I_{FS}	Fail-Safe Output Leakage	V_O = BAT NEG (Inputs open)	−100	−2.0		μA
I_{LC}	Output Clamp Leakage Current	V_O = BAT GND	−100	−2.0		μA
V_C	Output Clamp Voltage	$I_{CLAMP} = -50$ mA, Referenced to BAT NEG	−1.2	−0.9		V
V_P	Positive Output Clamp Voltage	$I_{CLAMP} = +50$ mA, Referenced to BAT GND		0.9	1.2	V
$I_{B(ON)}$	Supply Current	All Drivers On	−4.4	−2.0		mA
$I_{B(OFF)}$	Supply Current	All Drivers Off	−100	−1.0		μA
t_{PLH}	Propagation Delay, Output Low-to-High	L = 1.0 H, R_L = 1.0 kΩ		1.0	10	μs
t_{PHL}	Propagation Delay, Output High-to-Low	L = 1.0 H, R_L = 1.0 kΩ		1.0	10	μs

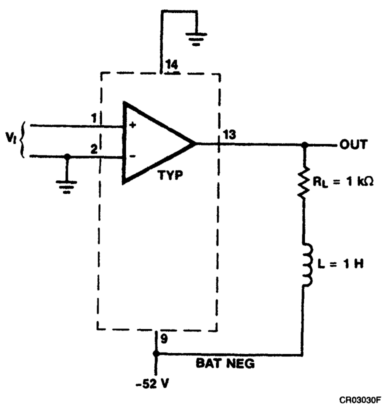
Equivalent Circuit (1/4 of circuit)

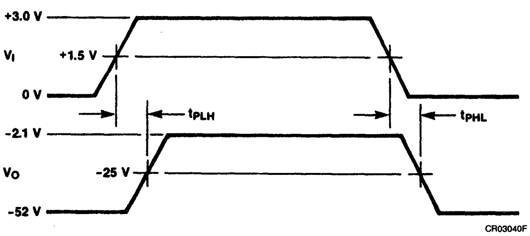


DC Test Circuit

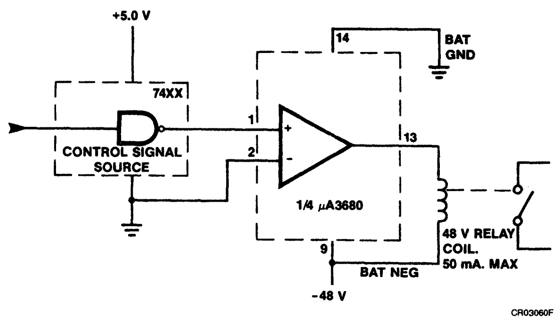


AC Test Circuit and Waveforms





Typical Applications



FAIRCHILD

A Schlumberger Company

μA555
Single Timing Circuit

Linear Division Special Functions

Description

The μA555 Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

- **Timing Control, μs To Hours**
- **Astable Or Monostable Operating Modes**
- **Adjustable Duty Cycle**
- **200 mA Sink or Source Output Current**
- **TTL Output Drive Capability**
- **Temperature Stability Of 0.005% Per °C Typ**
- **Normally On Or Normally Off Output**
- **Direct Replacement For SE555/NE555**

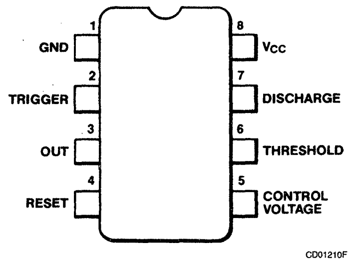
Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Molded DIP	0.93 W
SO-8	0.81 W
Supply Voltage	+18 V

Notes

1. $T_{J\ Max} = 150°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Molded DIP at 7.5 mW/°C, and SO-8 at 6.5 mW/°C.

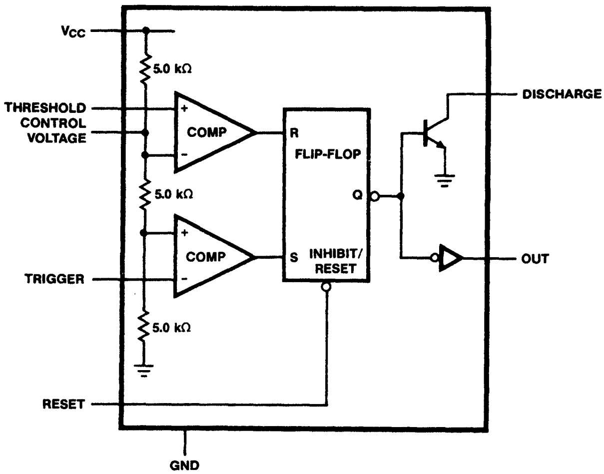
Connection Diagram
8-Lead DIP and SO-8 Package
(Top View)



Order Information

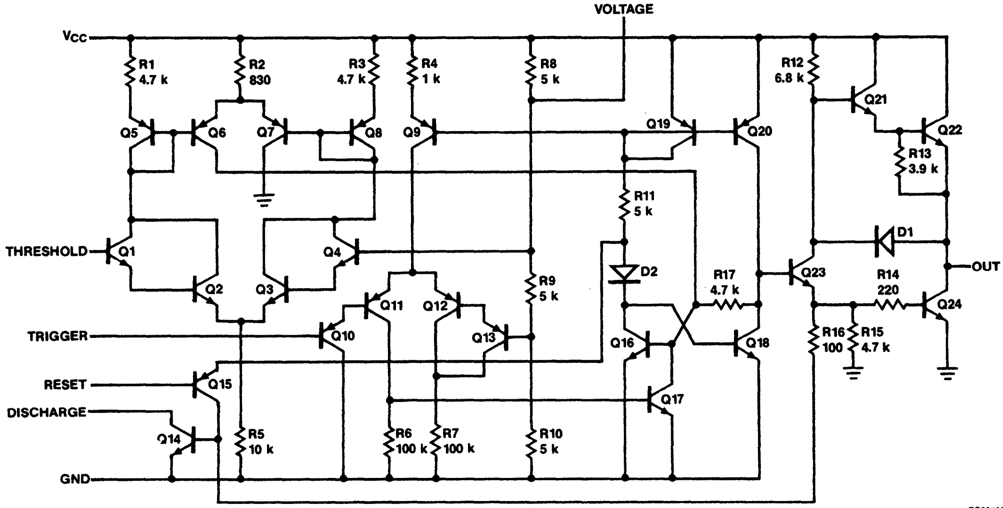
Device Code	Package Code	Package Description
μA555TC	9T	Molded DIP
μA555SC	KC	Molded Surface Mount

Block Diagram



EQ00480F

Equivalent Circuit (Note 1)



EQ00490F

Note
1. All resistor values in ohms.

μA555

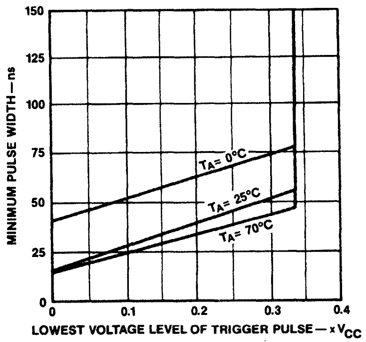
Electrical Characteristics $T_A = 25°C$, V+ = +5.0 V to +15 V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage			4.5		16	V
I_{CC}	Supply Current[1]		$V_{CC} = 5.0$ V, $R_L = \infty$		3.0	6.0	mA
			$V_{CC} = 15$ V, $R_L = \infty$ LOW State		10	15	
t_D	Timing Error	Initial Accuracy	$R_I = 2.0$ kΩ to 100 kΩ C = 0.1 μF		1.0		%
		Drift with Temperature			50		ppm/°C
		Drift with Supply Voltage			0.1		% V
V_{TH}	Threshold Voltage		$V_{CC} = 5.0$ V	2.6	3.33	4.0	V
			$V_{CC} = 15$ V	9.0	10	11	
V_{TR}	Trigger Voltage		$V_{CC} = 15$ V	4.0	5.0	6.0	V
			$V_{CC} = 5.0$ V	1.1	1.67	2.2	
I_{TR}	Trigger Current				0.5	5.0	μA
V_R	Reset Voltage			0.4	0.7	1.0	V
I_R	Reset Current				0.1	1.5	mA
I_{TH}	Threshold Current[2]				0.1	0.25	μA
V_{CV}	Control Voltage Level		$V_{CC} = 15$ V	9.0	10	11	V
			$V_{CC} = 5.0$ V	2.6	3.33	4.0	
V_{OL}	Output Voltage LOW		$V_{CC} = 15$ V, $I_O- = 10$ mA		0.1	0.25	V
			$I_O- = 50$ mA, $V_{CC} = 15$ V		0.4	0.75	
			$I_O- = 100$ mA, $V_{CC} = 15$ V		2.0	2.5	
			$I_O- = 200$ mA, $V_{CC} = 15$ V		2.5	3.5	
			$V_{CC} = 5.0$ V, $I_O- = 8.0$ mA		0.3		
			$I_O- = 5.0$ mA, $V_{CC} = 5.0$ V		0.25	0.35	
V_{OH}	Output Voltage HIGH		$I_O+ = 200$ mA, $V_{CC} = 15$ V	11.0	12.5		V
			$I_O+ = 100$ mA, $V_{CC} = 15$ V	12.75	13.3		
			$V_{CC} = 5.0$ V, $I_O+ = 100$ mA	2.75	3.3		
t_r	Rise Time of Output				100		ns
t_f	Fall Time of Output				100		ns
I_{DIS}	Discharge Leakage Current				20	100	nA

Notes
1. Supply Current is typically 1.0 mA less when output is HIGH.
2. This will determine the maximum value of $R_1 + R_2$. For 15 V operation, the maximum total R = 10 MΩ.

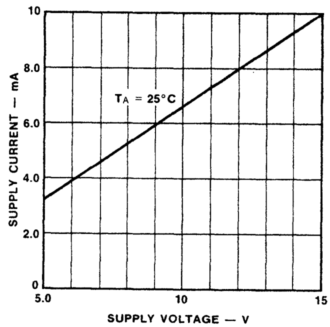
Typical Performance Curves

Minimum Pulse Width Required for Triggering



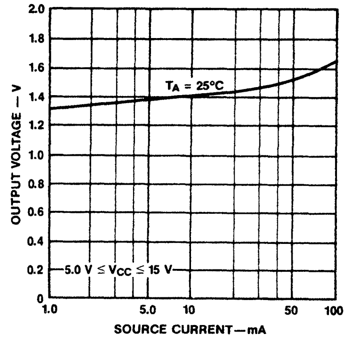
PC07111F

Total Supply Current vs Supply Voltage



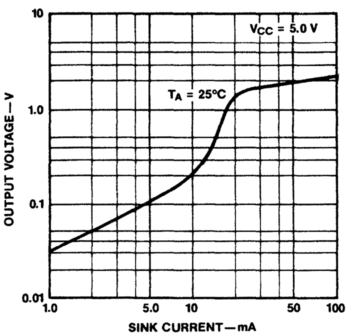
PC02120F

Output Voltage HIGH vs Output Source Current



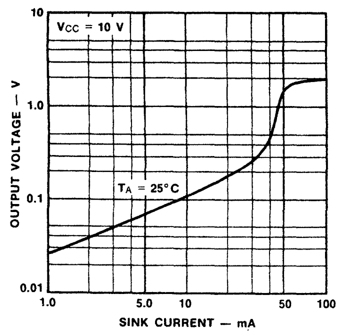
PC07640F

Output Voltage LOW vs Output Sink Current



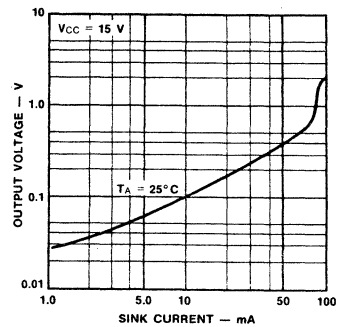
PC07650F

Output Voltage LOW vs Output Sink Current



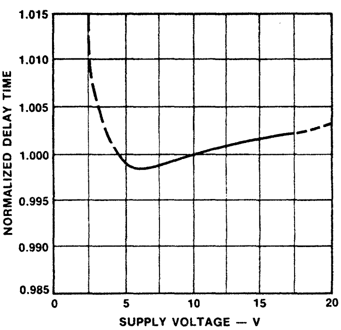
PC02150F

Output Voltage LOW vs Output Sink Current



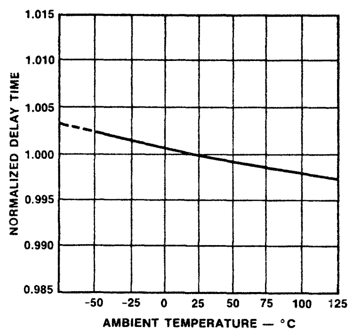
PC02160F

Delay Time vs Supply Voltage



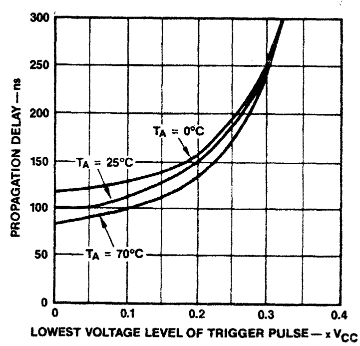
PC02170F

Delay Time vs Ambient Temperature



PC02180F

Propagation Delay vs Voltage Level of Trigger Pulse



PC07661F

11

Typical Applications

Monostable Operation

In the monostable mode, the timer functions as a one shot. Referring to *Figure 1* the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 2, the flip-flop is set, releasing the short circuit across the external capacitor and driving the output HIGH. The voltage across the capacitor increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals ⅔ V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. *Figure 2* shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches ⅓ V_{CC}. Once triggered, the circuit remains in this state until the set time elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by *Figure 3.* Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the trigger terminal (lead 2) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied HIGH to avoid any possibility of false triggering.

Figure 1 Monostable Mode

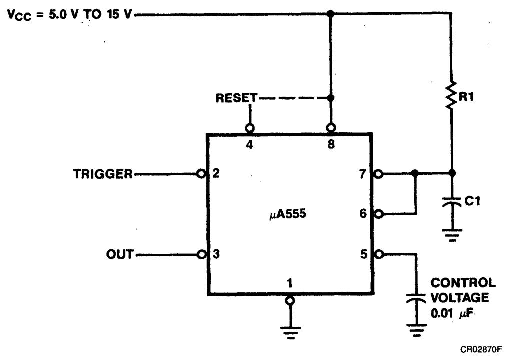


Figure 2 Monostable Waveform

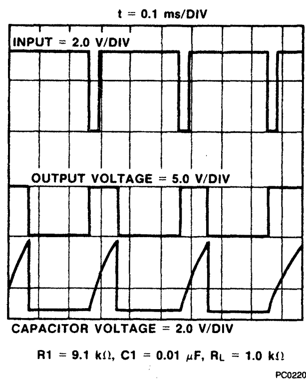
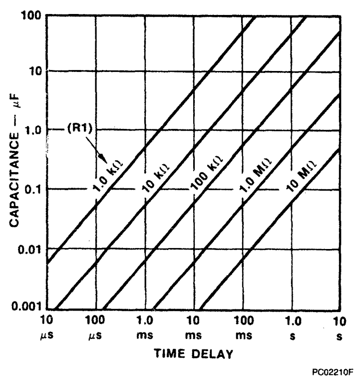


Figure 3 Time Delay vs R1 and C1



Astable Operation

When the circuit is connected as shown in *Figure 4* (leads 2 and 6 connected) it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between ⅓ V_{CC} and ⅔ V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by *Figure 6.*

The duty cycle is given by:

$$DC = \frac{R2}{R1 + 2R2}$$

Figure 4 Astable Mode

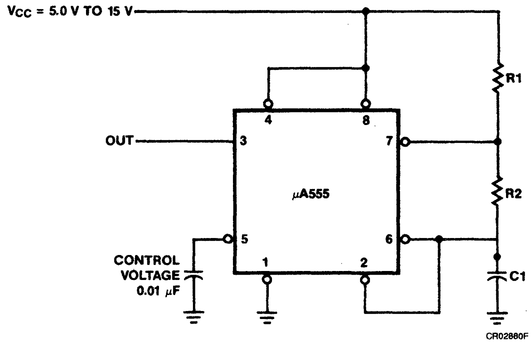
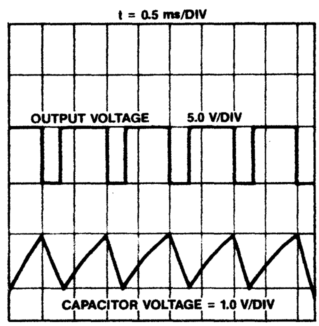


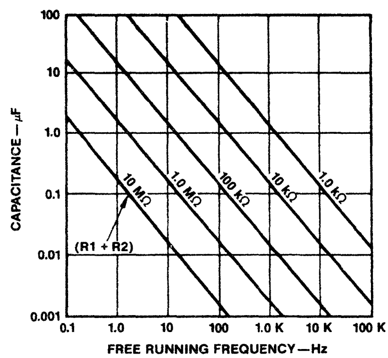
Figure 5 Astable Waveform



R1 = R2 = 4.8 kΩ, C1 = 0.1 μF, R_L = 1 kΩ

PC02221F

Figure 6 Free Running Frequency vs R1, R2, and C1



PC02231F

FAIRCHILD

A Schlumberger Company

μA556 Dual Timing Circuits

Linear Division Special Functions

Description

The μA556 Timing Circuits are very stable controllers for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied, ending the time-out.

The output, which is capable of sinking or sourcing 200 mA, is compatible with TTL circuits and can drive relays or indicator lamps.

The μA556 Dual Timing Circuit is a pair of μA555s for use in sequential timing or applications requiring multiple timers.

- **Timing Control, μs To Hours**
- **Astable Or Monostable Operating Modes**
- **Adjustable Duty Cycle**
- **200 mA Sink Or Source Output Current**
- **TTL Output Drive Capability**
- **Temperature Stability Of 0.005% Per °C Typ**
- **Normally On Or Normally Off Output**

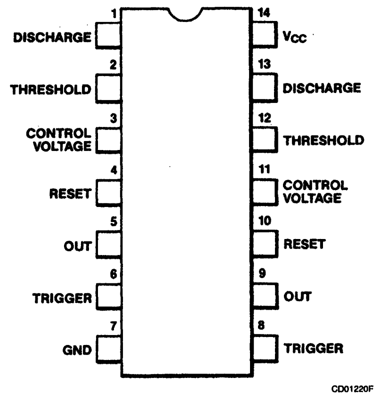
Absolute Maximum Ratings

Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	1.04 W
Supply Voltage	+18 V

Notes

1. $T_{J\ Max} = 150°C$.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate at 8.3 mW/°C.

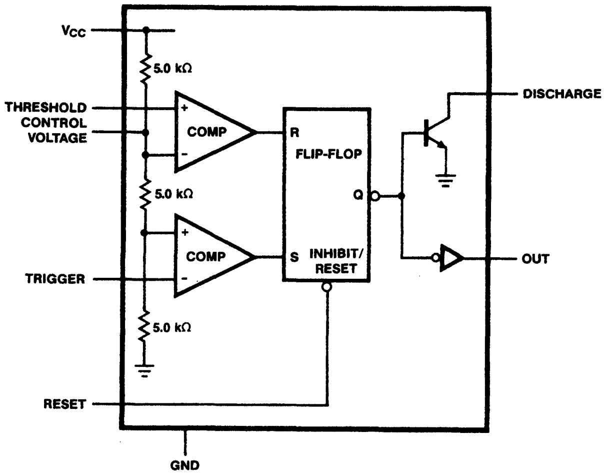
Connection Diagram
14-Lead DIP
(Top View)



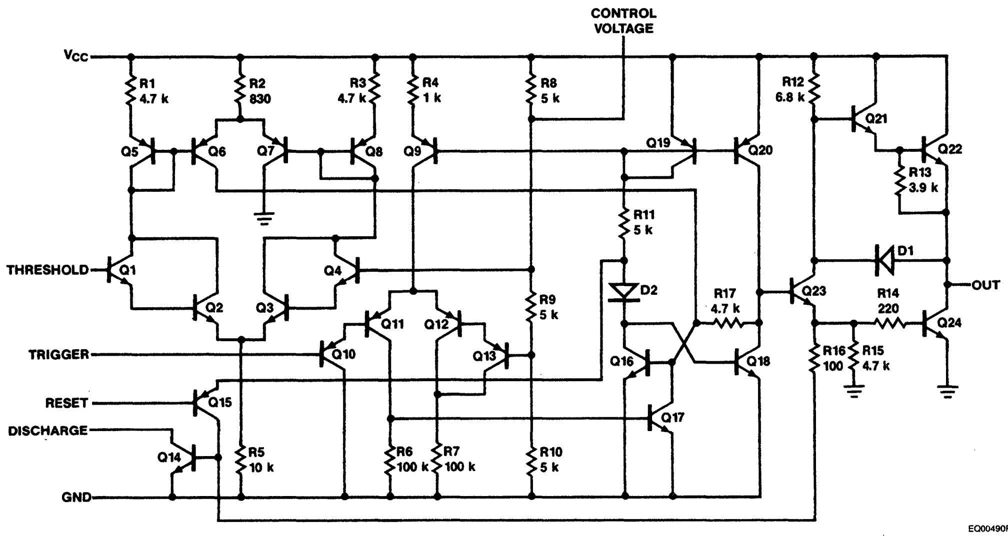
Order Information

Device Code	Package Code	Package Description
μA556PC	9A	Molded DIP

Block Diagram (1/2 of circuit)



Equivalent Circuit (1/2 of circuit) (Note 1)



Note

1. All resistor values in ohms.

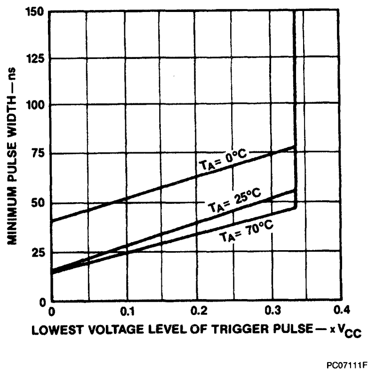
μA556
Electrical Characteristics $T_A = 25°C$, V+ = +5.0 V to +15 V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage			4.5		16	V
I_{CC}	Supply Current (Total)[1]		$V_{CC} = 5.0$ V, $R_L = \infty$		6.0	12	mA
			$V_{CC} = 15$ V, $R_L = \infty$ LOW State		20	28	
t_D	Timing Error (Monostable)	Initial Accuracy	$R_1 = 2.0$ kΩ to 100 kΩ C = 0.1 μF		0.75		%
		Drift with Temperature			50		ppm/°C
		Drift with Supply Voltage			0.1		% V
$t_{CH, DIS}$	Timing Error (Astable)	Initial Accuracy	R_1, $R_2 = 2.0$ kΩ to 100 kΩ C = 0.1 μF		2.25		%
		Drift with Temperature			150		ppm/°C
		Drift with Supply Voltage			0.3		% V
V_{TH}	Threshold Voltage		$V_{CC} = 5.0$ V	2.6	3.33	4.0	V
			$V_{CC} = 15$ V	9.0	10	11	
I_{TH}	Threshold Current[2]				30	250	nA
V_{TR}	Trigger Voltage		$V_{CC} = 15$ V	4.0	5.0	6.0	V
			$V_{CC} = 5.0$ V	1.3	1.67	2.0	
I_{TR}	Trigger Current				0.5	5.0	μA
V_R	Reset Voltage			0.4		1.0	V
I_R	Reset Current				0.1	1.5	mA
V_{CV}	Control Voltage Level		$V_{CC} = 15$ V	9.0	10	11	V
			$V_{CC} = 5.0$ V	2.6	3.33	4.0	
V_{OL}	Output Voltage LOW		$I_O- = 10$ mA, $V_{CC} = 15$ V		0.1	0.25	V
			$I_O- = 50$ mA, $V_{CC} = 15$ V		0.4	0.75	
			$I_O- = 100$ mA, $V_{CC} = 15$ V		2.0	2.75	
			$I_O- = 200$ mA, $V_{CC} = 15$ V		2.5	3.5	
			$I_O- = 5.0$ mA, $V_{CC} = 5.0$ V		0.25	0.35	
V_{OH}	Output Voltage HIGH		$V_{CC} = 15$ V, $I_O+ = 200$ mA	11	12.5		V
			$V_{CC} = 15$ V, $I_O+ = 100$ mA	12.75	13.3		
			$V_{CC} = 5.0$ V, $I_O+ = 100$ mA	2.75	3.3		
t_r	Rise Time of Output				100		ns
t_f	Fall Time of Output				100		ns
I_{DIS}	Discharge Leakage Current				20	100	nA
Δt_D	Matching Characteristics	Initial Timing Accuracy			0.1	2.0	%
		Timing Drift with Temperature			±10		ppm/°C
		Drift with Supply Voltage			0.2	0.5	% V

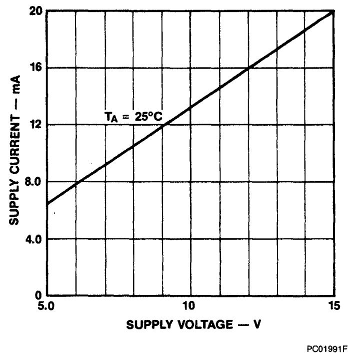
Notes
1. Supply current when output is HIGH is typically 1.0 mA less.
2. This will determine the maximum value of $R_1 + R_2$ for 15 V operation. The maximum total R = 10 MΩ.
3. Matching characteristics refer to the difference between performance characteristics of each timer section.

Typical Performance Curves

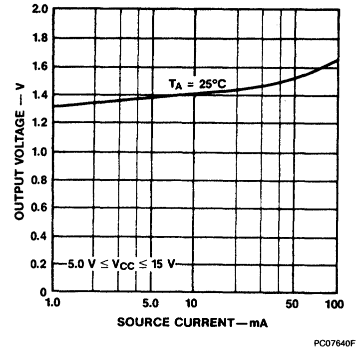
Minimum Pulse Width Required for Triggering



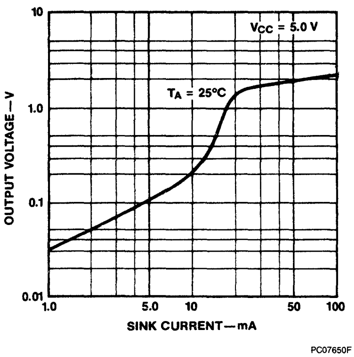
Total Supply Current vs Supply Voltage



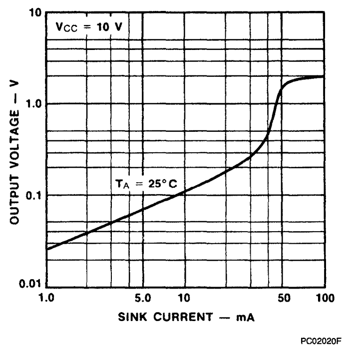
Output Voltage HIGH vs Output Source Current



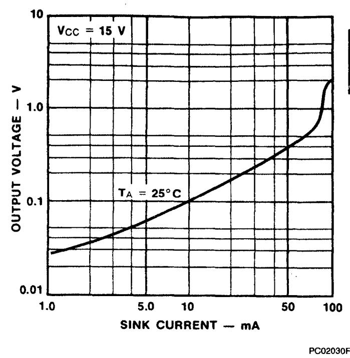
Output Voltage LOW vs Output Sink Current



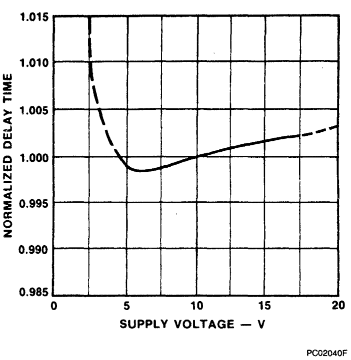
Output Voltage LOW vs Output Sink Current



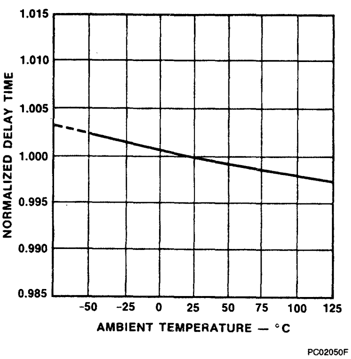
Output Voltage LOW vs Output Sink Current



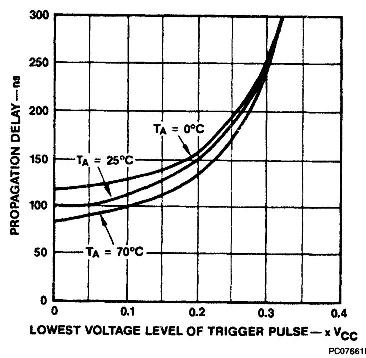
Delay Time vs Supply Voltage



Delay Time vs Ambient Temperature



Propagation Delay vs Voltage Level of Trigger Pulse



Typical Applications

Monostable Operation

In the monostable mode, the timer functions as a one shot. Referring to *Figure 1* the external capacitor is initially held discharged by a transistor inside the timer.

When a negative trigger pulse is applied to lead 6, the flip-flop is set, releasing the short circuit across the external capacitor and drives the output HIGH. The voltage across the capacitor, increases exponentially with the time constant $\tau = R1C1$. When the voltage across the capacitor equals ⅔ V_{CC}, the comparator resets the flip-flop which then discharges the capacitor rapidly and drives the output to its LOW state. *Figure 2* shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches ⅓ V_{CC}. Once triggered, the circuit remains in this state until the set time has elapsed, even if it is triggered again during this interval. The duration of the output HIGH state is given by $t = 1.1\ R1C1$ and is easily determined by *Figure 3*. Notice that since the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the Reset terminal (lead 4) and the trigger terminal (lead 6) during the timing cycle discharges the external capacitor and causes the cycle to start over. The timing cycle now starts on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its LOW state.

When Reset is not used, it should be tied HIGH to avoid any possibility of false triggering.

Figure 1 Monostable Mode

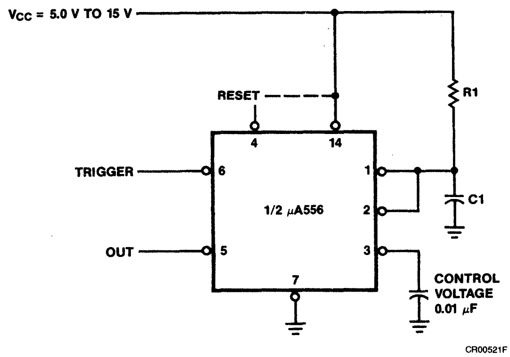


Figure 2 Monostable Waveform

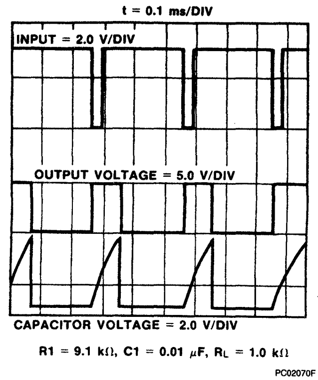
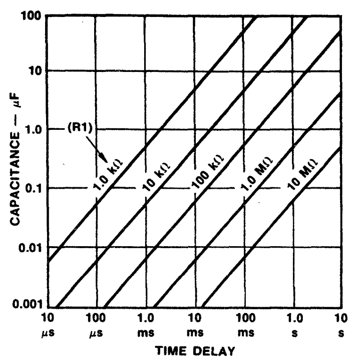


Figure 3 Time Delay vs R1 and C1



Astable Operation

When the circuit is connected as shown in *Figure 4* (leads 2 and 6 connected), it triggers itself and free runs as a multivibrator. The external capacitor charges through R1 and R2 and discharges through R2 only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In the astable mode of operation, C1 charges and discharges between $\frac{1}{3}$ V_{CC} and $\frac{2}{3}$ V_{CC}. As in the triggered mode, the charge and discharge times and therefore frequency are independent of the supply voltage.

Figure 5 shows actual waveforms generated in this mode of operation.

The charge time (output HIGH) is given by:

$$t_1 = 0.693\ (R1 + R2)\ C1$$

and the discharge time (output LOW) by:

$$t_2 = 0.693\ (R2)\ C1$$

Thus the total period T is given by:

$$T = t_1 + t_2 = 0.693\ (R1 + 2R2)\ C1$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R1 + 2R2)\ C1}$$

and may be easily found by *Figure 6.*

The duty cycle is given by:

$$DC = \frac{R2}{R1 + 2R2}$$

Figure 4 Astable Mode

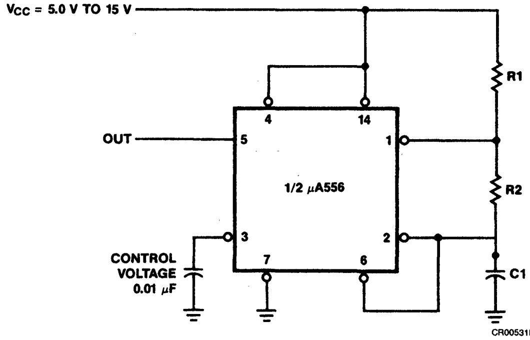
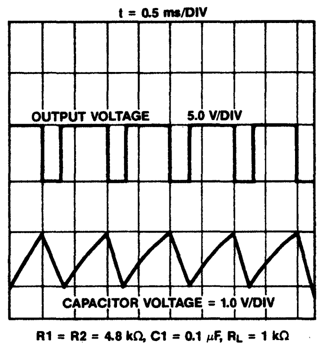


Figure 5 Astable Waveform



R1 = R2 = 4.8 kΩ, C1 = 0.1 μF, R_L = 1 kΩ

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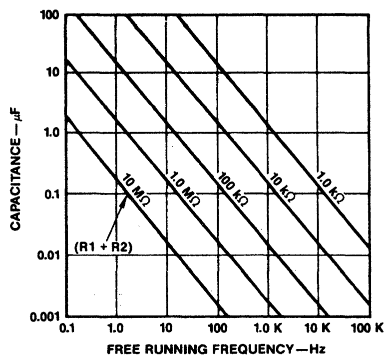
Figure 6 Free Running Frequency vs R1, R2 and C1



PC02231F

FAIRCHILD

A Schlumberger Company

μA592 Differential Video Amplifier

Linear Division Special Functions

Description

The μA592 is a monolithic two-stage differential input, differential output video amplifier constructed using the Fairchild Planar Epitaxial process. Internal series shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current source biased to obtain high power supply and common mode rejection ratios.

The μA592, in the 14-lead version, offers fixed gains of 100 and 400 without external components. A fixed gain of 400 is available in the 8-lead part. Adjustable gains from 0 to 400 are obtained with one external resistor.

No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding. Other applications include general purpose video and pulse amplifiers.

- **90 MHz Bandwidth Typ**
- **Selectable Gains From 0 To 400 Typ**
- **No Frequency Compensation Required**
- **Adjustable Pass Band**

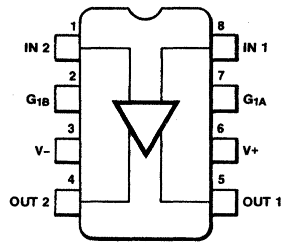
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP, SO-8	−65°C to +150°C
Operating Temperature Range	
Extended (μA592M)	−55°C to +125°C
Commercial (μA592C)	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO Package (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
8L-Molded DIP	0.93 W
SO-8	0.81 W
14L-Molded DIP	1.04 W
14L-Ceramic DIP	1.36 W
Supply Voltage	±8.0 V
Differential Input Voltage	±5.0 V
Common Mode Input Voltage	±6.0 V
Output Current	10 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SOIC, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Molded DIP at 7.5 mW/°C, the SO-8 at 6.5 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the 14L-Ceramic DIP at 9.1 mW/°C.

Connection Diagram 8-Lead DIP and SO-8 Package (Top View)

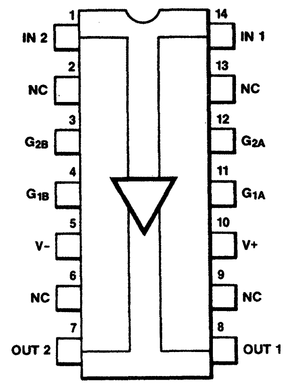


CD01230F

Order Information

Device Code	Package Code	Package Description
μA592TC	9T	Molded DIP
μA592SC	KC	Molded Surface Mount

Connection Diagram 14-Lead DIP (Top View)

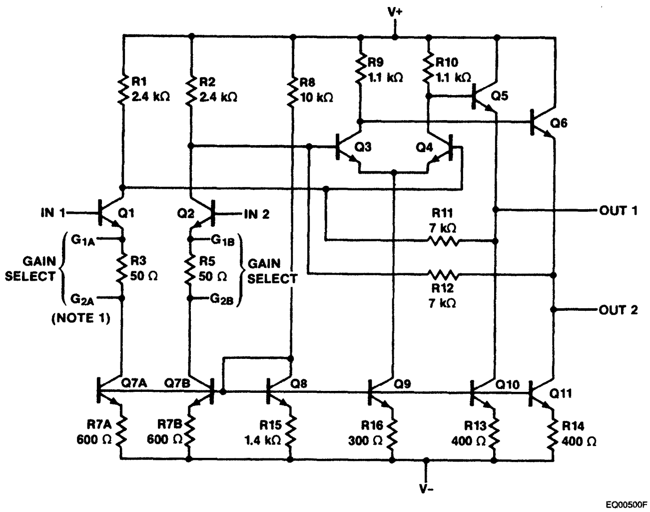


CD01240F

Order Information

Device Code	Package Code	Package Description
μA592DM	6A	Ceramic DIP
μA592DC	6A	Ceramic DIP
μA592PC	9A	Molded DIP

Equivalent Circuit



Note

1. G_{2A} and G_{2B} applies to 14 lead device only.

μA592 and μA592C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 6.0$ V unless otherwise specified.

Symbol	Characteristic	Condition[1, 2]		μA592 Min	μA592 Typ	μA592 Max	μA592C Min	μA592C Typ	μA592C Max	Unit
A_{VD}	Differential Voltage Gain	$R_L = 2.0$ kΩ, $V_O = 3.0$ $V_{p\text{-}p}$	Gain 1	300	400	500	250	400	600	V/V
			Gain 2	90	100	110	80	100	120	
B_W	Bandwidth	$R_S = 50$ Ω	Gain 1		40			40		MHz
			Gain 2		90			90		
t_r	Risetime	$R_S = 50$ Ω, $V_O = 1.0$ $V_{p\text{-}p}$	Gain 1		10.5			10.5		ns
			Gain 2		4.5	10		4.5	12	
t_{PD}	Propagation Delay	$R_S = 50$ Ω, $V_O = 1.0$ $V_{p\text{-}p}$	Gain 1		7.5			7.5		ns
			Gain 2		6.0	10		6.0	10	
Z_I	Input Impedance		Gain 1		4.0			4.0		kΩ
			Gain 2	20	30		10	30		
C_I	Input Capacitance		Gain 2		2.0			2.0		pF
I_{IO}	Input Offset Current				0.4	3.0		0.4	5.0	μA
I_{IB}	Input Bias Current				9.0	20		9.0	30	μA
e_n	Input Noise Voltage	$R_S = 50$ Ω, BW = 1.0 kHz to 10 MHz			12			12		μV_{rms}

μA592 and μA592C (Cont.)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 6.0$ V unless otherwise specified.

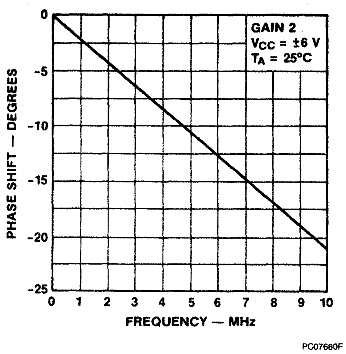
Symbol	Characteristic	Condition[1, 2]	μA592 Min	μA592 Typ	μA592 Max	μA592C Min	μA592C Typ	μA592C Max	Unit
V_{IR}	Input Voltage Range		±1.0			±1.0			V
CMR	Common Mode Rejection	$V_{CM} = 1.0$ V, Gain 2	60	86		60	86		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_{CC} = \pm 0.5$ V, Gain 2	50	70		50	70		dB
V_{OO}	Output Offset Voltage	Gain 1		0.6	1.5		0.6	1.5	V
		Gain 2		0.35	0.75		0.35	0.75	
V_{OCM}	Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OP}	Output Voltage Swing		3.0	4.0		3.0	4.0		V_{p-p}
I_{O-}	Output Sink Current		2.5	3.6		2.5	3.6		mA
R_O	Output Resistance			20			20		Ω
I_{CC}	Supply Current			18	24		18	24	mA

Notes

1. Gain Select leads G_{1A} and G_{1B} connected together for Gain 1 and Gain Select leads G_{2A} and G_{2B} connected together for Gain 2.
2. Gain 2 not applicable to 8 lead device.

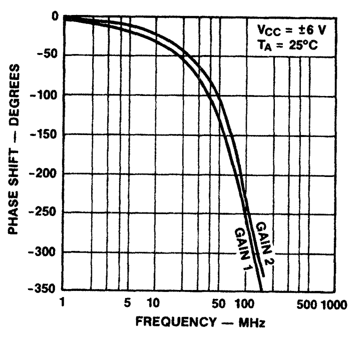
Typical Performance Curves

Phase Shift vs Frequency



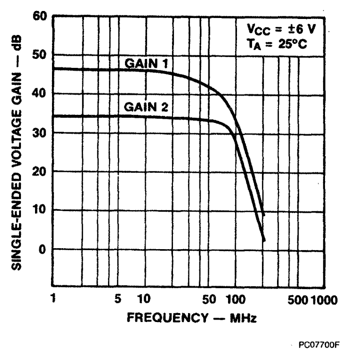
PC07680F

Phase Shift vs Frequency



PC07690F

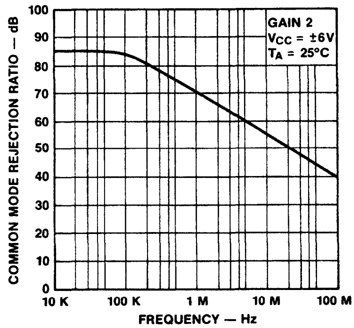
Voltage Gain vs Frequency



PC07700F

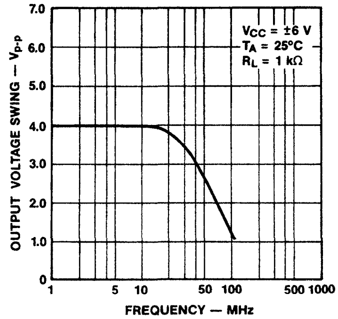
Typical Performance Curves (Cont.)

Common Mode Rejection Ratio vs Frequency



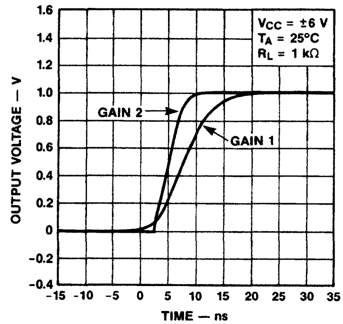
PC07710F

Output Voltage Swing vs Frequency



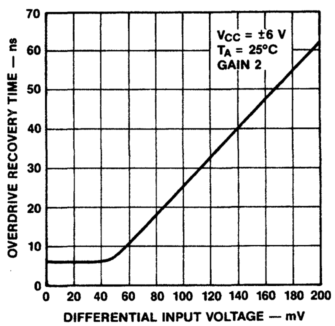
PC07720F

Pulse Response



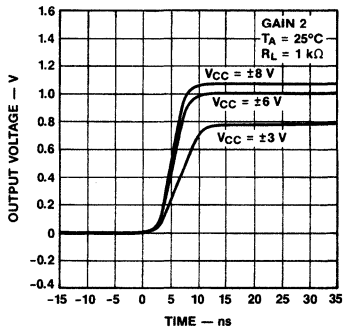
PC07730F

Differential Overdrive Recovery Time



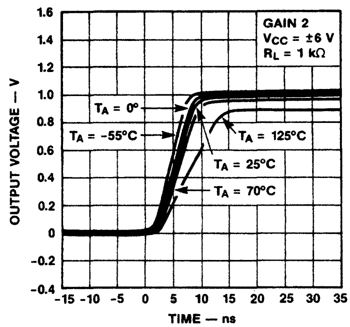
PC07740F

Pulse Response vs Supply Voltage



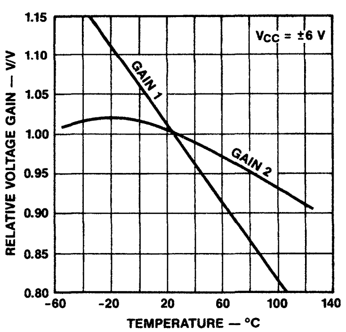
PC07750F

Pulse Response vs Temperature



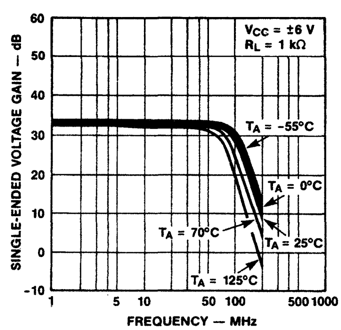
PC07760F

Voltage Gain vs Temperature



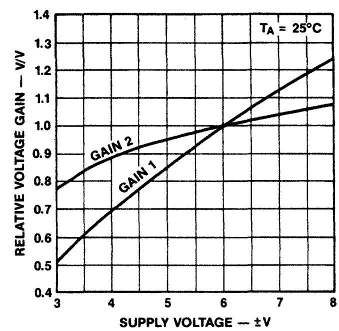
PC07770F

Gain vs Frequency vs Temperature



PC07780F

Voltage Gain vs Supply Voltage

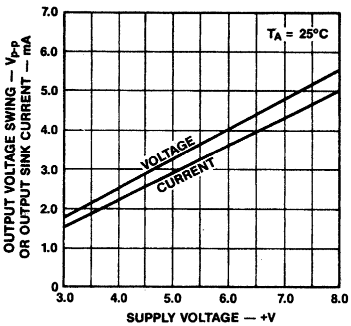


PC07790F

11

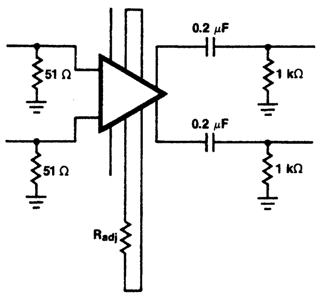
Typical Performance Curves (Cont.)

Output Voltage and Current Swing vs Supply Voltage



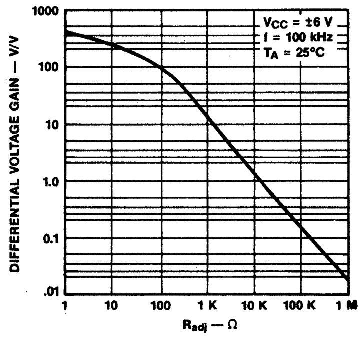
PC07800F

Voltage Gain Adjust Circuit



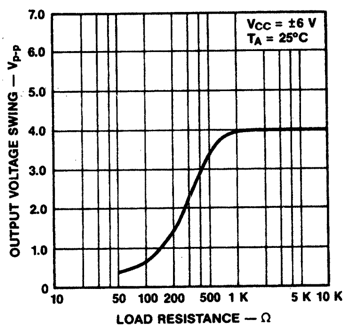
PC07671F

Voltage Gain vs R_{ADJ}



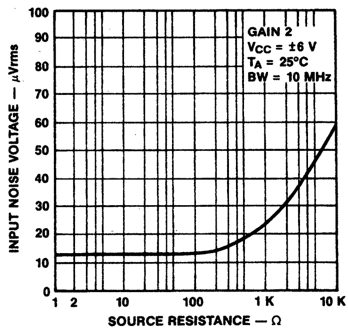
PC07810F

Output Voltage Swing vs Load Resistance



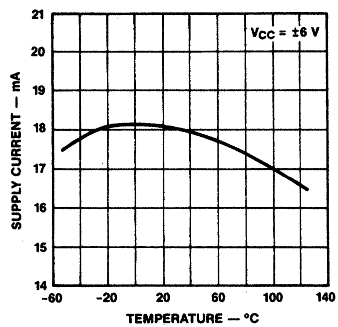
PC07820F

Input Noise Voltage vs Source Resistance



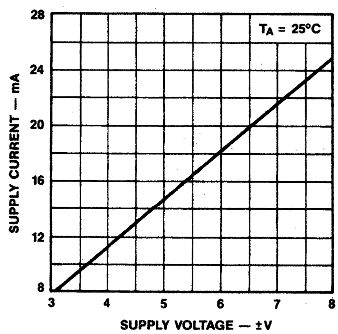
PC07830F

Supply Current vs Temperature



PC07840F

Supply Current vs Supply Voltage



PC07850F

FAIRCHILD

A Schlumberger Company

μA733
Differential Video Amplifier

Linear Division Special Functions

Description

The μA733 is a monolithic two-stage differential input, differential output video amplifier constructed using the Fairchild Planar Epitaxial process. Internal series shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

- **120 MHz Bandwidth Typ**
- **250 kΩ Input Resistance Typ**
- **Selectable Gains Of 10, 100, And 400**
- **No Frequency Compensation Required**

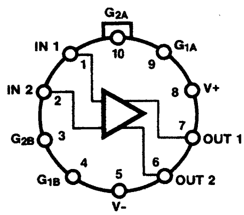
Absolute Maximum Ratings

Storage Temperature Range	
Metal Can and Ceramic DIP	−65°C to +175°C
Molded DIP and SO-14	−65°C to +150°C
Operating Temperature Range	
Extended (μA733M)	−55°C to +125°C
Commercial (μA733C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
10L-Metal Can	1.07 W
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	±8.0 V
Differential Input Voltage	±5.0 V
Common Mode Input Voltage	±6.0 V
Output Current	10 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

Connection Diagram
10-Lead Metal Package
(Top View)



CD01250F

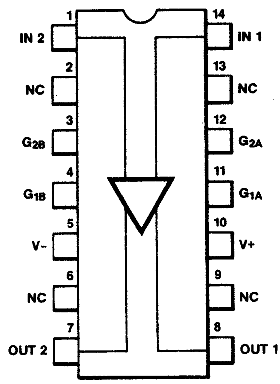
Note

Pin 5 connected to case.

Order Information

Device Code	Package Code	Package Description
μA733HM	5X	Metal
μA733HC	5X	Metal

Connection Diagram
14-Lead DIP and SO-14 Package
(Top View)

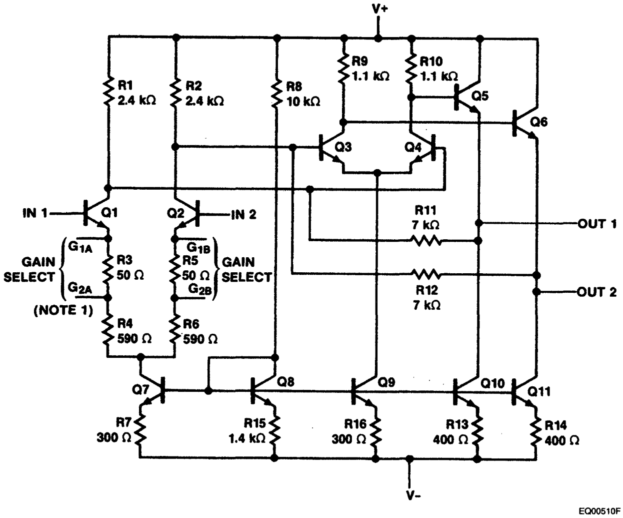


CD01240F

Order Information

Device Code	Package Code	Package Description
μA733DM	6A	Ceramic DIP
μA733DC	6A	Ceramic DIP
μA733PC	9A	Molded DIP
μA733SC	KD	Molded Surface Mount

Equivalent Circuit



μA733 and μA733C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 6.0$ V unless otherwise specified.

Symbol	Characteristic	Condition[1]		μA733 Min	μA733 Typ	μA733 Max	μA733C Min	μA733C Typ	μA733C Max	Unit
A_{VD}	Differential Voltage Gain		Gain 1	300	400	500	250	400	600	V/V
			Gain 2	90	100	110	80	100	120	
			Gain 3	9.0	10	11	8.0	10	12	
BW	Bandwidth	$R_S = 50\ \Omega$	Gain 1		40			40		MHz
			Gain 2		90			90		
			Gain 3		120			120		
t_r	Risetime	$R_S = 50\ \Omega$, $V_O = 1.0\ V_{p\text{-}p}$	Gain 1		10.5			10.5		ns
			Gain 2		4.5	10		4.5	12	
			Gain 3		2.5			2.5		
t_{PD}	Propagation Delay	$R_S = 50\ \Omega$, $V_O = 1.0\ V_{p\text{-}p}$	Gain 1		7.5			7.5		ns
			Gain 2		6.0	10		6.0	10	
			Gain 3		3.6			3.6		
Z_I	Input Impedance		Gain 1		4.0			4.0		kΩ
			Gain 2	20	30		10	30		
			Gain 3		250			250		
C_I	Input Capacitance		Gain 2		2.0			2.0		pF
I_{IO}	Input Offset Current				0.4	3.0		0.4	5.0	μA

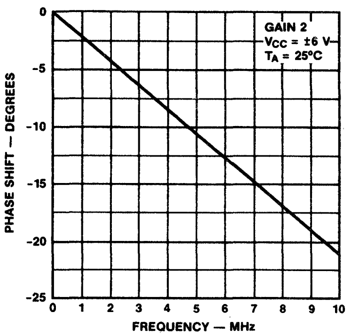
μA733 and μA733C (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 6.0$ V unless otherwise specified.

Symbol	Characteristic	Condition[1]	μA733 Min	μA733 Typ	μA733 Max	μA733C Min	μA733C Typ	μA733C Max	Unit
I_{IB}	Input Bias Current			9.0	20		9.0	30	μA
e_n	Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1.0 kHz to 10 MHz		12			12		μV_{rms}
V_{IR}	Input Voltage Range		±1.0			±1.0			V
CMR	Common Mode Rejection	$V_{CM} = \pm 1.0$ V, Gain 2	60	86		60	86		dB
PSRR	Supply Voltage Rejection Ratio	$\Delta V_{CC} = \pm 0.5$ V, Gain 2	50	70		50	70		dB
V_{OS}	Output Offset Voltage	Gain 1		0.6	1.5		0.6	1.5	V
		Gain 2 and Gain 3		0.35	1.0		0.35	1.5	
V_{OCM}	Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OP}	Output Voltage Swing		3.0	4.0		3.0	4.0		V_{p-p}
I_{O-}	Output Sink Current		2.5	3.6		2.5	3.6		mA
R_O	Output Resistance			20			20		Ω
I_{CC}	Supply Current			18	24		18	24	mA
The following specifications apply over the range of $-55°C \leqslant T_A \leqslant 125°C$ for μA733 and $0°C \leqslant T_A \leqslant 70°C$ for μA733C.									
A_{VD}	Differential Voltage Gain	Gain 1	200		600	250		600	V/V
		Gain 2	80		120	80		120	
		Gain 3	8.0		12	8.0		12	
Z_I	Input Impedance	Gain 2	8.0			8.0			kΩ
I_{IO}	Input Offset Current				5.0			6.0	μA
I_{IB}	Input Bias Current				40			40	μA
V_{IR}	Input Voltage Range		±1.0			±1.0			V
CMR	Common Mode Rejection		50			50			dB
PSRR	Power Supply Rejection Ratio		50			50			dB
V_{OS}	Output Offset Voltage	Gain 1			1.5			1.5	V
		Gain 2 and Gain 3			1.2			1.5	
V_{OP}	Output Swing		2.5			2.8			V_{p-p}
I_{O-}	Output Sink Current		2.2			2.5			mA
I_{CC}	Supply Current				27			27	mA

Notes
1. Gain Select leads G_{1A} and G_{1B} connected together for Gain 1.
2. Gain Select leads G_{2A} and G_{2B} connected together for Gain 2.
3. All Gain Select leads open for Gain 3.

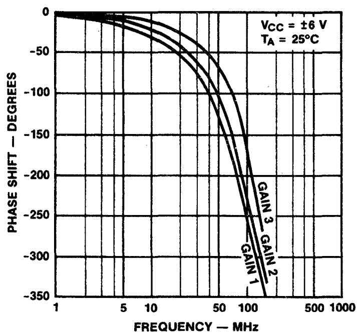
Typical Performance Curves

Phase Shift vs Frequency



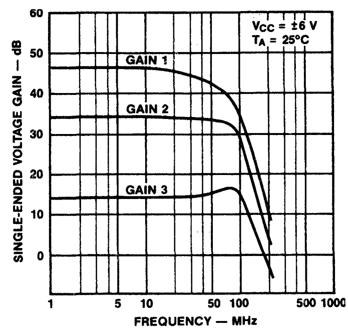
PC07860F

Phase Shift vs Frequency



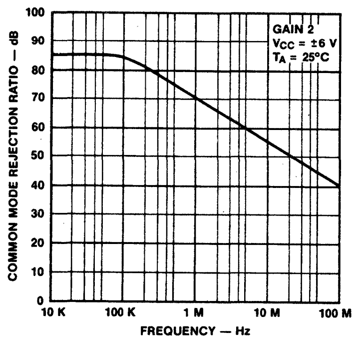
PC07870F

Voltage Gain vs Frequency



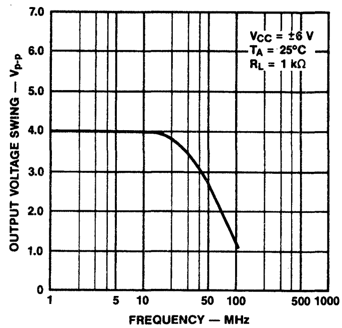
PC07880F

Common Mode Rejection Ratio vs Frequency



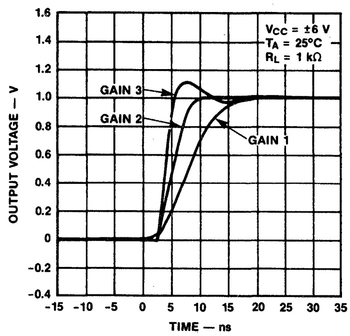
PC07890F

Output Voltage Swing vs Frequency



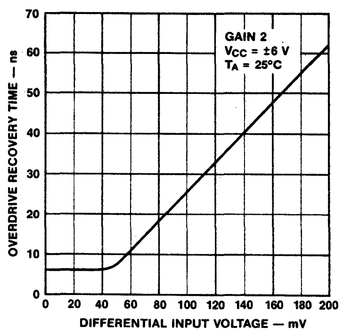
PC07900F

Pulse Response



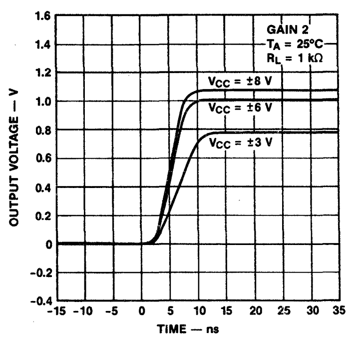
PC07910F

Differential Overdrive Recovery Time



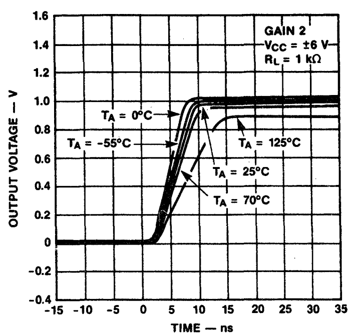
PC07920F

Pulse Response vs Supply Voltage



PC07930F

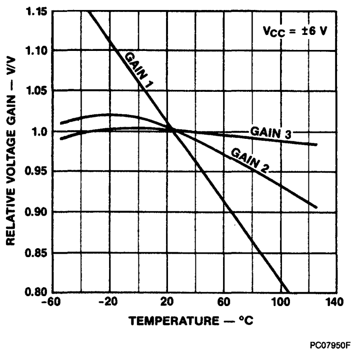
Pulse Response vs Temperature



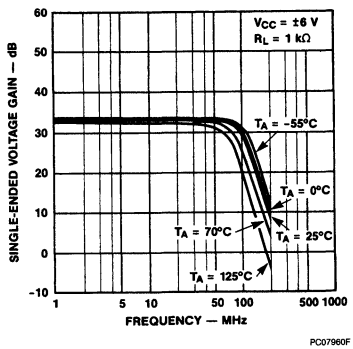
PC07940F

Typical Performance Curves (Cont.)

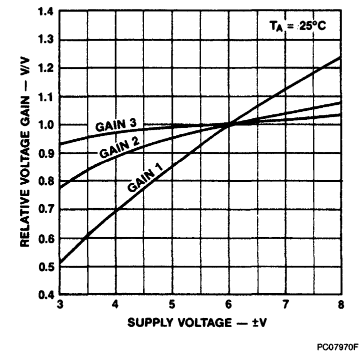
Voltage Gain vs Temperature



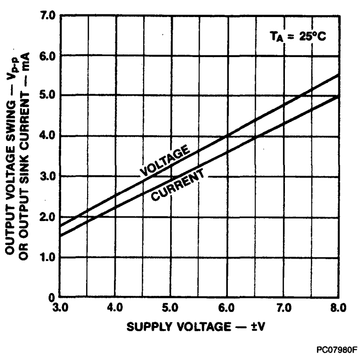
Gain vs Frequency vs Temperature



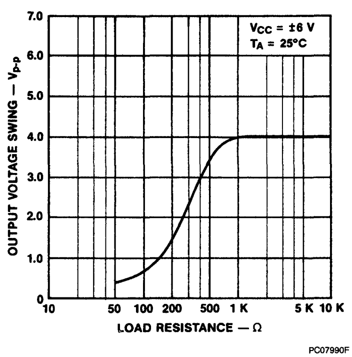
Voltage Gain vs Supply Voltage



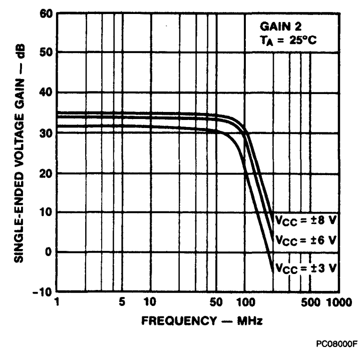
Output Voltage and Current Swing vs Supply Voltage



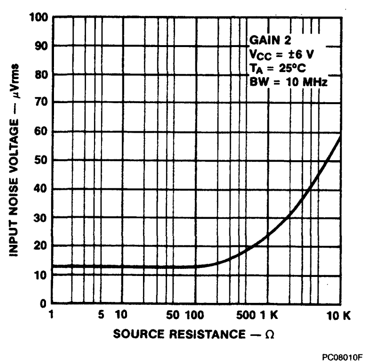
Output Voltage Swing vs Load Resistance



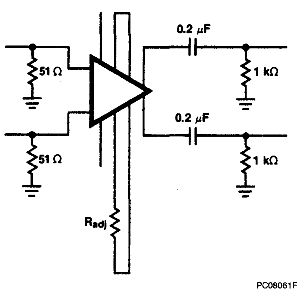
Gain vs Frequency vs Supply Voltage



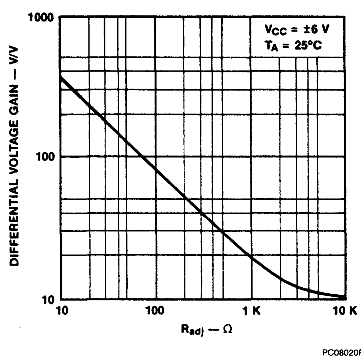
Input Noise Voltage vs Source Resistance



Voltage Gain Adjust Circuit

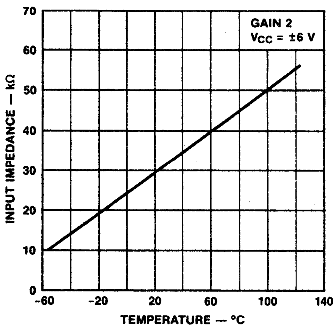


Voltage Gain vs R_{adj}



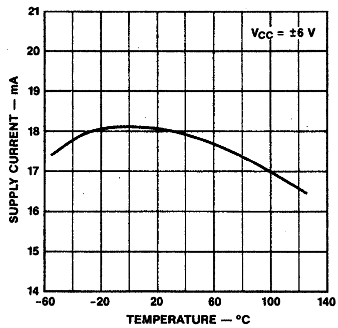
Typical Performance Curves (Cont.)

Input Impedance vs Temperature



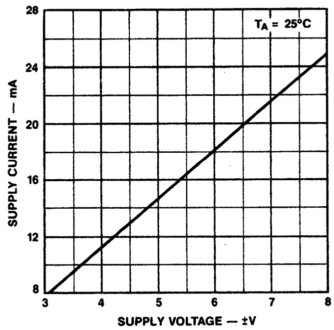
PC08030F

Supply Current vs Temperature



PC08040F

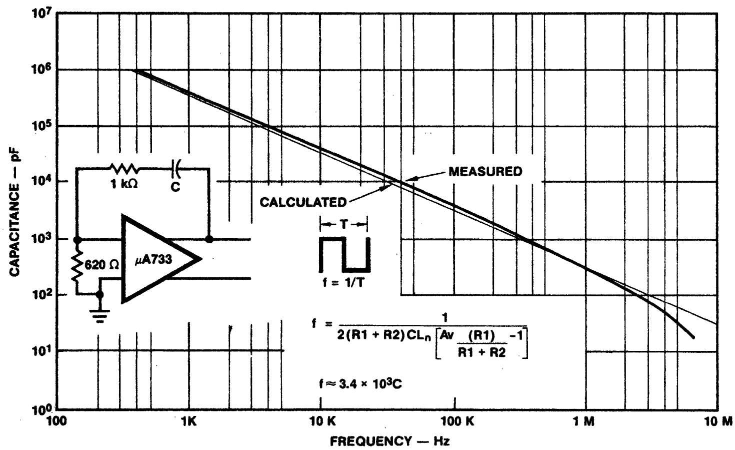
Supply Current vs Supply Voltage



PC08050F

Typical Applications

Oscillator Frequency for Various Capacitor Values



PC08070F

FAIRCHILD

A Schlumberger Company

μA7392 DC Motor Speed Control Circuit

Linear Division Special Functions

Description

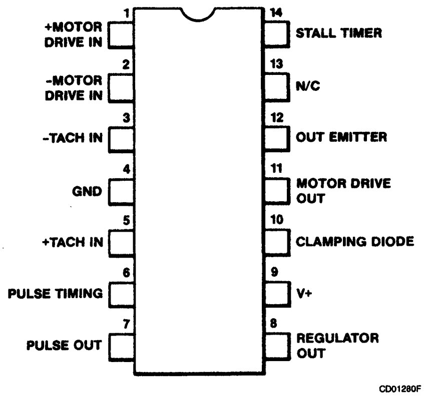
The μA7392 is designed for precision, closed loop, motor speed control systems. It regulates the speed of capstan drive motors in automotive and portable tape players and is useful in a variety of industrial and military control applications, e.g., floppy disc drive systems and data cartridge drive systems. The device is constructed using the Fairchild Planar Epitaxial process.

The μA7392 compares actual motor speed to an externally presettable reference voltage. The motor speed is determined by frequency to voltage conversion of the input signal provided by the tachometer generator. The result of the comparison controls the duty cycle of the pulse width modulated switching motor drive output stage to close the system's negative feedback loop.

Thermal and over voltage shutdown are included for self-protection, and a stall-timer feature allows the motor to be protected from burn out during extended mechanical jams.

- **Precision Performance**
- **High Current Performance**
- **Wide Range Tachometer Input**
- **Thermal Shutdown, Over Voltage And Stall Protection**
- **Internal Regulator**
- **Wide Supply Voltage Range 6.3 V To 16 V**

Connection Diagram 14-Lead DIP (Top View)



Order Information

Device Code	Package Code	Package Description
μA7392DV	6A	Ceramic DIP
μA7392PV	9A	Molded DIP

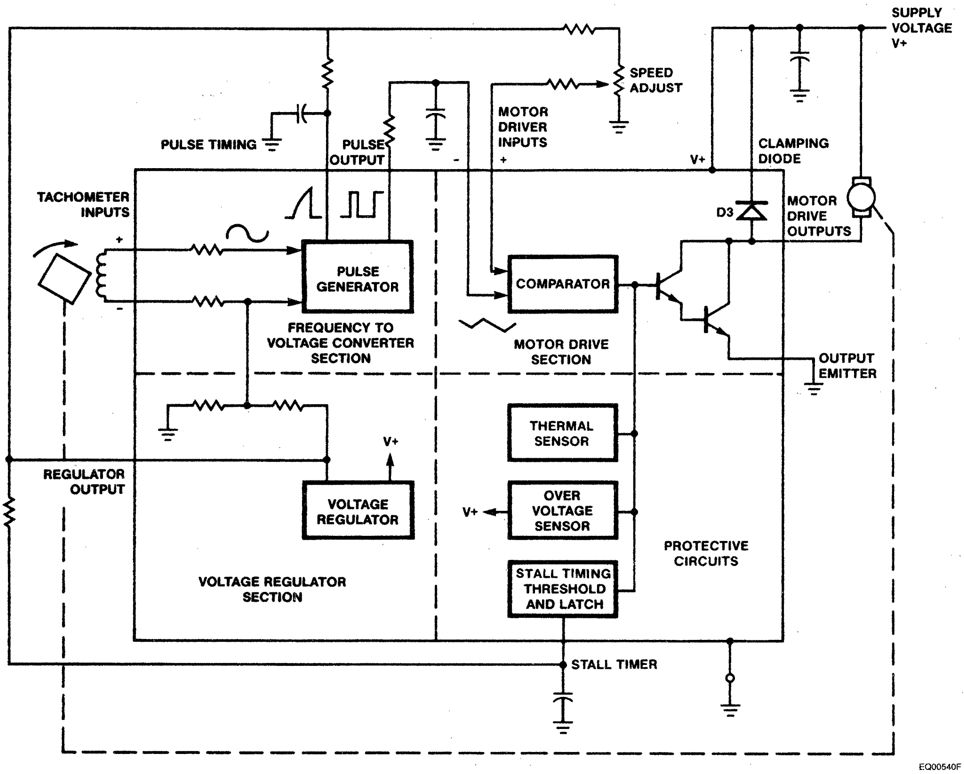
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1-3]	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
Supply Voltage (V+), V_9, V_{10}, V_{11}	24 V
Regulator Output Current, I_8	15 mA
Voltage Applied to Lead 6 (Tachometer Pulse Timing)	7.0 V
Voltage Applied Between Leads 3 and 5 (Tachometer Inputs)	±6.0 V
Continuous Current through Leads 11 and 12 Motor Drive Output ON	0.3 A
Repetitive Surge Current through Leads 11 and 12 (Motor Drive ON)	1.0 A
Repetitive Surge Current through Leads 10 and 11 (Motor Drive OFF)	0.3 A

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C.
3. Internally Limited.

Block Diagram



μA7392

Electrical Characteristics $T_A = 25°C$, V+ = 14.5 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Voltage Regulator Section (Test Circuit 1)						
I_{CC}	Supply Current	Excluding Current into Lead 11		7.5	10	mA
V_{Reg}	Regulator Output Voltage		4.5	5.0	5.5	V
$LINE_{Reg}$	Regulator Output Line Regulation (ΔV_8)	V+ = 10 V to 16 V		6.0	20	mV
		V+ = 6.3 V to 16 V		12	50	
$LOAD_{Reg}$	Regulator Output Load Regulation (ΔV_8)	I_8 from 10 mA to 0		40		mV
Frequency to Voltage Converter Section (Test Circuit 2)						
V_{IN}	Tachometer (−) Input Bias Voltage			2.4		V
I_{IN}	Tachometer (+) Input Bias Current	$V_5 = V_3$		1.0	10	μA
V_{DIFF}	Tachometer Input Positive Threshold	$(V_5 - V_3)$	10	25	50	mV_{p-p}
V_{HY}	Tachometer Input Hysteresis		20	50	100	mV_{p-p}
R	Pulse Timing ON Resistance	$V_6 = 1.0$ V		300	500	Ω
V_{TH}	Pulse Timing Switch Threshold		45	50	55	$\%V_8$
t_r	Output Pulse Rise Time			0.3		μs
t_f	Output Pulse Fall Time			0.1		μs
$V_{Sat\text{-}LOW}$	Pulse Output LOW Saturation (V_7)			0.13	0.25	V
$V_{Sat\text{-}HI}$	Pulse Output HIGH Saturation ($V_8 - V_7$)			0.12	0.2	V
I_{Source}	Pulse Output HIGH Source Current	$V_7 = 1.0$ V	−340	−260	−180	μA
SVS	Frequency-to-Voltage Conversion Supply Voltage Stability[1]	$V_{FV} = 0.25\ V_8{}^2$ $V_+ = 10$ V to 16 V		0.1		%
TS	Frequency-to-Voltage Conversion Temperature Stability[3]	$V_{FV} = 0.25\ V_8{}^2$ $T_A = -40°C$ to $+85°C$		0.3		%
Motor Drive Section						
V_{IO}	Input Offset Voltage				20	mV
I_{IB}	Input Bias Current			0.1	10	μA
CMR	Common Mode Range		0.8		2.5	V
V_{SAT}	Motor Drive Output Saturation	$I_{11} = 300$ mA		1.3	2.0	V
I_{LEAK}	Motor Drive Output Leakage	$V_{11} = V_{10} = 16$ V			5.0	μA
I_D	Flyback Diode Leakage	$V_{10} = 16$ V, $V_{11} = 0$ V			30	μA

μA7392 (Cont.)

Electrical Characteristics T_A = 25°C, V+ = 14.5 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_D	Flyback Diode Clamp Voltage	I_{11} = 300 mA Motor Drive Output OFF		1.1	1.3	V
Protective Circuits						
J-T°C	Thermal Shutdown Junction Temperature[4]			160		°C
Over Voltage	Overvoltage Shutdown[4]		18	21	24	V
V_{TH}	Stall Timer Threshold Voltage[5]		2.5	2.9	3.5	V
I_{TH}	Stall Timer Threshold Current[5]			0.3	3.0	μA

Notes

1. Frequency-to-voltage conversion, supply voltage stability is defined as:

$$\frac{V_{FV}(16\ V)}{V_8(16\ V)} - \frac{V_{FV}(10\ V)}{V_8(10\ V)} \div \frac{V_{FV}(14.5\ V)}{V_8(14.5\ V)} \times 100\%$$

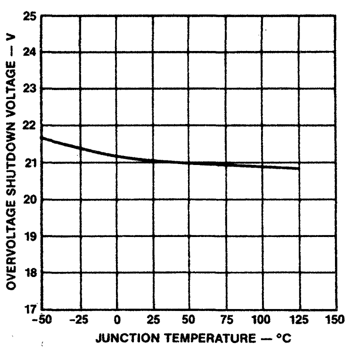
2. V_{FV} is the integrated DC output voltage from the pulse generator (Lead 7)
3. Frequency-to-voltage conversion temperature stability is defined as:

$$\frac{V_{FV}(85°C)}{V_8(85°C)} - \frac{V_{FV}(-40°C)}{V_8(-40°C)} \div \frac{V_{FV}(25°C)}{V_8(25°C)} \times 100\%$$

4. Motor Drive circuitry is disabled when these limits are exceeded. If the condition continues for the duration set by the external stall timer components, the circuit is latched off until reset by temporarily opening the power supply input line.
5. If stall timer protection is not required, lead 14 should be grounded.

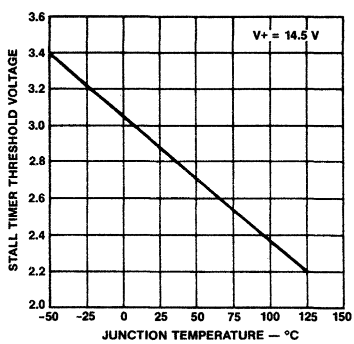
Typical Performance Curves

Overvoltage Shutdown Voltage vs Junction Temperature



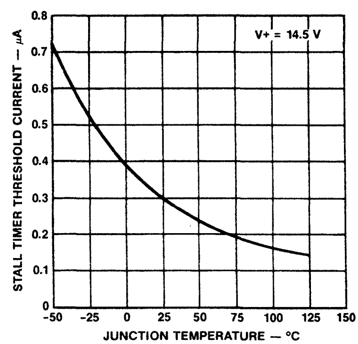
PC08340F

Stall Timer Threshold Voltage vs Junction Temperature



PC08350F

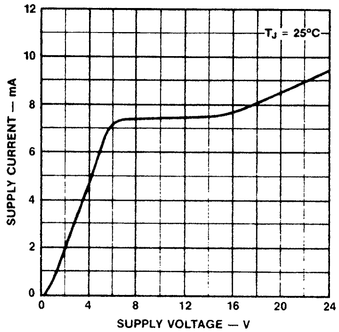
Stall Timer Threshold Current vs Junction Temperature



PC08360F

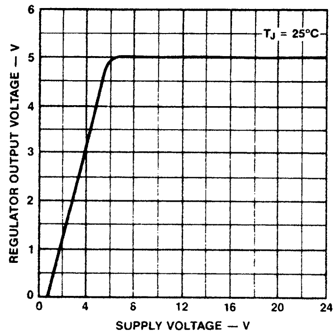
Typical Performance Curves (Cont.)

Supply Current vs Supply Voltage



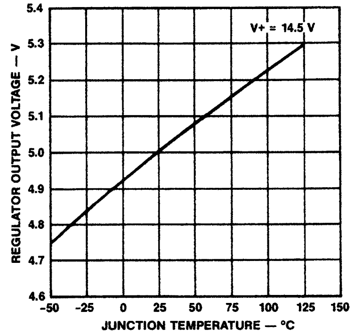
PC08370F

Regulator Output Voltage vs Supply Voltage



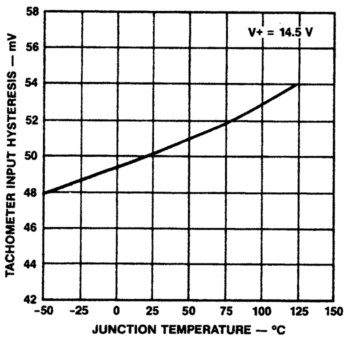
PC08380F

Regulator Output Voltage vs Junction Temperature



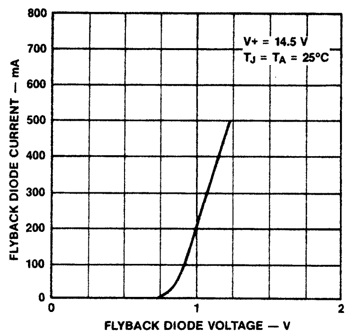
PC08390F

Tachometer Input Hysteresis vs Junction Temperature



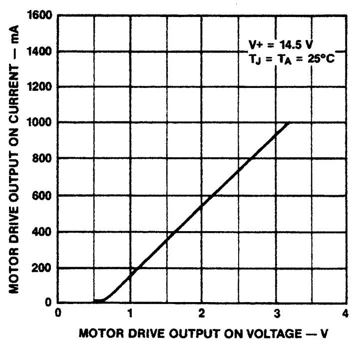
PC08400F

Flyback Diode Current (D3) vs Flyback Diode Voltage



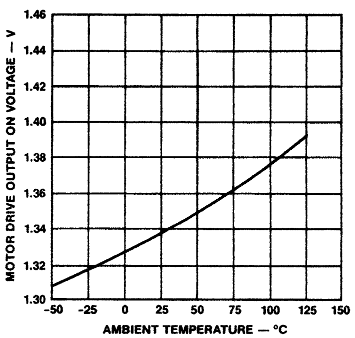
PC08410F

Motor Drive Output ON Current vs Motor Drive Output ON Voltage



PC08420F

Motor Drive Output ON Voltage vs Ambient Temperature

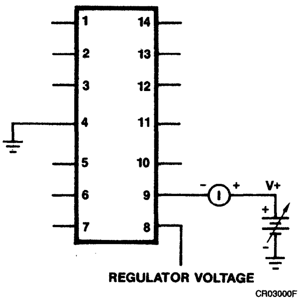


PC08430F

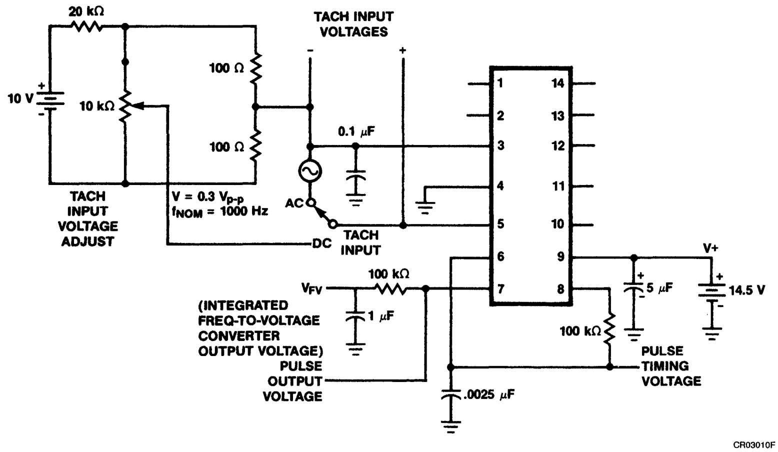
11

Test Circuits

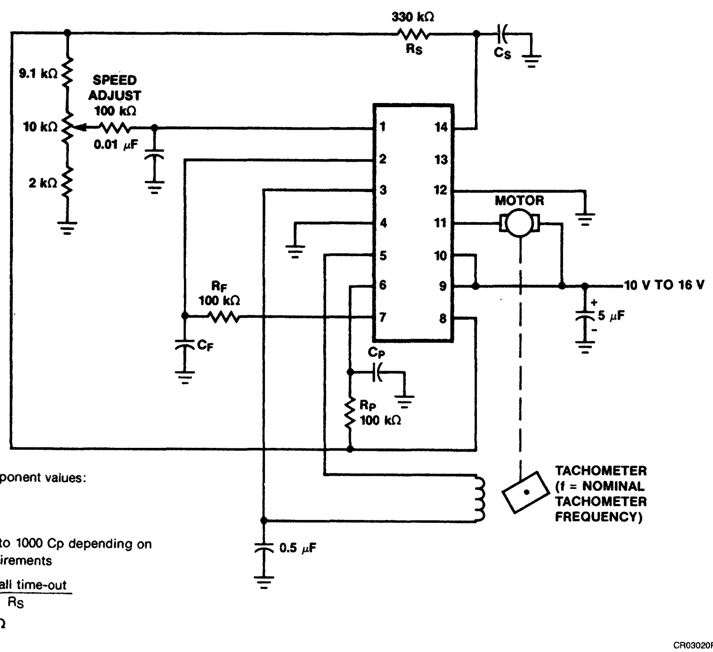
Test Circuit 1



Test Circuit 2



Typical Application Using Magnetic Tachometer



Typical component values:

$C_P = \frac{1}{4 R_{PF}}$

C_F = 10 Cp to 1000 Cp depending on system requirements

$C_S = \frac{2 \text{ X stall time-out}}{R_S}$

$R_{Motor} \geq 5\ \Omega$

FAIRCHILD
A Schlumberger Company

FSP100 Programmable Digital Filter

Preliminary

Advanced Signal Processing Division

Description

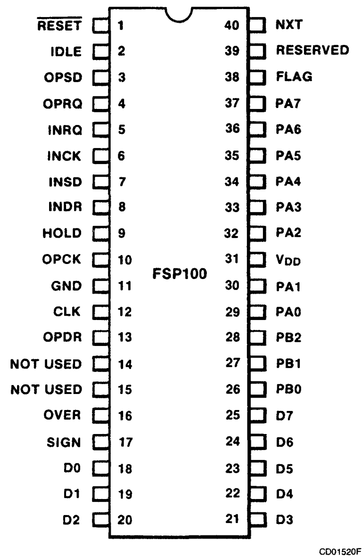
The Fairchild FSP100 is a device optimized for use in one dimensional data stream processing. It efficiently implements both recursive and non-recursive filter structures. It has, on-chip, all the functions necessary to perform most common filter primitives in a single instruction. The advanced architecture has separate data and instruction paths to avoid input-output bottlenecks, and utilizes a high performance crosspoint switch to efficiently route data between the processing elements. A transparent pipeline allows simultaneous instruction fetch, execution and data input/output. The serial data path permits variable data word lengths between 20 and 32-bits, which allows efficient single-chip implementations that have not been possible with previous single chip digital signal processors.

The FSP100 uses an external byte-wide program memory for maximum design flexibility without compromising performance. Multiprocessing is straightforward because the FSP100 is directly cascadeable.

The FSP100 instruction set implements familiar digital signal processing primitives such as Pole-pairs, Zeros, Peak Detectors and Oscillators.

The FSP100 comes with a comprehensive software support system, including an assembler and a simulator, which runs under the UNIX*, VMS** and MS-DOS operating systems. A hardware development system which allows real time verification of applications software completes the support package.

Connection Diagram (Top View)



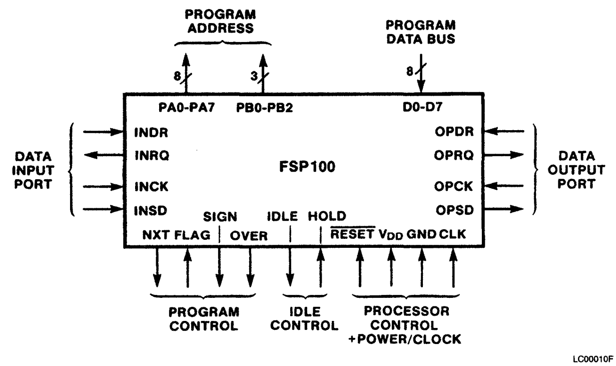
Order Information

Device Code	Package Code	Package Description
FSP100DC	Consult Factory	40-Lead Ceramic DIP
FSP100LC	Consult Factory	44-Lead LCC

- **Single-Chip Programmable Digital Filter**
- **Programmed in the Language of Filter Designers (in Terms of Poles and Zeros)**
- **Programmable Internal Data Word Lengths Between 20 and 32-Bits**
- **Executes Complete Filter Functions in a Single Instruction Cycle**
- **Triple Multiplier-Accumulator Provides 3 Million Multiplies Per Second**
- **Sample Rates up to 200 KHz for Single-Chip Applications**
- **Simply Cascade Processors with no Intermediate Logic for Higher Sample Rates**
- **Separate Data and Instruction Paths On- and Off-Chip**
- **Separate Processor and Data Input/Output Clocks for Ease of System Design**
- **Requires No External Synchronization Between Input/Output Clocks and Processor Clocks**
- **Optional Data Input and Output Formats and Word Lengths**
- **External Program Memory for Maximum Design Flexibility**
- **On-Chip Data Memory for Storing State Variables**
- **Complete Software and Hardware Support Package for Design Development**
- **Single-Phase 16 MHz Processor Clock Frequency**
- **Single-Phase 10 MHz Data Input and Output Clock Frequency**
- **40-Lead Ceramic DIP and 44-Lead LCC Packages**
- **TTL- and CMOS-Compatible Input/Outputs**
- **Full Performance Over −55°C to +125°C Operating Temperature Range**
- **2-Micron CMOS Process**

*A trademark of AT&T
**A trademark of Digital Equipment Corporation

Logic Symbol



Architecture

General Description

The data path contains all of the components necessary to execute a two-pole filter section with a single instruction:

- A triple multiplier-adder.
- An editing unit which modifies the result from the triple multiplier to obtain saturation and other non-linear effects.
- Scratch pad registers.
- An accumulator with extension bits and scaler.
- A sequential access memory with two data channels for state variable storage.
- A crosspoint switch for passing data between the blocks.
- An input and an output interface, which can synchronize the chip with the input and/or output data rate.

The control path is totally independent of the data path, thus eliminating the need for pipeline flushing. A simple program sequencer is provided on-chip, but a clock output is also provided for use with an external program sequencer, if desired. The major elements of the control path are:

- A program sequencer, providing branching and looping.
- An instruction decoder for configuring the crosspoint switch.
- A bus for distributing the instruction bytes for local decoding.

Triple Multiplier-Adder

Most of the arithmetic unit consists of a triple multiplier-adder. During each instruction cycle, it forms the sum of products:

$$R = Xg \cdot Gamma + Xa \cdot Alpha + Xb \cdot Beta$$

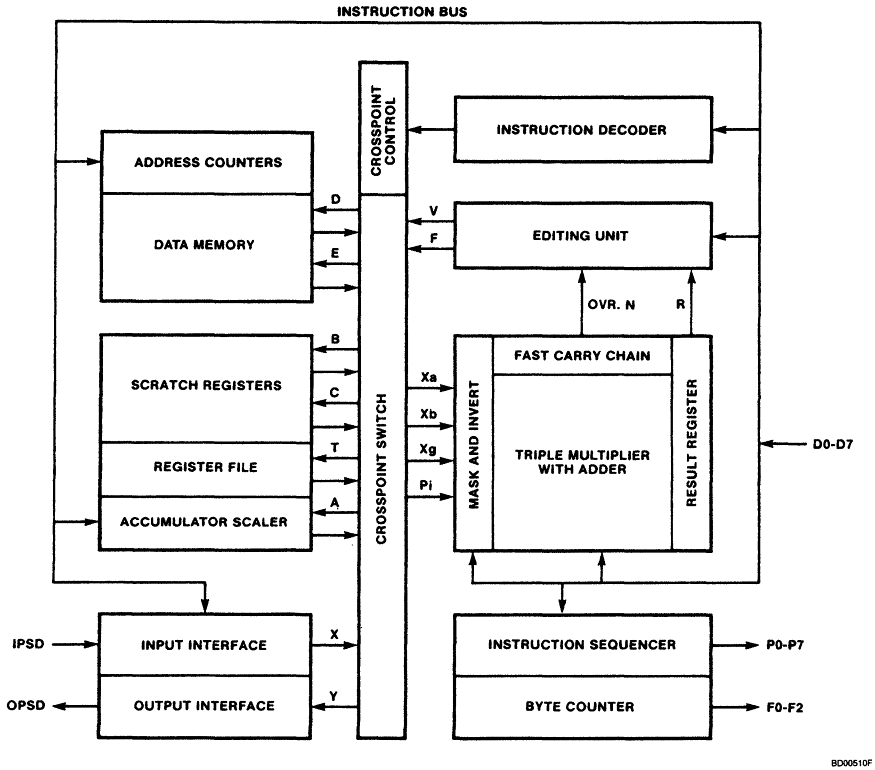
The X's are signal data streams emerging from the crosspoint switch. Alpha, Beta and Gamma are coefficients. Alpha is in the range −2 to +2. Beta is in the range −1 to +1. Gamma is normally a power of two scaling factor in the range of −2 to +2, but it is possible to feed signal data to the Gamma coefficient input to effect the signal-by-signal multiplications required for modulation, VCO's and time-varying filters.

Normally the multiplier rounds the final sum-of-products. However, recursive filtering instructions may invoke random switching between rounding and truncation in order to defeat limit cycles.

The triple multiplier includes a fast carry chain. This fast carry chain provides an overflow and sign output in advance of the serial data output, in order to control the saturation and non-linear function logic in the editing unit.

The triple multiplier uses Booth encoders operating directly on the incoming data bit-pairs. These Booth encoders can also perform non-linear functions. Signals from the control section can cause the input data streams to be masked to zero or inverted as they enter the arithmetic unit, to provide half or full wave rectification or a sign-dependent gain.

Figure 1 Block Diagram



Editing Unit
The primary function of the editing unit is to saturate the result from the multiplier to prevent overflow oscillations in recursive filters.

The saturation logic consists of a multiplexer which can select between the multiplier output, +1, −1 or 0. A control PLA sets the switches according to the FUNCTION code and the sign/overflow flags, to achieve either saturation or the more complex behavior required for the other non-linear operators.

Another function of the editing unit is to provide some commonly used, computationally simple filter zeros. This function allows execution of some biquadratic sections in a single instruction cycle. When this function is used, the output of the filter is different than the new value of the state variable (which needs to be stored in the data memory). There are, therefore, two outputs from the editing unit: one for the filter output, and the other for the new state variable value.

Scratch Pad Registers
The scratch pad registers are a group of six variable-length registers. Two registers serve as working stores; each one is connected between a crosspoint switch output and input. The use of these registers is determined by the FUNCTION code.

A dual-port connects another crosspoint switch output and input four-word register file. This register file is directly addressable by an instruction field. It can be used to store intermediate results for more complex filter topologies.

Accumulator
An accumulator is also connected to an output from the crosspoint switch. It is used primarily for implementing FIR and parallel IIR summing nodes. It has six extension bits

which permit accumulation of up to 64 values without the risk of overflow. The accumulator output is connected to a crosspoint switch input via a power-of-four scaling circuit, the scaling factor being determined by the SETUP instruction.

Data Memory
The data memory is organized as a 64-column, 32-row array of 2-port, 3-transistor RAM cells. It functions logically as an adjustable length shift register, with two data channels each two bits wide. The length of the "shift register" is set up during initialization.

The rows are written sequentially. Each row receives 16 bits from each of four input bit streams (two data channels) for an effective register length of a multiple of 32 bits per channel. Adjustable length shift registers on the input increase the length resolution to four bits per channel.

The serial access memory restricts operation to algorithms in which the data flows in an ordered stream, such as filters and correlators. However, this memory organization can efficiently store data of arbitrary word length. Also, the instruction word does not require a memory address field.

Input and Output
The input/output data is single bit wide serial with four possible arithmetic formats. It may be either most- or least-significant bit first. The input and output word lengths are independent both of each other and of the internal word length.

Associated with both the input and output port are two handshake lines; one indicates that the external device is ready, the other that the FSP100 is ready. The FSP100 can suppress its ready signal until the external device is ready, thus enabling the processor to directly control the transfer.

The input and output ports each have their own clock. These clocks may be asynchronous with respect to each other and with respect to the processor clock. The interface logic is designed to have an arbitrarily low error rate without reducing the interface throughput.

While the processor is waiting for an external device to become ready, the I/O interface stops the execution of the program. Execution resumes upon completion of the I/O transfer. The processor thus synchronizes itself to the sample rate of the rest of the system.

Crosspoint Switch
The crosspoint switch replaces the data busses of more conventional architectures. It enables all the necessary data transfers for one instruction cycle to take place simultaneously, with no contention, at effective data rates up to 240M bits per second.

The crosspoint switch is double-buffered, so that it may be set up for the next instruction during the execution of the current instruction. The connection pattern determines the signal processing algorithm.

Program Sequencer
The program sequencer is built around an eight bit instruction counter and a three-bit byte counter. The byte counter addresses the eight bytes of one instruction. To avoid the need for a branch address field in the program counter, the branch address is loaded with the SETUP instruction into the label register. The program sequencer also contains a loop counter and loop control logic. The branch logic can perform unconditional branches and conditional branches depending on the state of the "Flag" pin.

Instruction Decoder
Instruction decoding is performed by two PLA's operating on the function code. One PLA generates the crosspoint switch configuration; the other controls the non-linear functions in the editing unit. The remainder of the instruction word is decoded locally by the small control sections associated with each data path component.

Pipelining
The FSP100 incorporates instruction-level pipelining to eliminate time lost in many processors fetching the next instruction from memory and storing the results of the previous instruction back into memory.

The *following Table 1* depicts this action. Time slot T3 is typical. The result of instruction N is stored in memory. Instruction N + 1 is executed within the FSP100 and the 64 bits of the instruction N + 2 are fetched from the external memory. During the time slot T4 the progress of each instruction advances. Instruction N + 1's results are stored back in memory. Instruction N + 2 is executed within the FSP100 and instruction N + 3 is fetched from external memory.

Pipelining continues in this fashion without conflict since the time to either fetch an instruction or store a result is always less than or equal to the time required by the FSP100 to execute an instruction.

Table 1 Pipelining

	TIME PERIODS					
	T1	T2	T3	T4	T5	T6
INST. N	FETCH	EXECUTE	STORE			
INST. N+1		FETCH	EXECUTE	STORE		
INST. N+2			FETCH	EXECUTE	STORE	
INST. N+3				FETCH	EXECUTE	STORE

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Signal Processing Functions

The following list presents the functions selectable by the FUNCTION code. Those functions that require more than one instruction cycle are implemented as two separate instructions. The software support package allows these multiple instruction sequences to be coded as a single instruction. The list does not include functions for testing, initialization and control, because the user does not usually code these functions directly.

Name	Number of Instructions	Function
Filter Poles:		
POLES	1	Direct form pole-pair
CPOLES	2	State-space pole-pair
APOLES	2	Adaptive pole-pair
RPOLE	1	Real pole with well-defined gain
RPOLES	2	Two independent real poles with well-defined gain
Filter Zeros:		
ZERO	1	Real zero with well-defined gain
ZEROS	1	Direct form zero pair
NOTCH	1	Adaptive notch
FIR	1	Two taps of an FIR
Combined Poles and Zeros:		
POLEP	1	Real pole with well-defined gain; zero at Z = +1
POLEN	1	Real pole with well-defined gain; zero at Z = −1
POLEZERO	1	Real pole and zero
BIQ	2	Direct form second order section
BIQR	2	Second order section for parallel forms
BIQU	2	Second order section with zeros in unit circle
BIQT	3	Transposed form second order section
BIQPP	1	Direct form second order section, zeros at Z = +1
BIQPN	1	Direct form second order section, zeros at Z = ±1
BIQNN	1	Direct form second order section, zeros at Z = −1
LADDR	2	Ladder form filter section
Miscellaneous Linear Functions:		
GAIN	1	Gain and offset
SUM	1	Weighted sum of two signals
INTEGS	1	Resettable integrator
Signal Generators:		
RAMP	1	Ramp/sawtooth generator
EXPVCO	1	Exponential ramp/VCO
SINEGEN	1	Sinewave oscillator
RANDY	1	Pseudo random noise
PULSE	1	Pulse generator
PULSERT	1	Retriggerable pulse generator

Name	Number of Instructions	Function
Point Non-Linearities:		
BREAKPT	1	Breakpoint (for piecewise linear functions)
SDGAIN	1	Sign dependent gain
SDOFF	1	Sign dependent offset
SDLEVEL	1	Sign dependent level
SDSRC	1	Sign dependent source
CCLIP	1	Center clipping
SUBIZ	1	Substitute zero inside window
SUBIT	1	Substitute data inside window
LIMIT	1	Limiting function (like saturation)
MAXVAL	1	Maximum of two signals
MINVAL	1	Minimum of two signals
RESTORE	1	Restore sign removed by absolute value
Non-Linearities with State:		
SAMPLE	1	Sample and hold
PEAKHOLD	1	Tracks and holds peaks
LEVELDET	1	Comparator with hysteresis
ZCROSS	1	Zero crossing detector
Housekeeping:		
GETMEM	1	Recover state variables
PUTMEM	1	Save value to memory
LOADB	1	Load B register
LOADC	1	Load C register
LOADBC	1	Load B and C register

Notes
Instruction names are preliminary.
"Well-defined" means that the gain coefficient is not restricted to a power of 2.

Table 2 Instruction Format

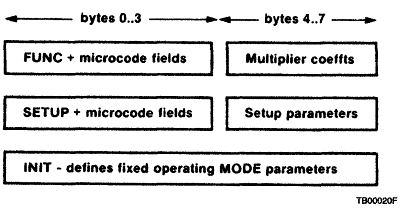


Table 2.1 Default Microcode Format – All Function Codes Except INIT

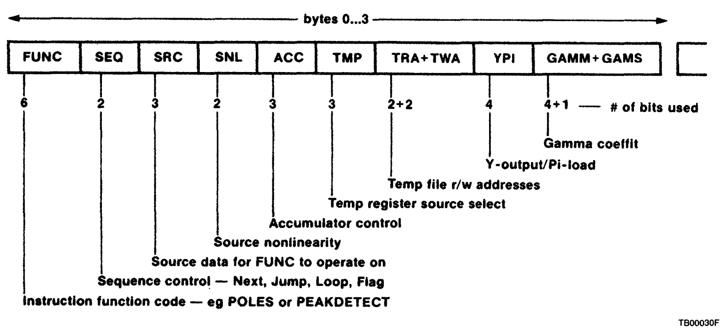


Table 2.2 Coefficient Format (all Function Codes Except INIT And SETUP)

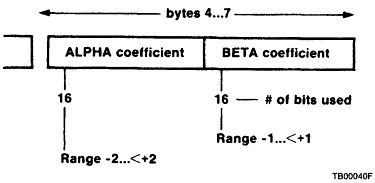


Table 2.3 SETUP Parameter Format (only Applies For SETUP Function Code)

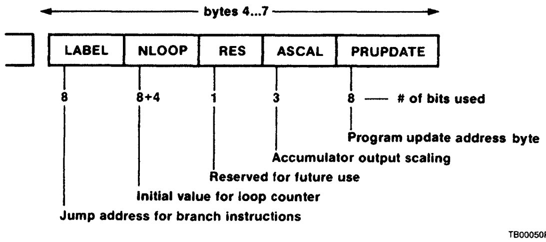
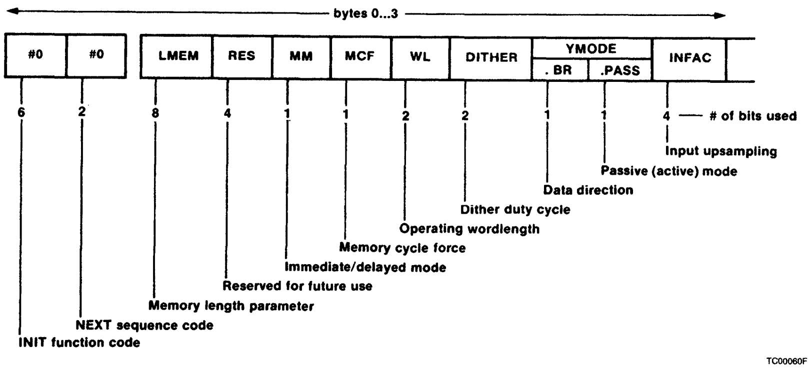
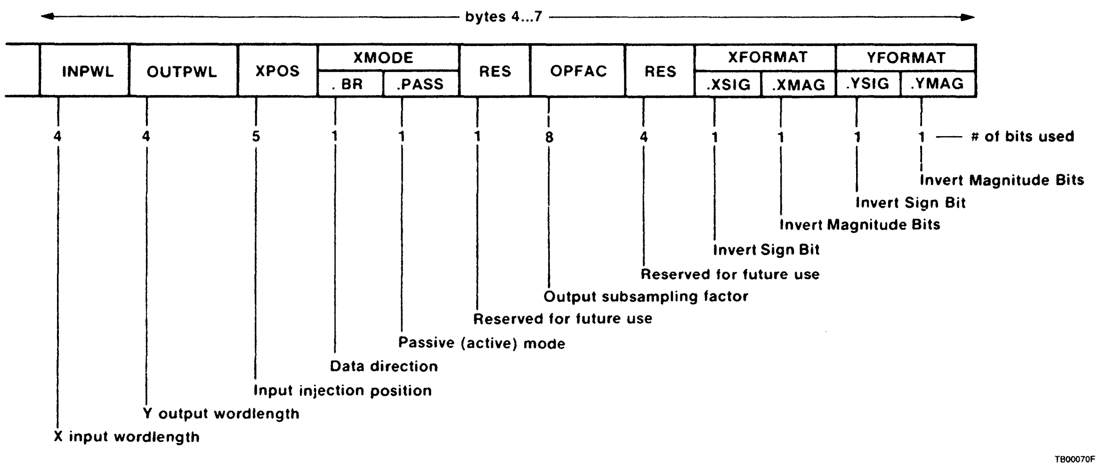


Table 2.4 Special INIT Instruction Format





Notes

The XFORMAT field operates on the incoming data stream AFTER it has entered the PDF and it has been subject to the XMODE data direction field. Thus, it regards the Most Significant bit of incoming data as the sign bit and the remaining bits as the magnitude bits.

The YFORMAT field operates on the outgoing data stream while it is still in the internal two's complement format. Thus, it regards the Most Significant bit of internal data as the sign bit and the remaining bits as the magnitude bits. The data is still subject to bit reversing as specified in the YMODE data direction field.

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Signal Descriptions

Name	I/O	H/L	Description
VCC	I		Power
GND	I		Power
INCK	I	H	Input clock
INDR	I	H	Input device ready
INRQ	O	H	Input request
INSD	I	H	Input serial data
OPCK	I	H	Output clock
OPDR	I	H	Output device ready
OPRQ	O	H	Output request
OPSD	O	H	Output serial data
RESET	I	L	Reset
HOLD	I	H	Force processor wait
IDLE	O	H	Indicates forced processor wait
CLK	I		Processor clock
OVER	O	H	Overflow
SIGN	O	H	Sign
NXT	O	H	External sequencer clock
FLAG	I	H	Flag (branch control)
PAO-7	O	H	Program word address (tri-state)
PBO-2	O	H	Program byte address (tri-state)
DO-7	I	H	Program byte input

Program Memory Operation

The FSP100 is designed to operate with an external program memory with no impact on the data throughput. To achieve this, a separate instruction bus is utilized with dedicated address and data lines. Internally, a 64-bit instruction word is used, but it is time-multiplexed into eight bytes.

The 11-bit program address bus can address a total of 256 instructions with the least significant three bits addressing both the eight bytes of the current instruction and the eight most significant bits of the program counter. This configuration means that, when using a byte-wide memory, no additional external interface logic is required.

Figure 2 illustrates the typical configuration of an FSP100 and its program memory, in this case a 1K x 8-bit PROM. A timing diagram follows.

Data Input/Output Operation

The FSP100 has a dedicated data input-output port that allows maximum utilization of the processor while requiring a minimum of external logic. To achieve this, dedicated input and output channels are available that can be asynchronous from the CPU and each other in a variety of configurations, according to external requirements. Further, to simplify multiprocessor systems, the ports are configured such that processors can be directly tied output to input with no additional logic.

The operation of the two ports is largely the same with the exception of the data pin itself. Both ports are serial, one bit wide, and come with a variety of options to independently configure each channel. These options are as follows:

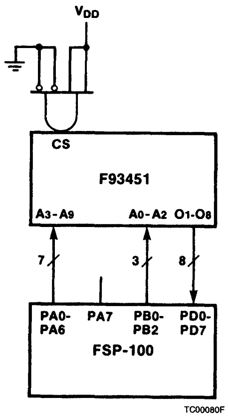
Clock Frequency: This determines the rate at which the bits are serially clocked into and out of the data pins. It is individually selectable for each channel and need not be synchronous with the CPU clock.

Data Word Length: The input-output ports can operate with any data word length from 8 up to 32 bits in increments of 2 bits. Further, this word length does not have to be the same as that used internally; the FSP100 automatically adjusts for the value selected.

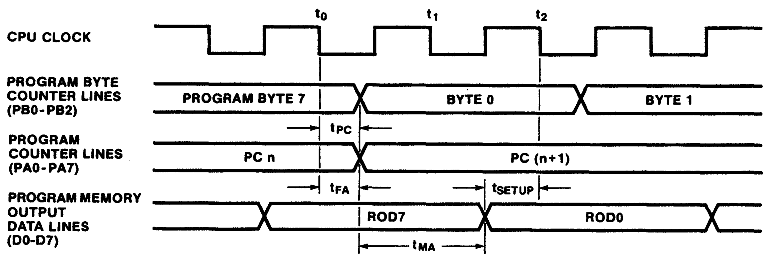
Data Format: This indicates the arithmetic format of the external serial data stream. The options for the incoming arithmetic format are two's complement, inverted two's complement, offset binary and inverted offset binary. The FSP100 will automatically convert between the format specified and its' own internal two's complement format.

Data Direction: This determines the direction in which the bits are passed into and out of the data pins. The data can be either least- or most- significant-bit first. The FSP100 automatically adjusts for this choice internally.

Figure 2 FSP100 With External Program Memory



Program Memory Timing Diagram (20-Bit Operation)



NOTE: t_{MA} = 65 ns @ 16 MHz (Typical)
t_{PC} = 25 ns Typical @ 30pF Loading

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Handshake Mode: This determines whether the FSP100 behaves as a master or slave during the input and output handshake operation. The two modes are called "ACTIVE" and "PASSIVE" mode. In active mode, the FSP100 determines when the transfer begins. In passive mode, the FSP100 waits until the device ready line goes high before beginning a transfer.

Figure 3 shows a typical data path configuration for a cascaded pair of FSP100s being driven by a standard A-D input and D-A output. Input and Output timing diagrams follow.

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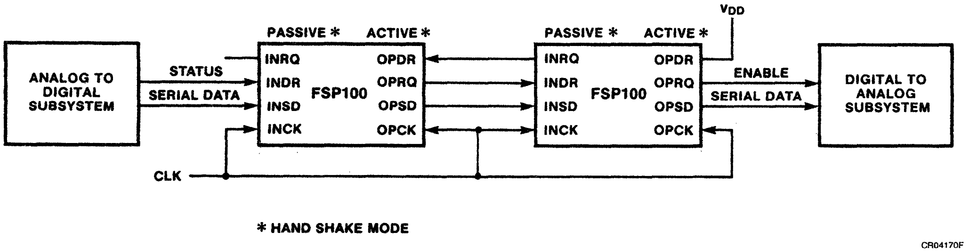
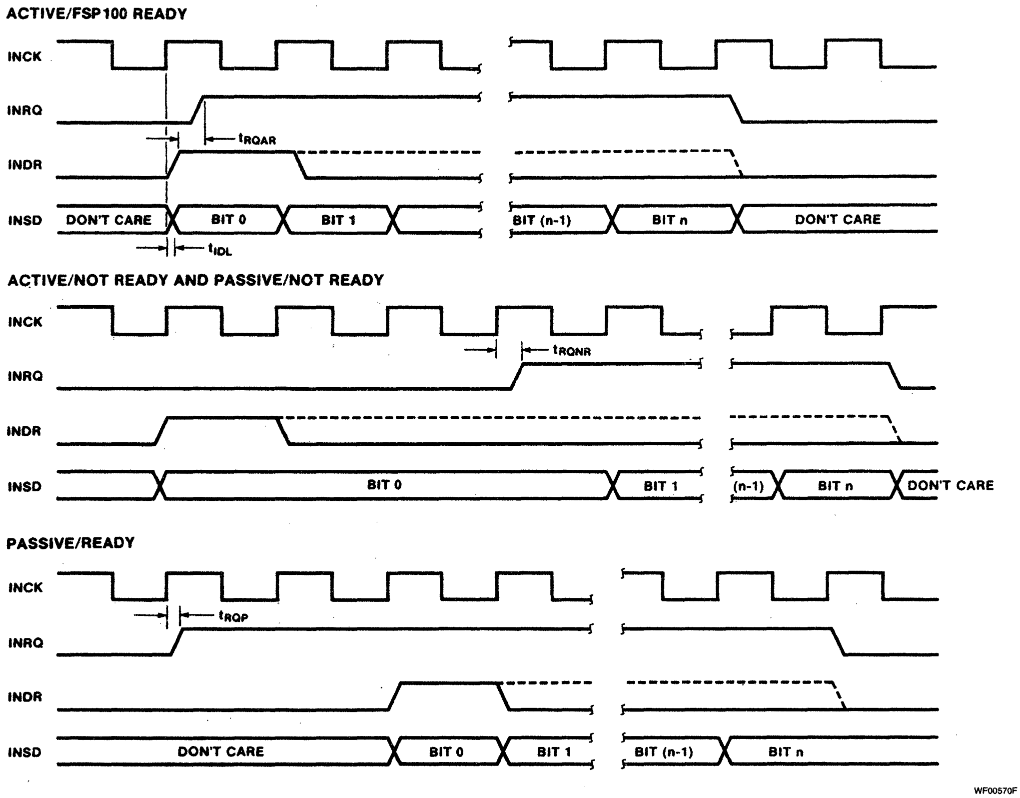
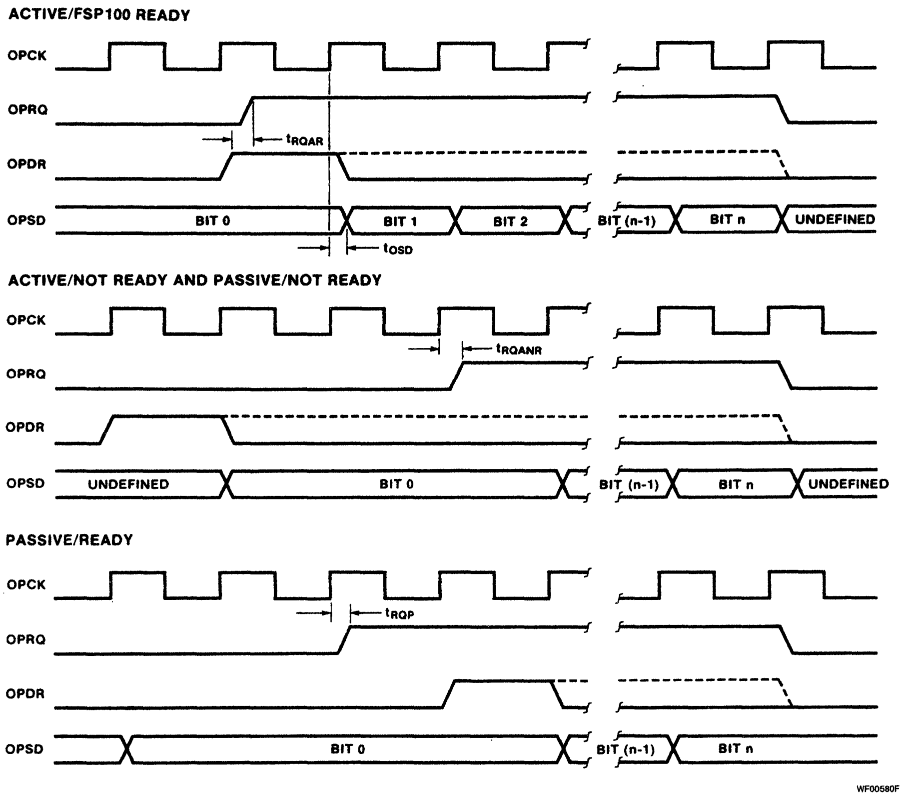
Figure 3 Dual Processor Configuration with Analog Input and Output



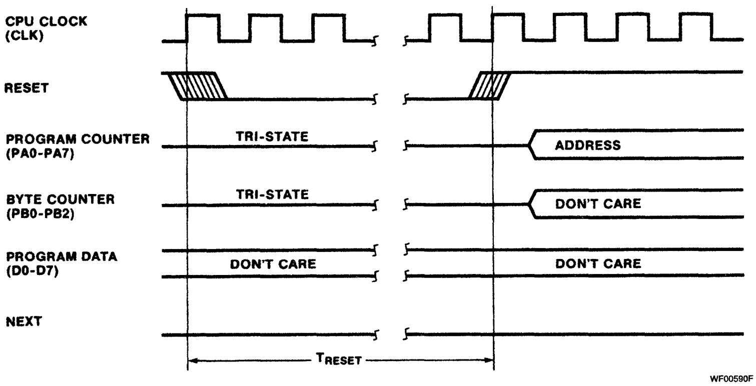
Data Input Timing/Handshake Timing ("n" Bit Data)



Data Output Timing ("n" Bit Data)



PFD Reset Operation



NOTE: T_{RESET} must be the greater time period of 25 CPU clock cycles of three (3) Input Data Clock cycles.

Absolute Maximum Ratings[1]

Symbol	Characteristic	Range	Unit
V_{DD}	Supply Voltage	−0.5 to +6.0	V
V_I	Input Voltage	−0.5 to V_{DD} +0.5	V
I_I	dc Input Current	±20	mA
T_{STG}	Storage Temperature Ceramic Package Plastic Package	 −65 to +150 −40 to +125	°C
T_A	Ambient Temperature Under Bias[2] Commercial/Industrial	 −40 to +70	°C
T_L	Lead Temperature (Soldering, 10 s)	300	°C

Electrical Characteristics V_{DD} = 5.0 V ±0.25 V, 0 to 70°C

Symbol	Characteristic	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage CMOS Input TTL Input	Guaranteed Input HIGH Voltage	3.5 2.0	V_{DD} V_{DD}	V
V_{IL}	Input LOW Voltage CMOS Input TTL Input	Guaranteed Input LOW Voltage	−0.5 −0.5	1.5 0.8	V V
V_{OH}	Output HIGH Voltage	70°C, V_{DD} = 4.5 V	V_{DD}	−0.05	V
V_{OL}	Output LOW Voltage	70°C, V_{DD} = 4.5 V		0.1	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or GND	−10	10	μA
I_{OZ}	Three-State Output Leakage Current	V_{OUT} = V_{DD} or GND	−10	10	μA
C_{IN}	Input Capacitance	Excluding Package		5.0	pF
C_{OUT}	Output Capacitance	Excluding Package		5.0	pF

Notes

1. Stresses greater than those listed under Absolute Maximum Ranges may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Junction temperature may not exceed ambient temperature by more than 20°C.

FAIRCHILD

A Schlumberger Company

F2224 • F2212 2400/1200/600/300 bps Full Duplex Modem

Advance Information, June 1986

Advanced Signal Processing Division

Description

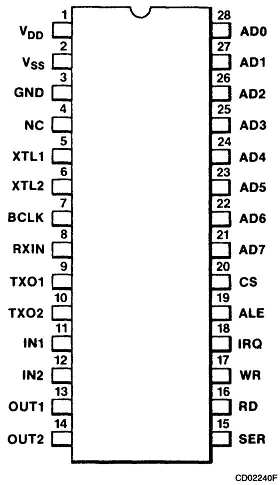
The F2224 and F2212 are single-chip full-duplex modem circuits, operating at 2400 (F2224 only), 1200, 600 and 0-300 bps. The F2224 is compatible with the CCITT V.22 bis modem specification, and both chips are compatible with V.22B, Bell 212A, Bell 103, V.21, V.23 and Bell 202. The ICs perform all signal processing functions, and feature both a parallel microprocessor interface with integral UART and an alternate four line serial control and separate data interface.

The F2212, under control of a host processor or dedicated microcontroller, provides a complete low-cost solution to data transmission at speeds up to 1200 bps and is pin for pin and functionally compatible with the F2224, which provides an upgrade path to 2400 bps operation, with minimal changes to existing firmware. Handshaking protocols are included on-chip, which will reduce control-processor firmware requirements.

An on-chip hybrid simplifies connection to the telephone network and uncommitted I/O lines are provided for DAA control and RS232 implementation if required. DTMF dialing and call progress tone detection are included.

- **V.22 bis (F2224 Only), V.22B, 212A, 103, V.21, V.23 And Bell 202 Compatible**
- **V.23 And 202 Modes Have Selectable 75 Or 150 bps Backward Channels**
- **Performs All Signal Processing Functions**
- **Parallel μP Interface With Integral UART**
- **Alternate Serial Control And Data Interface**
- **Register Control Of Modem And UART Operation**
- **DTMF Tone Generation And Call Progress Tone Detection For Smart Dialer Applications**
- **1300 Hz Calling Tone Generator On Chip**
- **On-Chip Hybrid And Programmable I/O For DAA Control And RS232 Implementation**
- **Very Few External Components Required**
- **Low Power Dissipation And A Very Low Power Standby Mode**
- **28-Lead Ceramic DIP, Plastic DIP And Surface Mount Packages**

Connection Diagram
28-Lead DIP
(Top View)



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Order Information

Device Code	Package Code	Package Description
F2224DC	FM	Ceramic DIP
F2224PC	*	Molded DIP
F2224QC	*	Molded Surface Mount
F2212DC	FM	Ceramic DIP
F2212PC	*	Molded DIP
F2212QC	*	Molded Surface Mount

FAIRCHILD

A Schlumberger Company

F30S54/F30S57 Monolithic Serial Interface CMOS CODEC/FILTER

Preliminary

Advanced Signal Processing Division

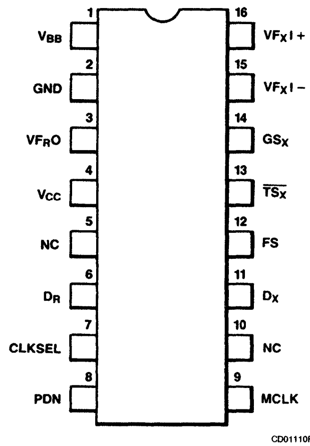
Description

The F30S54, F30S57 family consists of μ-law and A-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The F30S54, F30S57 operate in the synchronous mode only and are pin compatible with the F3054 and F3057 respectively. The devices are fabricated using Fairchild's advanced Double Poly Silicon-Gate CMOS process.

The transmit portion of each device consists of an input gain adjust amplifier, an active RC pre-filter, a switched-capacitor band-pass filter, and a compressing encoder with auto-zero circuitry. The active RC pre-filter eliminates very high frequency noise, and the switched-capacitor filter rejects signals below 200 Hz and above 3400 Hz. The compressing encoder samples the filtered signal and encodes it in the compressed μ-law and A-law PCM format. The receive portion of each device consists of an expanding decoder, which reconstructs the analog signal from the compressed μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require a 1.536 MHz, 1.544 MHz or 2.048 MHz master clock and an 8 kHz frame sync pulse. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

- **Pin Compatible with F3054, F3057**
- **Complete Codec and Filtering System Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter with Sin X/X Correction**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **μ-Law, 16 Pin — F30S54**
- **A-Law, 16 Pin — F30S57**
- **Meets or Exceeds all D3/D4 and CCITT Specifications**
- **±5 V Operation**
- **Low Operating Power — Typically 40 mW**
- **Power-Down Standby Mode — Typically 1.7 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**

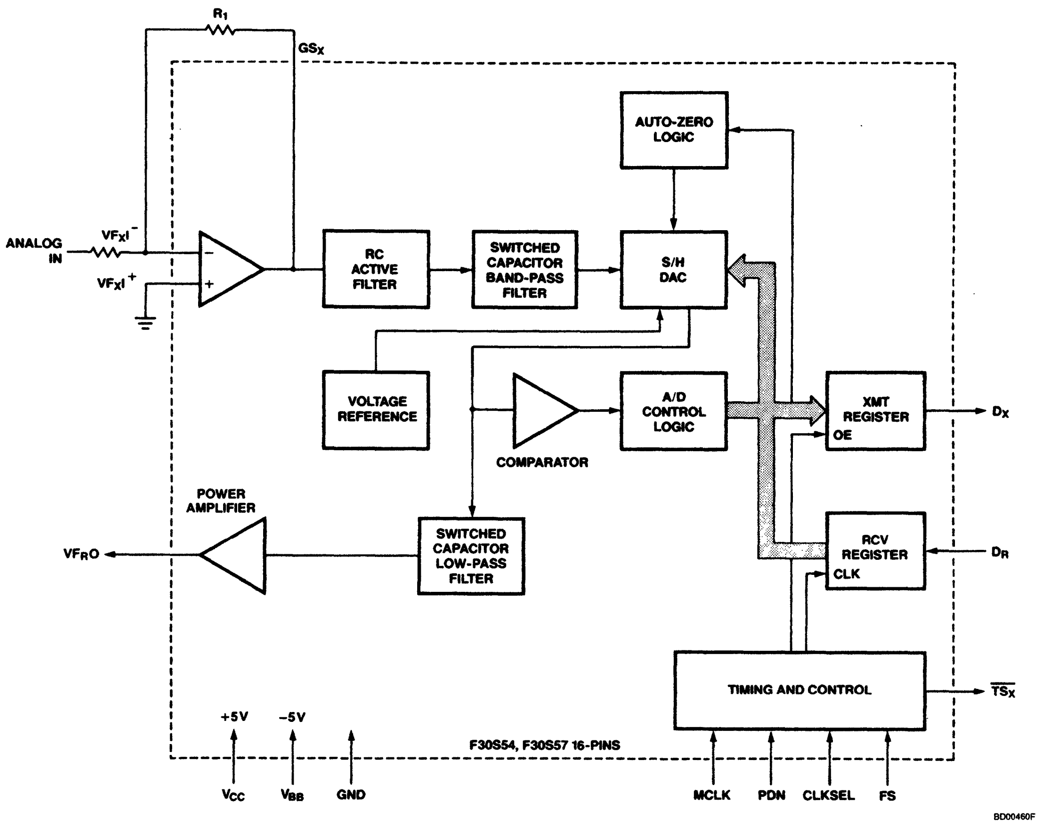
Connection Diagram (Top View)



Order Information

Device Code	Package Code	Package Description
F30S54DC	FW	Ceramic DIP
F30S57DC	FW	Ceramic DIP

Figure 1 Block Diagram



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Pin Description

Pin No.	Name	Function
1	V_{BB}	Negative power supply pin. $V_{BB} = -5.0\ V \pm 5\%$.
2	GND	Ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply pin. $V_{CC} = +5.0\ V \pm 5\%$.
5	N.C.	No internal connection.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS leading edge.
7	CLKSEL	Logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock. MCLK is used for both transmit and receive directions *(see Table 1).*
8	PDN	Power Down. The device is powered up when PDN is held low.
9	MCLK	Master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz.
10	N.C.	No internal connection.
11	D_X	The 3-state PCM data output which is enabled by FS.
12	FS	Frame sync pulse input which enables MCLK to shift out the PCM data on D_X. FS is an 8 kHz pulse train; *see Figures 2 and 3* for timing details.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

Power-Up

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level must be applied to the PDN pin and FS pulses must be present. Thus, two power-down control modes are available. The first is to pull the PDN pin high; the second is to hold the FS input continuously low — the device will power-down approximately 2 ms after the last FS pulse. Power-up will occur on the first FS pulse. The 3-state PCM data output, D_X, will remain in the high impedance state until the second FS pulse.

Synchronous Operation

Synchronous operation requires only one masterclock for both the transmit and receive directions. *Table 1 indicates* the frequencies which can be selected, depending on the state of CLKSEL. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Table 1 Selection of Master Clock Frequencies

CLKSEL	Master Clock Frequency Selected: F30S57	Master Clock Frequency Selected: F30S54
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Functional Description (Cont.)

Short Frame Sync Operation

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulse, FS, must be one MCLK period long, with timing relationships *specified in Figure 2.* With FS high during a falling edge of MCLK, the next rising edge of MCLK enables the D_X 3-state output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. The corresponding eight falling edges of the same clock pulses will clock in the receive data.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulse, FS, must be three or more MCLK periods long, with timing relationships *specified in Figure 3.* Based on the sync, FS, the device will sense whether short or long frame sync pulses are being used. The D_X 3-state output buffer is enabled with the rising edge of FS or the rising edge of MCLK, whichever comes later, and the first bit clocked out is the sign bit. The following seven MCLK rising edges clock out the remaining seven bits. The D_X output is disabled by the eighth falling edge of MCLK, or by FS going low, whichever comes later. Provided the frame sync FS is greater than three MCLK periods, the D_X output will be enabled for eight MCLK periods, independent of the actual length of the FS pulse.

Transmit Section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, *see Figure 1.* The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of an RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 128 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of compressing type according to μ-law (F30S54) or A-law (F30S57) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload level (t_{MAX}) of nominally 2.5 V peak (see table of Transmission Characteristics). The FS frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins after the decode cycle. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which total 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

Receive Section

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 128 kHz. The decoder is A-law (F30S57) or μ-law (F30S54) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity gain. Upon the occurrence of FS the data at the D_R input is clocked in on the falling edge of the next eight MCLK periods. At the end of the time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is approximately 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs).

Absolute Maximum Ratings

V_{CC} to GND	7.0 V
V_{BB} to GND	−7.0 V
Voltage at any Analog Input or Output	V_{CC} + 0.3 V to V_{BB} − 0.3 V
Voltage at any Digital Input or Output	V_{CC} + 0.3 V to GND − 0.3 V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Unless otherwise noted: V_{CC} = 5.0 V ± 5%, V_{BB} − 5.0 V ± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Operating Current						
$I_{CC}0$	Power-Down Current			0.3	1.5	mA
$I_{BB}0$	Power-Down Current			0.03	0.3	mA
$I_{CC}1$	Active Current			4.0	7.0	mA
$I_{BB}1$	Active Current			4.0	7.0	mA
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			0.4 0.4	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	2.4			V
I_{IL}	Input Low Current	GND ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State	D_X, GND ≤ V_O ≤ V_{CC}	−10		10	μA
Analog Interface With Transmit Amplifier Input						
I_IXA	Input Leakage Current	−2.5 V ≤ V ≤ +2.5 V, VF_XI+ or VF_XI−	−200		200	nA
R_IXA	Input Resistance	−2.5 V ≤ V ≤ +2.5 V, VF_XI+ or VF_XI−	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unit Gain		1.0	3.0	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L ≥ 10 kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1.0	2.0		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
Analog Interface With Receive Amplifier Output						
R_ORF	Output Resistance	Pin VF_RO		1.0	3.0	Ω
R_LRF	Load Resistance	VF_RO = ±2.5 V	600			Ω

Electrical Characteristics (Cont.) Unless otherwise noted: V_{CC} = 5.0 V ± 5%, V_{BB} − 5.0 V ± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
C_LRF	Load Capacitance	VF_RO to GND			25	pF
VOS_RO	Output DC Offset Voltage	VF_RO to GND	−200		200	mV
Timing Specifications						
$1/t_{PM}$	Frequency of Master Clock	Depends on the CLKSEL Pin		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High		160			ns
t_{WML}	Width of Master Clock Low		160			ns
t_{RM}	Rise Time of Master Clock				50	ns
t_{FM}	Fall Time of Master Clock				50	ns
t_{HMF}	Holding Time from Master Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Master Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFM}	Set-Up Time from Frame Sync to Master Clock Low	Long Frame Only	80			ns
t_{DMD}	Delay Time from MCLK High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS}_X$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from MCLK Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS or MCLK, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDM}	Set-Up Time from D_R Valid to MCLK Low		50			ns
t_{HMD}	Hold Time from MCLK Low to D_R Invalid		50			ns
t_{SF}	Set-Up time from FS to MCLK Low	Short Frame Sync Pulse (1 or 2 Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from MCLK Low to FS	Short Frame Sync Pulse (1 or 2 Clock Periods Long) (Note 1)	100			ns
t_{HMFI}	Hold Time from 3rd Period of Master Clock Low to Frame Sync FS	Long Frame Sync Pulse (from 3 to 8 Clock Periods Long)	100			ns

Note

For short frame sync timing, FS must go high while the Master Clock is high.

Transmission Characteristics Unless otherwise specified: $T_A = 0°C$ to 70°C, $V_{CC} = 5.0$ V ±5%, $V_{BB} = -5.0$ V ±5%, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Amplitude Response						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600 Ω) 0 dBm0 F30S54 F30S57		 1.2276 1.2276		Vrms
t_{MAX}	Max Overload Level	F30S54 (3.17 dBm0) F30S57 (3.14 dBm0)		2.501 2.492		V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5$ V, $V_{BB} = -5$ V Input at $GS_X = 0$ dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz - 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to 70°C			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5$ V ±5%, $V_{BB} = -5$ V ±5%			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_XI+ = −40 dBm0 to +3 dBm0 VF_XI+ = −50 dBm0 to −40 dBm0 VF_XI+ = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5$ V, $V_{BB} = -5$ V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to 70°C			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5$ V ±5%, $V_{BB} = -5$ V ±5%			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded−10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Output Drive Level	$R_L = 600$ Ω	−2.5		2.5	V

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0$ V ±5%, $V_{BB} = -5.0$ V ±5%, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Envelope Delay Distortion With Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	µs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz – 600 Hz f = 600 Hz – 800 Hz f = 800 Hz – 1000 Hz f = 1000 Hz – 1600 Hz f = 1600 Hz – 2600 Hz f = 2600 Hz – 2800 Hz f = 2800 Hz – 3000 Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	µs µs µs µs µs µs µs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	µs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz – 1000 Hz f = 1000 Hz – 1600 Hz f = 1600 Hz – 2600 Hz f = 2600 Hz – 2800 Hz f = 2800 Hz – 3000 Hz	–40 –30	–25 –20 70 100 145	 90 125 175	µs µs µs µs µs
Noise						
N_{XC}	Transmit Noise, C Message Weighted	F30S54 $VF_XI^+ = 0$ V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	F30S57 $VF_XI^+ = 0$ V		–74	–69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	F30S54 PCM Code Equals Alternating Positive and Negative Zero		8.0	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	F30S57 PCM Code Equals Positive Zero		–82	–79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms			–53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI+ = 0$ Vrms, $V_{CC} = 5.0$ V_{DC} + 100 mVrms f = 0 kHz – 50 kHz	 40			 dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI+ = 0$ Vrms, $V_{BB} = -5.0$ V_{DC} + 100 mVrms f = 0 kHz – 50 kHz	 40			 dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0$ V_{DC} + 100 mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0$ V_{DC} + 100 mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0$ V ±5%, $V_{BB} = -5.0$ V ±5%, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz – 3400 Hz Input Applied to VF_XI+, Measure Individual Image Signals at VF_RO				
		4600 Hz – 7600 Hz			−32	dB
		7600 Hz – 8400 Hz			−40	dB
		8400 Hz – 100,000 Hz			−32	dB
Distortion						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method				
		Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz			−41	dB
Crosstalk						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz – 3400 Hz D_R = Steady PCM Code		−90	−75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz – 3400 Hz, VF_XI = 0 V		−90	−70 (Note 2)	dB

Notes
1. Measured by extrapolation from the distortion test result.
2. CT_{R-X} is measured with a −40 dBm0 activating signal applied at VF_XI+.

Encoding Format At D_X

	F30S54 μ-Law	F30S57 A-Law (Includes Even Bit Inversion)
V_{IN} (at GS_X) = + Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0 V	{1 1 1 1 1 1 1 1 {0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = − Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

Figure 2 Timing Diagrams Short Frame Sync Timing

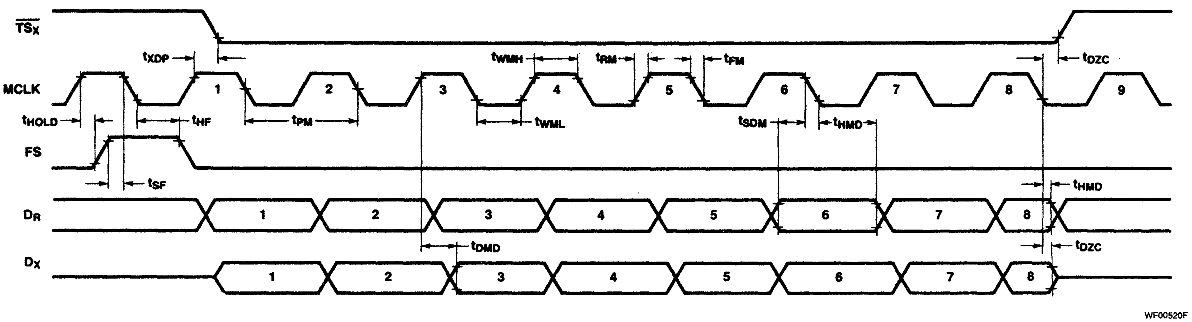
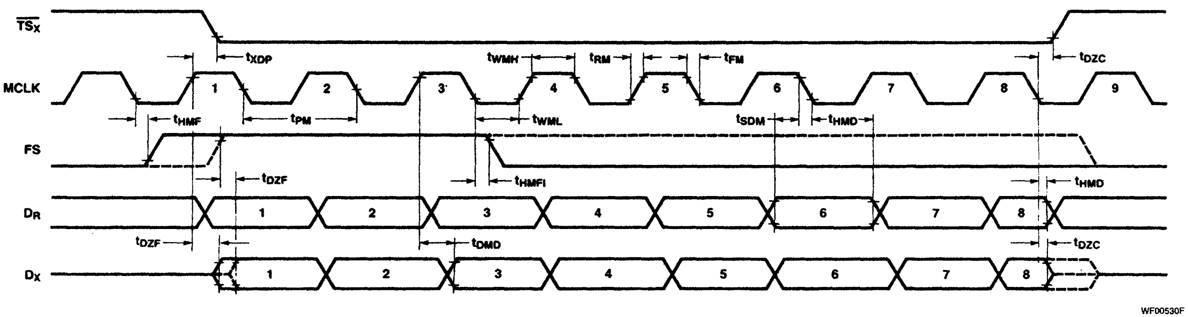


Figure 3 Long Frame Sync Timing



Applications Information

Power Supplies

While the pins of the F30S54 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

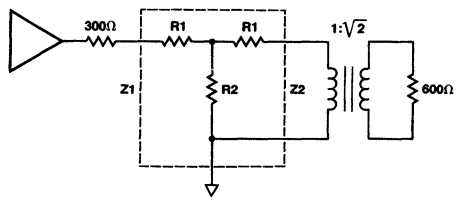
All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Receive Gain Adjustment

For applications where a F30S54 family CODEC/FILTER receive output must drive a 600 Ω load, but a peak swing lower than ±2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1, Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1, Z2}\left(\frac{N}{N^2-1}\right)$$

Where $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

$$S = \sqrt{\frac{Z1}{Z2}}$$

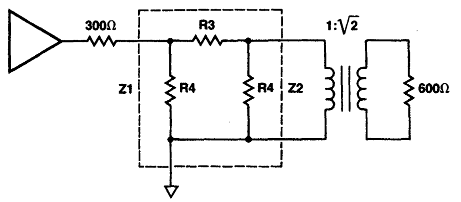
Also: $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

CD01150F

π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1, Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

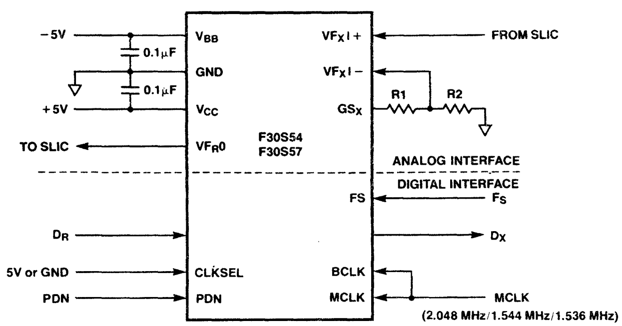
CD01160F

Applications Information (Cont.)

Table II. Attentuator Tables for Z1 = Z2 = 300 Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	6.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2.0	34.4	1.3k	70	2.6k
3.0	51.3	850	107	1.8k
4.0	68	650	144	1.3k
5.0	84	494	183	1.1k
6.0	100	402	224	900
7.0	115	380	269	785
8.0	179	284	317	698
9.0	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 4 Typical Synchronous Application



Note 1: XMIT gain = $20 \times \log\left(\frac{R1+R2}{R2}\right)$; $(R1 + R2) > 10K\Omega$

AD00020F

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FAIRCHILD

A Schlumberger Company

F30S64/F30S67 Monolithic Serial Interface CMOS CODEC/FILTER

Preliminary

Advanced Signal Processing Division

Description

The F30S64, F30S67 family consists of μ-law and A-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture *shown in Figure 1*, and a serial PCM interface. The F30S64, F30S67 operate in the synchronous mode only and are pin compatible with the TP3064 and TP3067 respectively. Similar to the F30S54 and F30S57, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6 V across a balanced 600 Ω load. Also included is an analog loopback switch and $\overline{TS_X}$ output. The devices are fabricated using Fairchild's advanced Double Poly Silicon-Gate CMOS process.

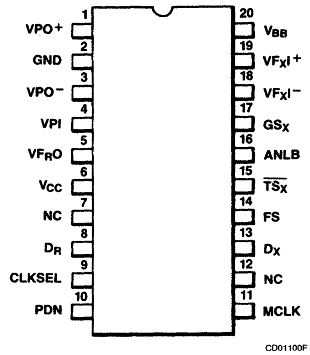
The transmit portion of each device consists of an input gain adjust amplifier, an active RC pre-filter, a switched-capacitor band-pass filter, and a compressing encoder with auto-zero circuitry. The active RC pre-filter eliminates very high frequency noise, and the switched-capacitor filter rejects signals below 200 Hz and above 3400 Hz. The compressing encoder samples the filtered signal and encodes it in the compressed μ-law or A-law PCM format.

The receive portion of each device consists of an expanding decoder, a switched-capacitor low-pass filter, and two power amplifiers. The decoder reconstructs the analog signal from the compressed μ-law or A-law code, and the low-pass filter corrects for the sin x/x response of the decoder output. The two power amplifiers are in a bridged configuration and are capable of driving low impedance loads.

The devices require a 1.536 MHz, 1.544 MHz or 2.048 MHz master clock and an 8 kHz frame sync pulse. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

- **Pin Compatible with TP3064, TP3067**
- **Complete Codec and Filtering System Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter with Sin X/X Correction**
  - **Receive Push-Pull Power Amplifier**
  - **Analog Loopback**
  - **Active RC Noise Filters**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **μ-Law, 20 Pin - F30S64**
- **A-Law, 20 Pin - F30S67**
- **Meets or Exceeds all D3/D4 and CCITT Specifications**
- **±5 V Operation**

Connection Diagram (Top View)

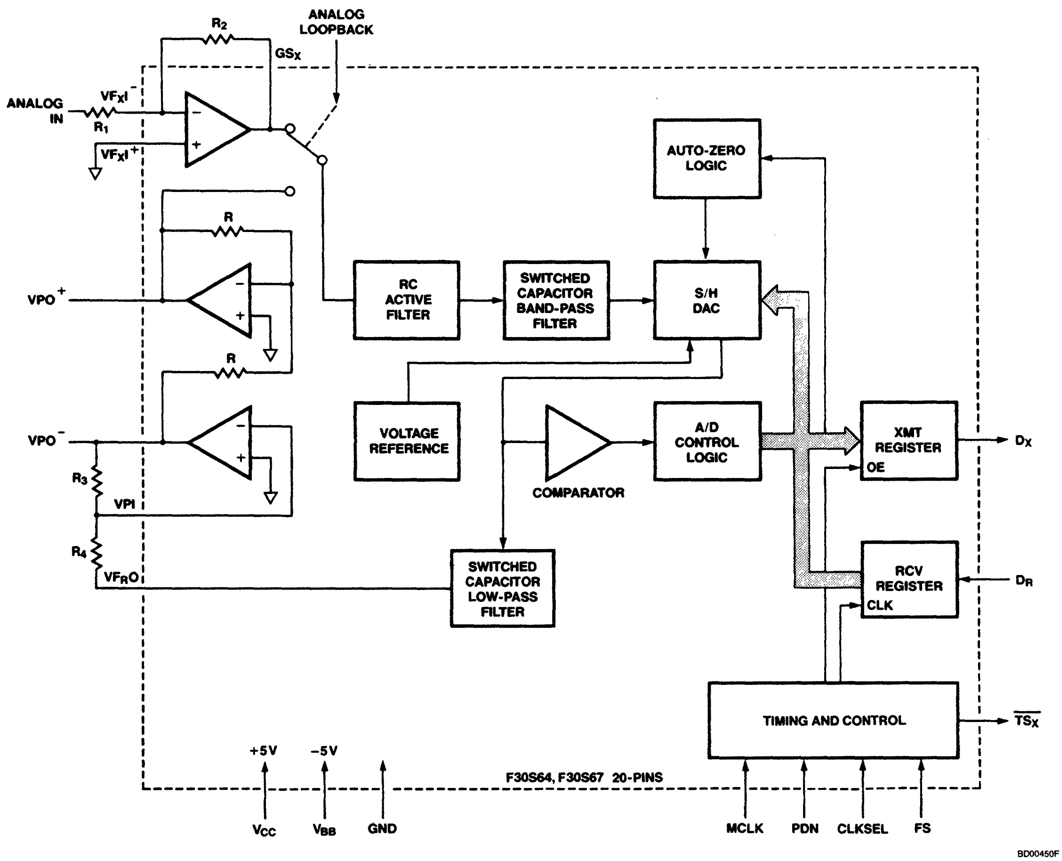


Order Information

Device Code	Package Code	Package Description
F30S64DC	FL	Ceramic DIP
F30S67DC	FL	Ceramic DIP

- **Low Operating Power — Typically 45 mW**
- **Power-Down Standby Mode — Typically 1.7 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**

Figure 1 Block Diagram



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Pin Description

Pin No.	Name	Function
1	VPO +	The non-inverted output of the receive power amplifier.
2	GND	Ground. All signals are referenced to this pin.
3	VPO –	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin. $V_{CC} = +5\ V \pm 5\%$.
7	N.C.	No internal connection.
8	D_R	Receive data input. PCM data is shifted into D_R following the FS leading edge.
9	CLKSEL	Logic input which selects either 1.536 MHz, 1.544 MHz or 2.048 MHz for master clock. MCLK is used for both transmit and receive directions (*See Table 1*).
10	PDN	Power down. The device is powered up when PDN is held low.
11	MCLK	Master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz.
12	N.C.	No internal connection.
13	D_X	The 3-state PCM data output which is enabled by FS.
14	FS	Frame sync pulse input which enables MCLK to shift out the PCM data on D_X and shift in data on D_R. FS is an 8 kHz pulse train, *see Figures* 2 *and* 3 for timing details.
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO + output of the receive power amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
18	VF_XI –	Inverting input of the transmit input amplifier.
19	VF_XI +	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin. $V_{BB} = -5\ V + 5\%$.

Functional Description

Power-Up

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level must be applied to the PDN pin and FS pulses must be present. Thus, two power-down control modes are available. The first is to pull the PDN pin high; the second is to hold the FS input continuously low — the device will power-down approximately 2 ms after the last FS pulse. Power-up will occur on the first FS pulse. The 3-state PCM data output, D_X, will remain in the high impedance state until the second FS pulse.

Synchronous Operation

Synchronous operation requires only one master clock for both the transmit and receive directions. *Table 1 indicates* the frequencies which can be selected, depending on the state of CLKSEL. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Table 1. Selection of Master Clock Frequencies

	Master Clock Frequency Selected	
CLKSEL	F30S67	F30S64
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Functional Description (Cont.)

Short Frame Sync Operation

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulse, FS, must be one MCLK period long, with timing relationships *specified in Figure 2*. With FS high during a falling edge of MCLK, the next rising edge of MCLK enables the D_X 3-state output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. The corresponding eight falling edges of the same clock pulses will clock in the receive data.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulse, FS, must be three or more MCLK periods long, with timing relationships *specified in Figure 3*. Based on the sync, FS, the device will sense whether short or long frame sync pulses are being used. The D_X 3-state output buffer is enabled with the rising edge of FS or the rising edge of MCLK, whichever comes later, and the first bit clocked out is the sign bit. The following seven MCLK rising edges clock out the remaining seven bits. The D_X output is disabled by the eighth falling edge of MCLK, or by FS going low, whichever comes later. Provided the frame sync FS is greater than three MCLK periods, the D_X output will be enabled for eight MCLK periods, independent of the actual length of the FS pulse.

Transmit Section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, *see Figure 1*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of an RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 128 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of compressing type according to μ-law (F30S64) of A-law (F30S67) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload level (t_{MAX}) of nominally 2.5 V peak (*see table of Transmission Characteristics*). The FS frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins after the decode cycle. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

Receive Section

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 128 kHz. The decoder is A-law (F30S67) or μ-law (F30S64) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS the data at the D_R input is clocked in on the falling edge of the next eight MCLK periods. At the end of the time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Receive Power Amplifiers

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5 V peak output signal from the receive filter up to ±3.3 V peak into an unbalanced 300 Ω load, or ±4.0 V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600 Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ration, as *shown in Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 8 mW of power.

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Absolute Maximum Ratings

V_{CC} to GND	7.0 V
V_{BB} to GND	-7.0 V
Voltage at any Analog Input or Output	V_{CC} + 0.3 V to V_{BB} − 0.3 V
Voltage at any Digital Input or Output	V_{CC} + 0.3 V to GND − 0.3 V
Operating Temperature Range	-25°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Unless otherwise noted: V_{CC} = 5.0 V± 5%, V_{BB} − 5.0 V± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Operating Current						
$I_{CC}0$	Power-Down Current			0.3	1.5	mA
$I_{BB}0$	Power-Down Current			0.03	0.3	mA
$I_{CC}1$	Active Current	Power Amplifier Active, VPI = 0 V		4.3	7.0	mA
$I_{BB}1$	Active Current	Power Amplifier Active, VPI = 0 V		4.3	7.0	mA
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS}_X$, I_L = 3.2 mA,Open Drain			0.4 0.4	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	2.4			V
I_{IL}	Input Low Current	GND $\leqslant V_{IN} \leqslant V_{IL}$, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	$V_{IH} \leqslant V_{IN} \leqslant V_{CC}$	−10		10	μA
I_{OZ}	Output Current in High Impedance State	D_X, GND $\leqslant V_O \leqslant V_{CC}$	−10		10	μA
Analog Interface With Transmit Input Amplifier						
I_IXA	Input Leakage Current	−2.5 V $\leqslant$ V $\leqslant$ +2.5 V, VF_XI+ or VF_XI-	-200		200	nA
R_IXA	Input Resistance	−2.5 V $\leqslant$ V $\leqslant$ +2.5 V, VF_XI+ or VF_XI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1.0	3.0	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \geqslant$ 10 kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1.0	2.0		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$X_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB

Electrical Characteristics (Cont.) Unless otherwise noted: V_{CC} = 5.0 V± 5%, V_{BB} – 5.0 V± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = –5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
PSRRXA	Power Supply Rejection Ratio		60			dB
Analog Interface With Receive Amplifier Output						
R_ORF	Output Resistance	Pin VF_RO		1.0	3.0	Ω
R_LRF	Load Resistance	VF_RO = ± 2.5 V	10			kΩ
C_LRF	Load Capacitance	VF_RO to GND			500	pF
VOS_RO	Output DC Offset Voltage	VF_RO to GND	–200		200	mV
Analog Interface With Power Amplifiers						
IPI	Input Leakage Current	–1.0 V ≤ VPI ≤ 1.0 V	–100		100	nA
RIPI	Input Resistance	–1.0 V ≤ VPI ≤ 1.0 V	10			MΩ
VIOS	Input Offset Voltage		–25		25	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1.0		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance	R_L ≥ 1500 Ω R_L = 600 Ω R_L = 300 Ω VPO + or VPO– to GND			100 500 1000	pF pF pF
GA_P+	Gain, VPO^- to VPO^+	R_L = 300 Ω VPO^+ to GND Level at VPO^- = 1.77 Vrms (+3 dBm0)		–1.0		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO – Connected to VPI 0 kHz – 4 kHz 0 kHz – 50 kHz	 60 36			 dB dB
Timing Specifications						
$1/t_{PM}$	Frequency of Master Clock	Depends on the CLKSEL Pin		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High		160			ns
t_{WML}	Width of Master Clock Low		160			ns
t_{RM}	Rise Time of Master Clock				50	ns
t_{FM}	Fall Time of Master Clock				50	ns
t_{HMF}	Holding Time from Master Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Master Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFM}	Set-Up Time from Frame Sync to Master Clock Low	Long Frame Only	80			ns

Electrical Characteristics (Cont.) Unless otherwise noted: V_{CC} = 5.0 V± 5%, V_{BB} – 5.0 V± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = –5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
t_{DMD}	Delay Time from MCLK High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from MCLK Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS or MCLK, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDM}	Set-Up Time from D_R Valid to MCLK Low		50			ns
t_{HMD}	Hold Time from MCLK Low to D_R Invalid		50			ns
t_{SF}	Set-Up time from FS to MCLK Low	Short Frame Sync Pulse (1 or 2 Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from MCLK Low to FS	Short Frame Sync Pulse (1 or 2 Clock Periods Long) (Note 1)	100			ns
t_{HMFI}	Hold Time from 3rd Period of Master Clock Low to Frame Sync FS	Long Frame Sync Pulse (from 3 to 8 Clock Periods Long)	100			ns

Note

For short frame sync timing, FS must go high while the Master Clock is high.

Figure 2 Timing Diagram Short Frame Sync Timing

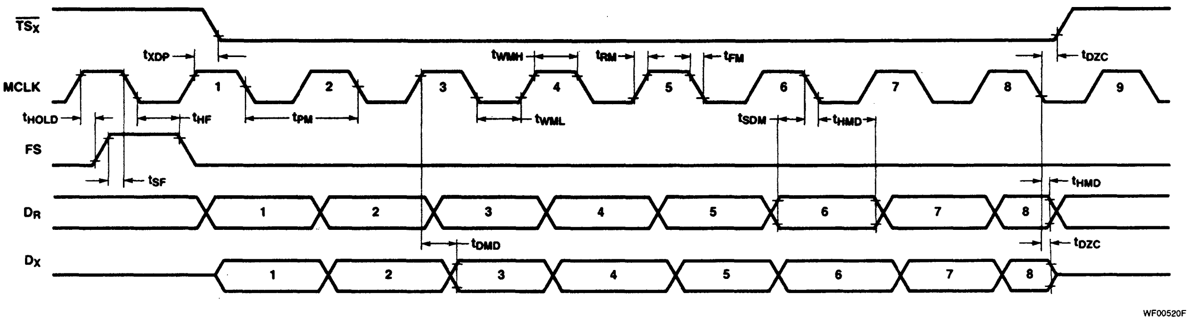
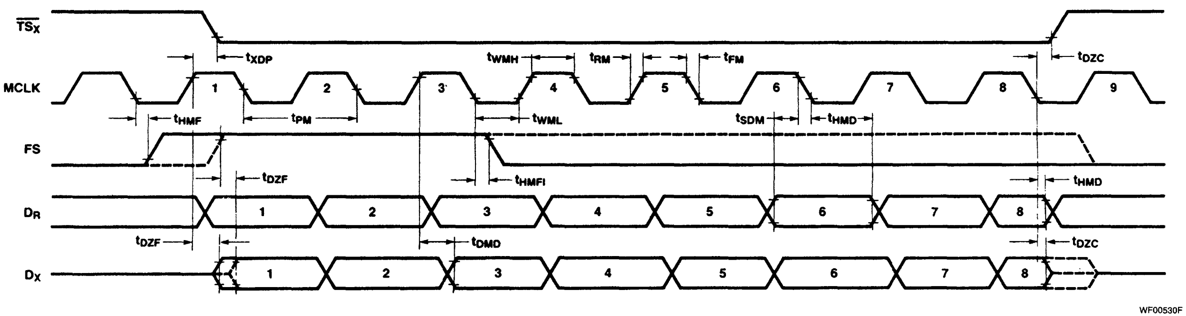


Figure 3 Timing Diagram Long Frame Sync Timing



Transmission Characteristics Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0$ V ± 5%, $V_{BB} = -5.0$ V ± 5%, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Amplitude Response						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600 Ω) 0 dBm0 F30S64 F30S67		 1.2276 1.2276		 Vrms Vrms
t_{MAX}		Max Overload Level F30S64 (3.17 dBm0) F30S67 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5$ V, $V_{BB} = -5$ V Input at $GS_X = 0$ dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz − 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5$ V ± 5%, $V_{BB} = -5$ V ± 5%			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_XI+ = −40 dBm0 to +3 dBm0 VF_XI+ = −50 dBm0 to −40 dBm0 VF_XI+ = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5$ V, $V_{BB} = -5$ V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $70°C$			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5$ V ± 5%, $V_{BB} = -5$ V ± 5%			±0.05	dB

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0\ V \pm 5\%$, $V_{BB} = -5.0\ V \pm 5\%$, GND = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded −10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0	−0.2		0.2	dB
		PCM Level = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		PCM Level = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
V_{RO}	Receive Filter Output at VF_RO	R_L = 10 kΩ	−2.5		2.5	V
Envelope Delay Distortion With Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz		195	220	μs
		f = 600 Hz − 800 Hz		120	145	μs
		f = 800 Hz − 1000 Hz		50	75	μs
		f = 1000 Hz − 1600 Hz		20	40	μs
		f = 1600 Hz − 2600 Hz		55	75	μs
		f = 2600 Hz − 2800 Hz		80	105	μs
		f = 2800 Hz − 3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1000 Hz	−40	−25		μs
		f = 1000 Hz − 1600 Hz	−30	−20		μs
		f = 1600 Hz − 2600 Hz		70	90	μs
		f = 2600 Hz − 2800 Hz		100	125	μs
		f = 2800 Hz − 3000 Hz		145	175	μs
Noise						
N_{XC}	Transmit Noise, C Message Weighted	F30S64 VF_XI^+ = 0 V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	F30S67 VF_XI^+ = 0 V		−74	−69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	F30S64 PCM Code Equals Alternating Positive and Negative Zero		8.0	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	F30S67 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI+ = 0 Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI+ = 0 Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 kHz − 50 kHz	40			dBC

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Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0\ V \pm 5\%$, $V_{BB} = -5.0\ V \pm 5\%$, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz – 3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100,000 Hz			 -32 –40 –32	 dB dB dB
Distortion						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to –30 dBm0 = –40 dBm0 XMT RCV = –55 dBm0 XMT RCV	 33 36 29 30 14 15			 dBC dBC dBC dBC dBC dBC
SFD_X	Single Frequency Distortion, Transmit				–46	dB
SFD_R	Single Frequency Distortion, Receive				–46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_XI+ = -4$ dBm0 to –21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz			–41	dB
Crosstalk						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz – 3400 Hz D_R = Steady PCM Code		-90	–75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz – 3400 Hz, $VF_XI = 0$ V		-90	–70 (Note 2)	dB

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to 70°C, $V_{CC} = 5.0$ V ± 5%, $V_{BB} = -5.0$ V ± 5%, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Power Amplifiers						
V_{OL}	Maximum 0 dBm0 Level for Better than ±0.1 dB Linearity Over the Range −10 dBm0 to +3 dBm0	Balanced Load, R_L Connected Between VPO^+ and VPO^-				
		$R_L = 600\ \Omega$	3.3			Vrms
		$R_L = 1200\ \Omega$	3.5			Vrms
		$R_L = 30\ k\Omega$	4.0			Vrms
S/D_P	Signal/Distortion	$R_L = 600\ \Omega$, 0 dBm0	50			dB

Notes
1. Measured by extrapolation from the distortion test result.
2. $CT_{R\text{-}X}$ is measured with a −40 dBm0 activating signal applied at VF_XI^+.

Encoding Format At D_X

	F30S64 µ-Law	F30S67 A-Law (Includes Even Bit Inversion)
V_{IN} (at GS_X) = + Full-Scale	1 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0
V_{IN} (at GS_X) = 0 V	{ 1 1 1 1 1 1 1 1 { 0 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V_{IN} (at GS_X) = − Full-Scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

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Applications Information

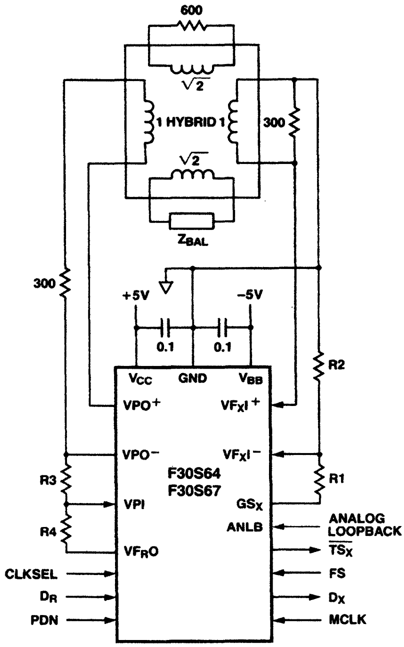
Power Supplies

While the pins of the F30S60 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.

Figure 4 Typical Synchronous Application



Note 1: Transmit gain $= 20 \times \log\left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10k\Omega$

Note 2: Receive gain $= 20 \times \log\left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10k\Omega$

AD00010F

FAIRCHILD

A Schlumberger Company

F3054/F3057 Monolithic Serial Interface CMOS CODEC/FILTER

Advanced Signal Processing Division

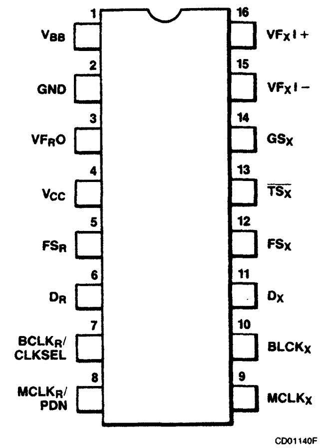
Description

The F3054, F3057 family consists of μ-law and A-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using Fairchild's advanced Double-Poly Silicon Gate CMOS process.

The transmit portion of each device consists of an input gain adjust amplifier, an active RC pre-filter, a switched-capacitor band-pass filter, and a compressing encoder with auto-zero circuitry. The active RC pre-filter eliminates very high frequency noise, and the switched-capacitor filter rejects signals below 200 Hz and above 3400 Hz. The compressing encoder samples the filtered signal and encodes it in the compressed μ-law or A-law PCM format. The receive portion of each device consists of an expanding decoder, which reconstructs the analog signal from the compressed μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

- **Complete Codec and Filtering System Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With Sin X/X Correction**
  - **Active RC Noise Filter**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **μ-Law, 16 Pin — F3054**
- **A-Law, 16 Pin — F3057**
- **Meets or Exceeds All D3/D4 and CCITT Specifications**
- **±5.0 V Operation**
- **Low Operating Power — Typically 60 mW**
- **Power-Down Standby Mode — Typically 3.0 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**

Connection Diagram (Top View)



Order Information

Device Code	Package Code	Package Description
F3054DC	FW	Ceramic DIP
F3057DC	FW	Ceramic DIP

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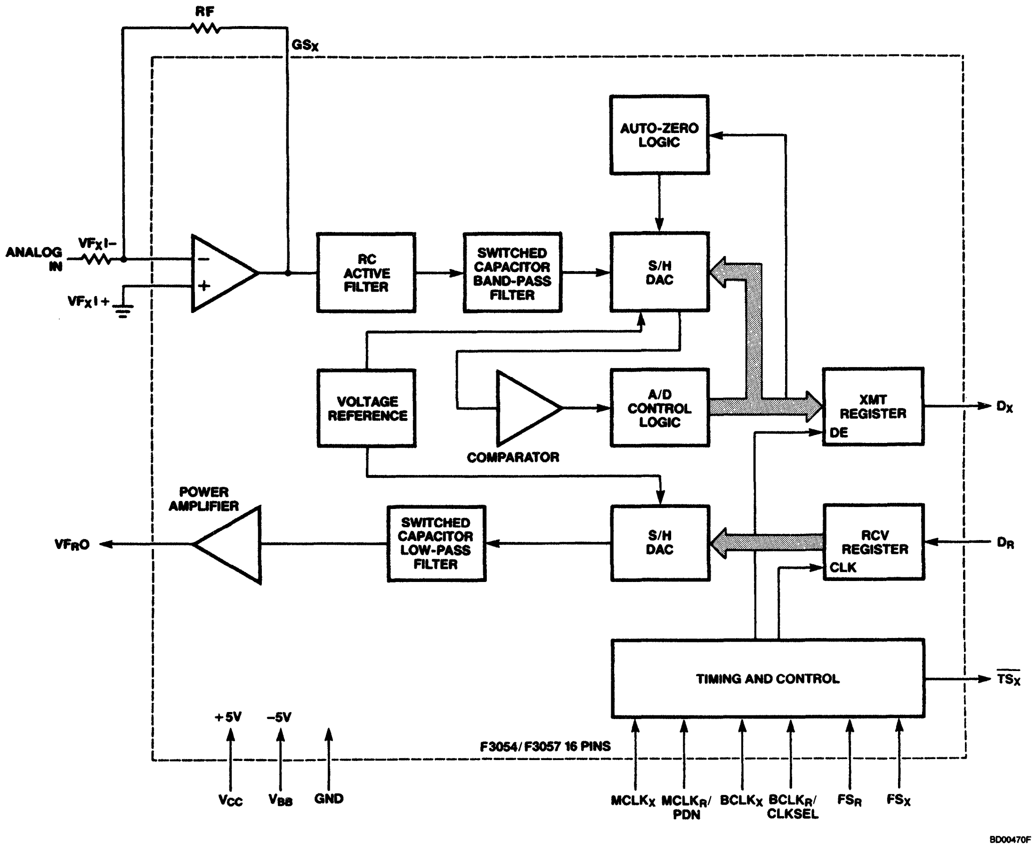
Figure 1 Block Diagram



Pin Description

Pin No.	Name	Function
1	V_{BB}	Negative power supply pin. $V_{BB} = -5\ V \pm 5\%$.
2	GND	Ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply pin. $V_{CC} = +5\ V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after FS_R leading edge. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCKL_R$. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions *(see Table 1).*
8	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
11	D_X	The 3-state PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train; see *Figures 2* and *3* for timing details.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

Power-Up

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, two power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the second is to hold both FS_X and FS_R inputs continuously low — the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The 3-state PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

Synchronous Operation

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Functional Description (Cont.)

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. *Table 1 indicates* the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the 3-state D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

Table 1 Selection of Master Clock Frequencies

	Master Clock Frequency Selected	
$BCLK_R$/CLKSEL	**F3057**	**F3054**
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Asynchronous Operation

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the F3057, and 1.536 MHz or 1.544 MHz for the F3054 and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (*see Pin Description*). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$, which must be a clock. The logic levels *shown in Table 1* are not valid for asynchronous operation. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

Short Frame Sync Operation

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships *specified in Figure 2.* With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X 3-state output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

Long Frame Sync Operation

To use the long frame sync mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships *specified in Figure 3.* Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X 3-state output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

Transmit Section

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, *see Figure 4.* The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of an RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 128 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of compressing type according to μ-law (F3054) or A-law (F3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5 V peak (*see table of Transmission Characteristics*). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which total 290 μs.

Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

Receive Section

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 128 kHz. The decoder is A-law (F3057) or μ-law (F3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a power amplifier capable of driving a 600 Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

V_{CC} to GND	7.0 V
V_{SS} to GND	−7.0 V
Voltage at any Analog Input or Output	V_{CC} + 0.3 V to V_{SS} − 0.3 V
Voltage at any Digital Input or Output	V_{CC} + 0.3 V to GND − 0.3 V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics Unless otherwise noted: V_{CC} = 5.0 V ± 5%, V_{BB} − 5.0 V ± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
Operating Current						
$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current			6.0	9.0	mA
$I_{BB}1$	Active Current			6.0	9.0	mA
Digital Interface						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			0.4 0.4	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	2.4			V
I_{IL}	Input Low Current	GND ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State	D_X, GND ≤ V_O ≤ V_{CC}	−10		10	μA
Analog Interface With Transmit Input Amplifier						
I_IXA	Input Leakage Current	−2.5 V ≤ V ≤ +2.5 V, VF_XI + or VF_XI −	−200		200	nA
R_IXA	Input Resistance	−2.5 V ≤ V ≤ +2.5 V, VF_XI + or VF_XI −	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1.0	3.0	Ω

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Electrical Characteristics (Cont.) Unless otherwise noted: V_{CC} = 5.0 V ± 5%, V_{BB} −5.0 V ± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \geqslant$ 10 kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI + to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1.0	2.0		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
Analog Interface With Receive Amplifier Output						
R_ORF	Output Resistance	Pin VF_RO		1.0	3.0	Ω
R_LRF	Load Resistance	VF_RO = ±2.5 V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
Timing Specifications						
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2 V	160			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6 V	160			ns
t_{RB}	Rise Time of Bit Clock	t_{PS} = 488 ns			50	ns
t_{FB}	Fall Time of Bit Clock	t_{PB} = 488 ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns

Electrical Characteristics (Cont.) Unless otherwise noted: V_{CC} = 5.0 V ± 5%, V_{BB} −5.0 V ± 5%, GND = 0 V, T_A = 0°C to 70°C; typical characteristics specified at V_{CC} = 5.0 V, V_{BB} = −5.0 V, T_A = 25°C; all signals are referenced to GND.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{SF}	Set-Up time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long)(Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long)(Note 1)	100			ns
t_{HBF1}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160			ns

Note

1. For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

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Figure 2 Timing Diagram Short Frame Sync Timing

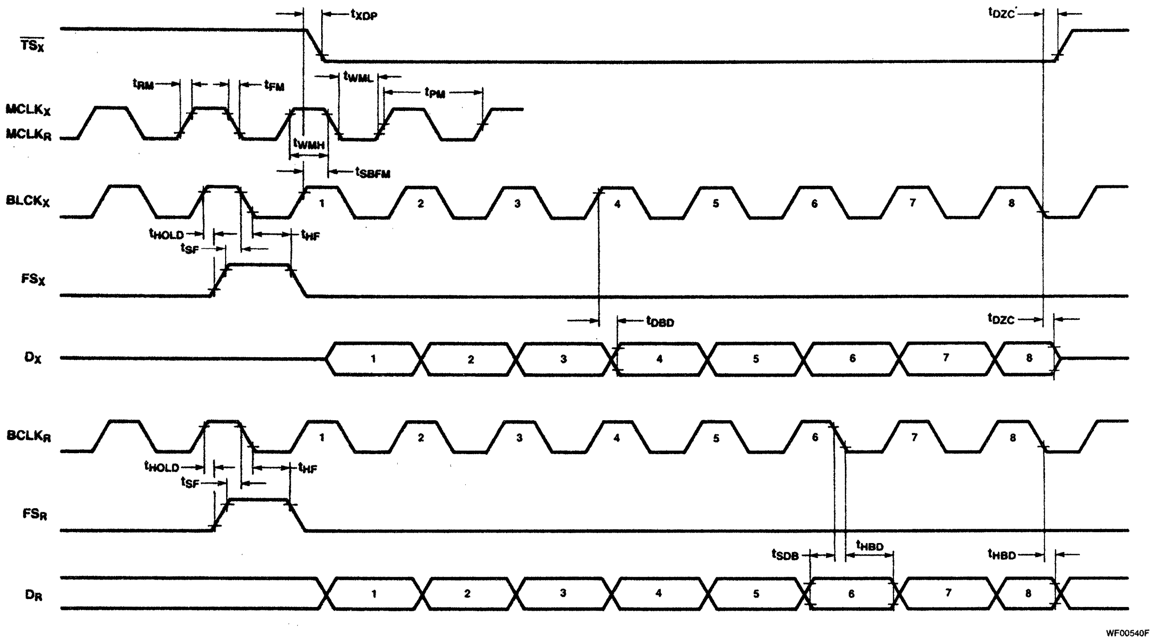
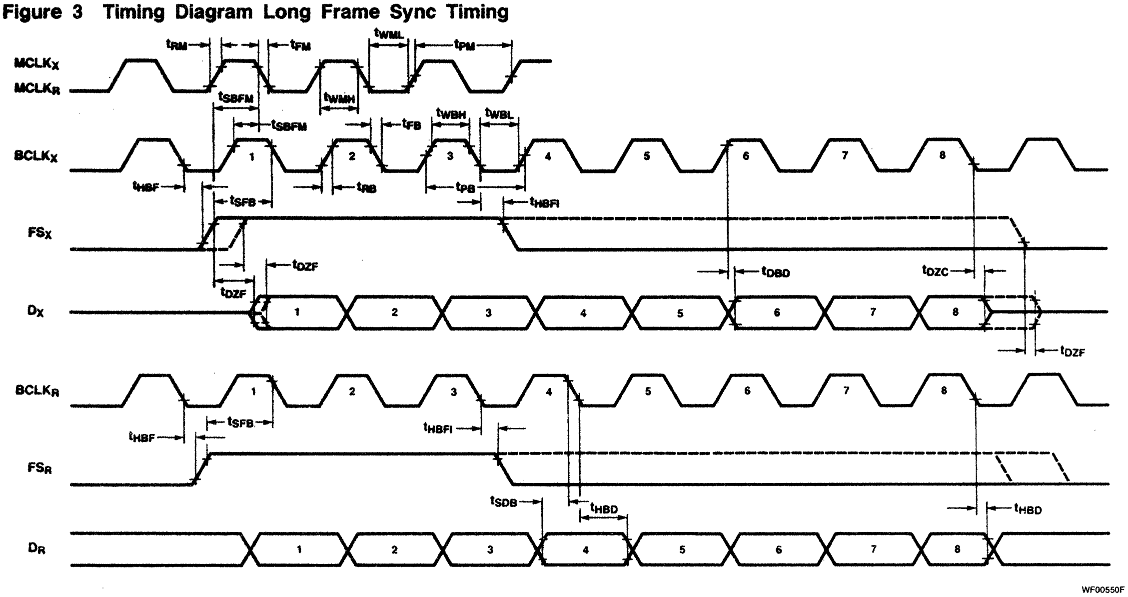


Figure 3 Timing Diagram Long Frame Sync Timing



Transmission Characteristics Unless otherwise specified: T_A = 0°C to 70°C, V_{CC} = 5.0 V ± 5%, V_{BB} = −5.0 V ± 5%, GND = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
Amplitude Response						
	Absolute Levels	Nominal 0 dBm0 Level is 4.0 dBm (600 Ω) 0 dBm0 F3054 F3057		 1.2276 1.2276		 Vrms Vrms
t_{MAX}		Max Overload Level F3054 (3.17 dBm0) F3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CC} = 5 V, V_{BB} = −5 V Input at GS_X = 0 dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz – 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 70°C		± 0.1	dB	
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%			± 0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_XI + = −40 dBm0 to +3 dBm0 VF_XI + = −50 dBm0 to −40 dBm0 VF_XI + = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CC} = 5 V, V_{BB} = −5 V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A = 0°C to 70°C			± 0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5 V ± 5%, V_{BB} = −5 V ± 5%			± 0.05	dB

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0\ V \pm 5\%$, $V_{BB} = -5.0\ V \pm 5\%$, GND = 0 V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded − 10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0	−0.2		0.2	dB
		PCM Level = −50 dBm0 to −40 dBm0	−0.4		0.4	dB
		PCM Level = −55 dBm0 to −50 dBm0	−1.2		1.2	dB
V_{RO}	Receive Output Drive Level	$R_L = 600\ \Omega$	−2.5		2.5	V
Envelope Delay Distortion With Frequency						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz		195	220	μs
		f = 600 Hz − 800 Hz		120	145	μs
		f = 800 Hz − 1000 Hz		50	75	μs
		f = 1000 Hz − 1600 Hz		20	40	μs
		f = 1600 Hz − 2600 Hz		55	75	μs
		f = 2600 Hz − 2800 Hz		80	105	μs
		f = 2800 Hz − 3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1000 Hz	−40	−25		μs
		f = 1000 Hz − 1600 Hz	−30	−20		μs
		f = 1600 Hz − 2600 Hz		70	90	μs
		f = 2600 Hz − 2800 Hz		100	125	μs
		f = 2800 Hz − 3000 Hz		145	175	μs
Noise						
N_{XC}	Transmit Noise, C Message Weighted	F3054 $VF_XI+ = 0$ V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	F3057 $VF_XI+ = 0$ V		−74	−69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	F3054 PCM Code Equals Alternating Positive and Negative Zero		8.0	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	F3057 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI+ = 0$ Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI+ = 0$ Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms, f = 0 kHz − 50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI+ = 0$ Vms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms, f = 0 kHz − 50 kHz	40			dBC

Transmission Characteristics (Cont.) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0\ V \pm 5\%$, $V_{BB} = -5.0\ V \pm 5\%$, GND = 0 V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{CC} = 5.0\ V_{DC} + 100$ mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero $V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 Hz – 4000 Hz f = 4 kHz – 25 kHz f = 25 kHz – 50 kHz	 40 40 36			 dBC dB dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz – 3400 Hz Input Applied to VF_XI+, Measure Individual Image Signals at VF_RO 4600 Hz – 7600 Hz 7600 Hz – 8400 Hz 8400 Hz – 100,000 Hz			 -32 -40 -32	 dB dB dB
Distortion						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 33 36 29 30 14 15			 dBC dBC dBC dBC dBC dBC
SFD_X	Single Frequency Distortion, Transmit				-46	dB
SFD_R	Single Frequency Distortion, Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz – 3400 Hz			-41	dB
Crosstalk						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz – 3400 Hz D_R = Steady PCM Code		-90	-75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz – 3400 Hz, VF_XI = 0 V		-90	-70 (Note 2)	dB

Notes

1. Measured by extrapolation from the distortion test result.
2. CT_{R-X} is measured with a −40 dBm0 activating signal applied at VF_XI+.

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Encoding Format At D_X

	F3054 µ-Law								F3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0 V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Applications Information

Power Supplies

While the pins of the F3054 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

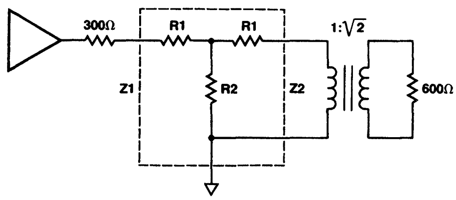
All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 µF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 µF capacitors.

Receive Gain Adjustment

For applications where a F3054 family CODEC/FILTER receive output must drive a 600 Ω load, but a peak swing lower than ±2.5 V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. *Table II* lists the required resistor values for 600 Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600 Ω is obtained if the output impedance of the attenuator is in the range 282 Ω to 319 Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1, Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1, Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \cdot Z_{OC}}$$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

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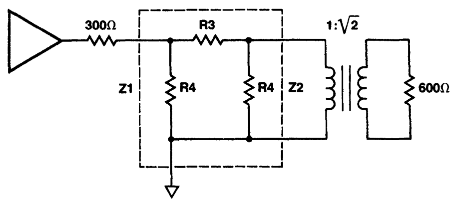
π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1, Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

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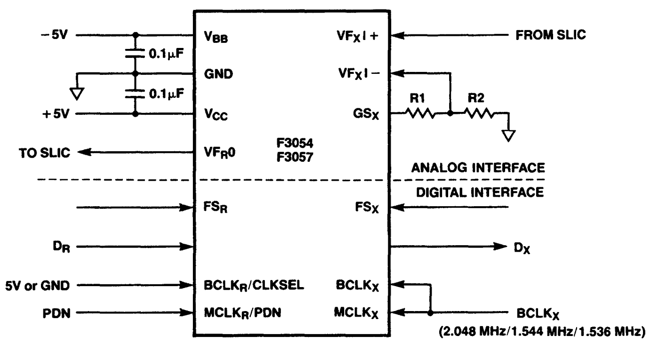
Applications Information (Cont.)

Table II Attentuator Tables for Z1 = Z2 = 300 Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	6.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	179	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Figure 4 Typical Synchronous Application



Note 1: XMIT gain $= 20 \times \log\left(\frac{R1 + R2}{R2}\right)$; $(R1 + R2) > 10K\Omega$

AD00030F

FAIRCHILD

A Schlumberger Company

μAV22 1200 bps Full Duplex Modem

Advance Information May 1986

Advanced Signal Processing Division

Description

The μAV22 1200 bps full duplex modes I.C. is fabricated in Fairchild's advanced Double-Poly Silicon-Gate CMOS process. The monolithic I.C. performs all the signal processing functions required of a CCITT V.22, alternative B compatible modem. Handshaking protocols, dialing control and mode control functions can be handled by a general purpose, single chip μC. The μAV22, μC and several components to perform the telephone line interface and control provide a high performance, cost effective and ultra-low power solution for V.22-compatible modem designs.

The modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a CCITT V.22-compatible modem, as well as additional enhancements. Both 550 Hz and 1800 Hz guard tones and notch filters and DTMF tone generator are on-chip. Switched-capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization. A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 DPSK operation.

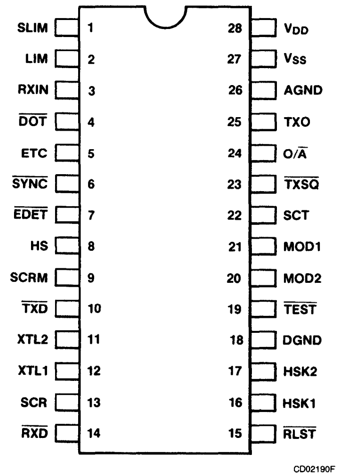
The receive filter and energy detector may be configured for call progress tone detection (dialtone, busy, ringback, voice) providing the front end for a smart dialer.

- **Functions as a CCITT V.22-compatible modem**
- **Interfaces to Single Chip μC Which Handles Handshaking Protocols and Mode Control Functions**
- **DTMF Tone Generation and Call Progress Tone Detection for Smart Dialer Applications**
- **1300 Hz Calling Tone Generator On Chip**
- **Pin and function compatible with the μA212A**
- **On Chip Oscillator Uses 3.6864 MHz Crystal**
- **Few External Components Required**
- **Operates from +5 and −5 Volt Supplies**
- **Low Operating Power: 35 mW Typical**
- **550 Hz and 1200 Hz guard tones and notch filters are on-chip**

Absolute Maximum Ratings

V_{DD} to DGND or AGND	7.0 V
V_{SS} to DGND or AGND	-7.0 V
Voltage at any Input	V_{DD} + 0.3 to V_{SS} −0.3 V
Voltage at any Digital Output	V_{DD} + 0.3 V to DGND −0.3V
Voltage at any Analog Output	V_{DD} + 0.3 V to V_{SS} −0.3 V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Connection Diagram 28-Lead Dip (Top View)



Order Information

Device Code	Package Code	Package Description
μAV22DC	FM	Ceramic DIP
μAV22PC	*	Molded DIP
μAV22QC	*	Molded Surface Mount

*Consult Factory

FAIRCHILD

A Schlumberger Company

µA212A • µA212AT 1200/300 bps Full Duplex Modem

Advanced Signal Processing Division

Description

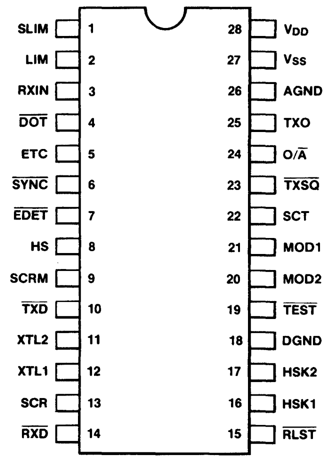
The µA212A and the µA212AT 1200 bps modem circuits are fabricated in Fairchild's advanced Double-Poly Silicon-Gate CMOS process. Either monolithic chip performs all signal processing functions required for a Bell 212A/103 compatible modem. Dialing, handshaking protocols, and mode control functions can be provided by a general purpose single-chip µC. The µA212A or µA212AT and µC; along with several components to handle the control and telephone line interfaces, provide a high performance, cost-effective solution for an intelligent Bell 212A-compatible modem design.

Either modem chip performs the modulation, demodulation, filtering and certain control and self-test functions required for a Bell 212A-compatible modem, as well as additional functional enhancements. Switched capacitor filters provide channel isolation, spectral shaping and fixed compromise equalization for both high and low speed modes.

A novel switched-capacitor modulator and a digital coherent demodulator provide 1200 bps QPSK operation while a separate digital FSK modulator and demodulator handle the 0-300 bps requirement. The µA212AT includes an integral DTMF tone generator on-chip. The µA212A without DTMF generator, is cost optimal for answer-only applications or if an external dialer is present. The µA212A and µA212AT are otherwise pin and firmware compatible. Existing µA212A applications can be easily upgraded to the µA212AT with minor software changes *(see technical bulletin M-1 appended.)* The receive filter and energy detector may be configured for call progress tone detection (dial-tone, busy, ringback, voice), providing the front end for a smart dialer on either the µA212A or µA212AT.

- **Functions as 212A and 103 Compatible Modem**
- **Performs all Signal Processing Functions**
- **Interfaces to Single Chip µC Which Handles Handshaking Protocols and Mode Control Functions**
- **DTMF Tone Generation (µA212AT)**
- **µA212A is Pin and Firmware Compatible with the µA212AT for Easy Upgrade**
- **Call Progress Tone Detection for Smart Dialer Applications**
- **On Chip Oscillator Uses Standard 3.6864 MHz Crystal**
- **Few External Components Required**
- **Industrial Temperature Range Option (-40°C to +85°C)**
- **Operates from +5 and -5 Volt Supplies**
- **Low Operating Power: 35 mW Typical**
- **28-Lead Ceramic DIP, 28-Lead Plastic DIP, and 28-Lead Surface Mount Packages**
- **A µA212A Designer's Kit Is Available**

Connection Diagram 28-Lead Dip (Top View)



CD02190F

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Order Information

Type	Temperature Range	Code	Package
µA212ATDC	0 to +70°C	FM	28-Lead Ceramic DIP
µA212ATDV	-40°C to +85°C	FM	28-Lead Ceramic DIP
µA212ATPC	0 to +70°C	*	28-Lead Molded DIP
µA212ATQC	0 to +70°C	*	28-Lead Molded Surface Mount
µA212ADC	0 to +70°C	FM	28-Lead Ceramic DIP
µA212ADV	-40°C to +85°C	FM	28-Lead Ceramic DIP
µA212APC	0 to +70°C	*	28-Lead Molded DIP

*Consult Factory

Absolute Maximum Ratings

V_{DD} to DGND or AGND	7.0 V
V_{SS} to DGND or AGND	-7.0 V
Voltage at any Input	V_{DD} + 0.3 to V_{SS} -0.3 V
Voltage at any Digital Output	V_{DD} + 0.3 V to DGND -0.3 V
Voltage at any Analog Output	V_{DD} + 0.3 V to V_{SS} -0.3 V
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 s)	300°C

Pin No.	Pin Description	
28	V_{DD}	Positive power supply $V_{DD} = +5$ V
26	AGND	Analog Ground
18	DGND	Digital Ground
27	V_{SS}	Negative power supply $V_{SS} = -5$ V
3	RXIN	Line signal to modem. From active or passive Hybrid output.
25	TXO	Line signal from modem. To active or passive Hybrid input.
24	O/$\overline{A}$	Orig/answer Mode Select. Assigns channels to XMTRS/RCVRS. 1 = Originate mode, 0 = Answer mode. (Note)
23	$\overline{TXSQ}$	Squelch XMTRS in date mode. 0 = Both XMTRS off; 1 = turns on XMTR selected by HS pin. μA212AT: In dialer mode, 0 = DTMF generator OFF/call progress detection. 1 = DTMF generator ON. μA212A: In dialer mode call progress detection only. $\overline{TXSQ}$ must be set to 0.
9	SCRM	Scrambler. "0" disables scrambler and descrambler for testing purposes.
12 11	XTL1 XTL2	Frequency control. 3.6864 MHz XTAL oscillator, operating parallel mode. Provides timing, sample clocks and L.O.'s.
8	HS	Selects modem speed. 1 selects 1200 bps. 0 selects 300 bps. (Note)
6	$\overline{SYNC}$	Selects CHAR ASYNC or BIT SYNC mode. 1 = ASYNC mode: enables XMIT & RCV buffers, sets character length according to MOD1, MOD2 pins. 0 = SYNC mode: disables buffers, selects TX clock source according to MOD1, MOD2 pins. Active only if HS = 1.

Pin No.	Pin Description	
21 20	MOD1 MOD2	Selects character length (ASYNC) or TX clock (SYNC). In ASYNC mode, selects 8, 9, 10 or 11 bit character length; in SYNC mode, selects internal, external or recovered RCV clock as XMTR data clock source. Active only if HS = 1. (*See Table 1*) (Note)
10	$\overline{TXD}$	XMIT Data. Serial data from host. Disconnected when in digital loop.
14	$\overline{RXD}$	RCVD Data. Serial data to host, Internally clamped to mark (= 1) when modem is in digital loop or $\overline{EDET}$ is inactive (= 1).
22	SCT	Serial Clock Transmit. 1200 Hz clock providing XMTR timing in SYNC mode. SCT source (INT., EXT., SLAVE) selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Internal clock provided in ASYNC mode.
5	ETC	External Transmit Clock. 1200 Hz external clock providing XMTR timing in SYNC mode, selected by MOD1, MOD2 pins. $\overline{TXD}$ changes on negative edge, sampled on positive edge. Provided on SCT pin if selected.
13	SCR	Serial Clock Receive. In SYNC mode, 1200 Hz bit clock recovered from RCVD signal. May be pin-selected (MOD1, MOD2) as local transmit clock (SLAVE mode); provided on SCT pin if selected. $\overline{RXD}$ changes on negative edge, sampled on positive edge. Undefined in ASYNC mode.
7	$\overline{EDET}$	Energy Detect. In data mode, $\overline{EDET} = 0$ if valid signal above threshold is present for 155 ± 50 ms, $\overline{EDET} = 1$ if signal below threshold for $> 17 \pm 7$ ms. In dialer mode, follows on/off variations of call-progress tones, when $\overline{TXSQ} = 0$

Note
For μA212AT in dialer mode, O/$\overline{A}$, HS, MOD1 and MOD2 select the DTMF to be generated (*see Table 2*).

Pin No.	Pin Description	
15	$\overline{\text{RLST}}$	Remote Loop Status, used in RDL mode. Responding modem: sets $\overline{\text{RLST}}$ = 0 upon receipt of unscrambled mark for 154 – 231 ms. initiating modem: asserts $\overline{\text{RLST}}$ = 0 upon receipt of scrambled mark for 231 – 308 ms. (*See Table 3*).
1	SLIM	Soft Limiter Output. Connect external 0.033 μF capacitor here.
2	LIM	Comparator input. Connected external 0.033 μF capacitor here.
4	$\overline{\text{DOT}}$	If HS = 1, forces a 1200 bps dotting pattern on the transmit path, for use when programming the 212AT high speed self-test mode. Both RCV and XMIT paths are in $\overline{\text{SYNC}}$ mode during dotting transmission, overriding the setting of $\overline{\text{SYNC}}$, and of HSK1, HSK2. If HS = 0, $\overline{\text{DOT}}$ forces a 155 bps dotting pattern for use in lowspeed self-test mode. 1 = Normal Path, 0 = Dotting.
19 16 17	$\overline{\text{TEST}}$ HSK1, HSK2	When the $\overline{\text{TEST}}$ pin is inactive (high), HSK1 and HSK2 select one of four transmit conditions, for use when programming the Handshake sequences. (*See Table 1*). When $\overline{\text{TEST}}$ is active (low), the HSK1 and HSK2 pins select one of three test conditions, or, alternatively, the dialer mode used for call progress tone detection and DTMF tone generation, μA212AT only.

Functional Description*

Refer to Figure 1.

Transmitter

The transmitter consists of high-speed and low-speed modulators, a transmit buffer and scrambler, and a transmit filter and line driver. In high-speed asynchronous mode, transmit data from the Data Terminal Equipment enters the transmit buffer, which synchronizes the data to the internal 1200 bps clock. Data which is underspeed relative to 1200 bps periodically has the last stop bit sampled twice resulting in an added stop bit. Similarly, overspeed input data periodically has unsampled — and therefore deleted — stop bits. The MOD1 and MOD2 pins choose 8, 9, 10 or 11 bit character lengths. In synchronous mode the transmit buffer is disabled. The transmitter clock source may be chosen by MOD1 and MOD2 internal, external or derived from the recovered received data. A scrambler preceeds encoding to ensure that the line spectrum is sufficiently distributed to avoid interference with the in-band supervisory single-frequency signaling system employed in most Bell System toll trunks. The randomized spectrum also facilitates timing recovery in the receiver. The scrambler is characterized by the following recursive equation:

$$Y_i = X_i \oplus Y_{i-14} \oplus Y_{i-17}$$

where X_i is the scrambler input bit at time i. Y_i is the scrambler output bit at time i and ⊕ denotes the XOR operation.

212A-type modems achieve full-duplex 1200 bps operation by encoding transmitted data by bit-pairs (dibits), thereby halving the apparent data rate. The resultant reduced spectral width allows both frequency channels to coexist in a limited bandwidth telephone channel with practical levels of filtering. The four unique dibits thus obtained are gray-coded and differentially phase modulated onto a carrier at either 1200 Hz (originate mode) or 2400 Hz (answer mode). Each dibit is encoded as a phase change relative to the phase of the preceding signal dibit element:

Dibit	Phase Shift (deg)
00	+90
01	0
11	–90
10	180

At the receiver, the dibits are decoded and the bits are reassembled in the correct sequence. The left-hand digit of the dibit is the one occurring first in the data stream as it enters the modulator after the scrambler. The lowspeed transmitter generates phase-coherent FSK using one of two programmable tone generators. Answer mode mark (2225 Hz) is also utilized as answer tone in both low and high speed operation.

In Dialer mode, both tone generators are employed to generate DTMF tone pairs. The summed modulator outputs drive a lowpass filter which serves as a fixed compromise amplitude and delay equalizer for the phone line and reduces output harmonic energy well below maximum specified levels. The filter output drives an output buffer amplifier with low output impedance. The buffer provides 700 mVrms in data mode, for a nominal –9 dBm level at the line, assuming 2 dB loss in the data access arrangement.

*For additional information contact sales office for Applications Note ASP-1 "Theory of Operation — μA212A" and Technical Bulletins M1, M3 & M4.

DTMF Tone Generation

The μA212AT includes on-chip DTMF generation, using two programmable tone generators. Dialer mode must be selected on $\overline{\text{TEST}}$, HSK1 and HSK2 for DTMF dialing. The O/$\overline{\text{A}}$, HS, MOD1 and MOD2 pins are used to select the required digit according to the encoding scheme *shown in Table 2,* and the tones are turned on and off by the logic level on $\overline{\text{TXSQ}}$. The generated tones meet the applicable CCITT and EIA requirement for tone dialing. DTMF output levels are 1.0 Vrms (low group) and 1.25 Vrms (high group).

Receiver

The received signal from the line-connection circuitry passes through a lowpass filter which performs anti-aliasing and compromise amplitude and delay equalization of the incoming signal. Depending upon mode selection (originate/answer) the following mixer either passes or down converts the signal to the 1200 Hz bandpass filter. In analog loopback mode, the receiver originate and answer mode assignments are inverted, which forces the receiver to operate in the transmitter frequency band. The 1200 Hz bandpass filter passes the desired received signal while attenuating the adjacent transmitted signal component reflected from the line (talker echo). The chosen passband shape converts the spectrum of the received high-speed signal to 100% raised cosine to minimize intersymbol interference in the recovered data. Following the filter is a soft limiter and a signal energy detector. An external capacitor is used to eliminate offset between the soft limiter output and the following limiter.

The energy detector provides a digital indication that energy is present within the filter passband at a level above a preset threshold. Approximately 3 dB of hysteresis is provided between on and off levels to stabilize the detector output. In dialer mode, the detector output is used to provide logic level indication of the presence of call progress tones.

The limiter output drives the QPSK demodulator and the carrier and clock recovery phase-locked loops. The low speed FSK demodulator shares part of the clock recovery loop. The QPSK demodulator and carrier loop form a digital coherent detector. This technique offers a 2 dB advantage in error performance compared to a differential demodulator. The demodulator output are in-phase (I) and quadrature (Q) binary signals which together represent the recovered dibit stream. The dibit decoder circuit utilizes the recovered clock signal to convert this dibit stream to serial data at 1200 bps.

The recovered bit stream is then descrambled, using the inverse of the transmit scrambler algorithm. In synchronous mode the descrambler output is identically the received data, while in asynchronous mode the descrambler output stream is selectively processed by the receive buffer. Underspeed data presented to the transmitting modem passes essentially unchanged through the receive buffer. Overspeed data, which had stop bits deleted at the transmitter, has those stop bits reinserted by the receive buffer. (Generally, stop bit lengths will be elastic). The receive buffer output is then presented to the receive data pin (RXD) at a nominal intracharacter rate of 1219.05 bps.

Master Clock/Oscillator/Divider Chain

The μA212A or μA212AT may be controlled by either a quartz crystal operating in parallel mode or by an external signal source at 3.6864 MHz. The crystal should be connected between XTL1 and XTL2 pins, with a 30 pF capacitor from each pin to digital ground *(see Figure 1).* Crystal requirements; $R_S < 150$ ohms, $C_L = 18$ pF, parallel mode, tolerance (accuracy, temp, aging) less than ±75 ppm. An external TTL drive may be applied to the XTL2 pin, with XTL1 grounded. Internal divider chains provide the timing signals required for modulation, demodulation, filtering, buffering, encoding/decoding, energy detection and remote digital loopback. Timing for line connect and disconnect sequences (handshaking) derives from the host controller, ensuring maximum applications flexibility.

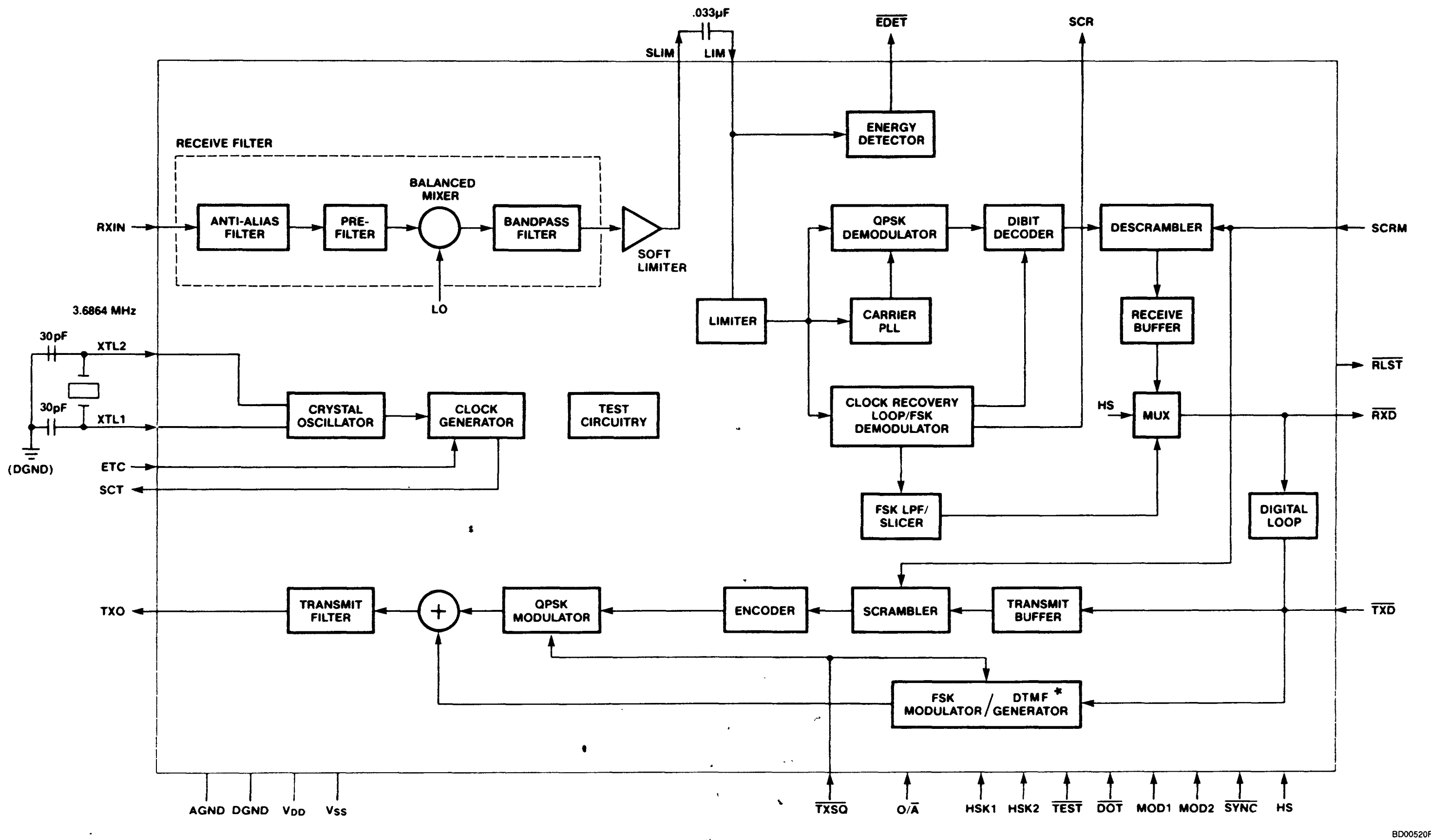
Control Considerations

The host controller, whether a dedicated microcontroller or a digital interface, controls the μA212A or μA212AT as well as the line connect circuit and other IC's. On-chip timing and logic circuitry has been specifically designed to simplify the development of control firmware.

Operating and Test Modes

Table 1 indicates the operating and test modes defined by the eight control pins. The μA212A and μA212AT (together with the host controller) supports analog loopback, and local and remote digital loopback modes. Analog loopback forces the receiver to the transmitter channel. The controller forces the line control circuit on-hook but continues to monitor the ring indicator. This mode is available for low-speed, highspeed synchronous and highspeed asynchronous operation. In local digital loop, the modem I.C. isolates the interface, slaves the transmit clock to SCR (high-speed mode), and loops received data back to the transmitter. In remote digital loop, local digital loop is initiated in the far-end modem by request of the near-end modem, if the far-end modem is so enabled. The μA212A and μA212AT includes the handshake sequences required for this mode; the controller merely monitors $\overline{\text{RLST}}$ and controls remote loopback according to *Table 3.* Remote loop is only available in high-speed mode.

Figure 1 Block Diagram



*µA212AT only

Answer Tone In this mode, 2225 Hz answer tone is transmitted provided $\overline{TXSQ}$ is inactive high (= 1). Receive speed is selected as normal with the HS pin. This permits the speed of the originating modem to be determined while answer tone is continuously transmitted.

Force Continuous Mark Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a mark (logic 1).

Force Continuous Space Disconnects $\overline{TXD}$ pin from the transmitter and forces the signal internally to a space (logic 0).

Analog Loop Receiver is forced to the transmitter channel. With modem on-hook (disconnected from line) signal from TXO is reflected through hybrid to RXIN.

Local Digital Loop Internally connects $\overline{RXD}$ to $\overline{TXD}$ and SCR to SCT. Transmitted data ($\overline{TXD}$) and clock (ETC) are ignored. SCR and SCT are provided. $\overline{RXD}$ is forced to 1.

Remote Digital Loop Initiating modem: If RDL is initiated ($\overline{TEST}$ = 0, HSK1 = 1, HSK2 = 0), $\overline{TXD}$ is isolated, $\overline{RXD}$ is clamped to a 1 and unscrambled mark is transmitted. When high speed scrambled dotting pattern is detected, scrambled mark is transmitted. At this point, upon receipt of scrambled mark, $\overline{RLST}$ is set to 0.

Responding modem: Upon receipt of unscrambled mark when in data mode ($\overline{TEST}$ = HSK1 = HSK2 = 1), $\overline{RLST}$ is set to 0. Upon detecting this the controller responds by setting $\overline{TEST}$ and HSK2 to 0, and the modem I.C. isolates $\overline{TXD}$, clamps $\overline{RXD}$ to 1, and transmits a 1200 bps scrambled dotting pattern. At this point, upon receipt of a scrambled mark signal, the modem I.C. internally loops RCVR data and clock to the XMTR, and sets $\overline{RLST}$ back to 1. (*See Table 3*)

Dialer Mode The μA212AT provides DTMF tone generation and energy indication at $\overline{EDET}$ pin to identify call progress tones, i.e. dial, busy and ringback. The DTMF digit is selected by the levels on O/$\overline{A}$, HS. MOD1 and MOD2 according to Table 2. Tone generation is turned on and off by the level on $\overline{TXSQ}$. 1 = on, 0 = off. The μA212A provides call progress indication only. $\overline{TXSQ}$ must be set to 0.

Electrical Characteristics Unless otherwise noted: $V_{DD} = 5.0$ V ±5%, $V_{SS} = -5.0$ V ±5%, DGND = AGND = 0 V, $T_A = 0°C$ to 70°C, typical characteristics specified at $V_{DD} = 5.0$ V, $V_{SS} = -5.0$ V, $T_A = 25°C$; all digital signals are referenced to DGND, all analog signals are referenced to AGND.

Table 1 Operating and Test Modes

$\overline{DOT}$	HS	$\overline{SYNC}$	MOD1	MOD2	$\overline{TEST}$	HSK1	HSK2	Description	SCT
0	–	X	X	X	1	1	1	Dotting Pattern (155 or 1200 bps)	INT
1	–	–	–	–	1	0	0	Answer Tone	X
1	–	–	–	–	1	0	1	Force Continuous Mark	X
1	–	–	–	–	1	1	0	Force Continuous Space	X
1	1	1	0	0	1	1	1	ASYNC, 8 Bit	INT
1	1	1	0	1	1	1	1	ASYNC, 9 Bit	INT
1	1	1	1	1	1	1	1	ASYNC, 10 Bit	INT
1	1	1	1	0	1	1	1	ASYNC, 11 Bit	INT
1	1	0	1	1	1	1	1	SYNC, Internal	INT
1	1	0	1	0	1	1	1	SYNC, Slave	SCR
1	1	0	0	1	1	1	1	SYNC, External	ETC
–	–	–	–	–	0	0	1	Analog Loop	ETC
1	–	X	X	X	0	1	1	Local Digital Loop	SCR
1	1	X	X	X	0	1	0	Response to Far End Request for RDL	SCR
1	0	X	X	X	–	–	–	Low Speed Mode	X
1	X	X	X	X	0	0	0	Dialer Mode, Note 1	X
1	1	–	–	–	0	1	0	Remote Digital Loop Initiate	X

Key:
SCT – TX Buffer and PSK Modulator Clock
SCR – Receive Clock
ETC – External Clock Input
INT – Internal 1200 Hz Clock
X – Don't Care
— – Set as appropriate for desired operating condition.

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Table 2 DTMF Encoding[2] (μA212AT only)

O/$\overline{A}$	HS	MOD1	MOD2	DTMF Digit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	*
1	0	1	1	#
1	1	0	0	A
1	1	0	1	B
1	1	1	0	C
1	1	1	1	D

Notes
1. DTMF digit is selected according to Table 2 for the μA212AT. $\overline{TXSQ}$ enables the tone generator: 1 = ON, 0 = OFF. $\overline{TXSQ}$ = 0 allows energy detection of call progress tone in both the μA212A and μA212AT.
2. For DTMF to operate dialer mode must be asserted. $\overline{TEST}$, HSK1 and HSK2 must be = 0.

Table 3 Remote Digital Loopback (RDL) Command Sequences

Modem Action	Controller Action	$\overline{TEST}$	HSK1	HSK2	$\overline{RLST}$
Data Mode		1	1	1	1
Initiate RDL:	"INITIATE RDL"	0	1	0	1
Disable scrambler					
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Transmit unscrambled mark (U.M.)					
Recognize Dotting for 231 – 308 ms					
Enable scrambler					
Transmit scrambled mark (S.M.)					
Recognize S.M. for 231 – 308 ms					
Connect $\overline{TXD}$					
Unclamp $\overline{RXD}$					
"RDL ESTABLISHED"		0	1	0	0
Response to far end request:		1	1	1	0
U.M. recognized for 154 – 231 ms					
"RDL REQUESTED"	"RDL RESPONSE OK"	0	1	0	0
Disconnect $\overline{TXD}$					
Force 1 on $\overline{RXD}$					
Force Sync Slave Mode					
Transmit Dotting					
S.M. recognized					
Internally loop Receiver to Transmitter					
"RDL ESTABLISHED"		0	1	0	1
Terminate RDL:	$\overline{TXSQ}$ active 80 ms	1	1	1*	0
Reset to Data Mode		1	1	1	1

*$\overline{TEST}$ = HSK1 = HSK2 = 1 may be asserted at anytime after "RDL ESTABLISHED" and before terminating.

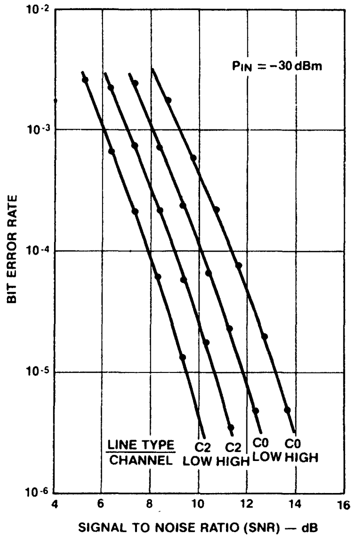
Energy Detector

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{thon}	Off/On Threshold	Voltage Level at RXIN		6.5		mV_{rms}
V_{thoff}	On/Off Threshold	Pin In Data Mode		5.2		
t_{on}	Energy Detect Time Data Mode	at $\overline{EDET}$ Pin	105	155	205	ms
t_{off}	Loss of Energy Detect Time		10	17	24	ms
V_{thon}	Dialer Mode					
V_{thon}	Off/On Threshold Dialtone	Voltage Level at RXIN		10		mV_{rms}
V_{thon}	Off/On Threshold Busy/Ringback	Pin in Dialer Mode		4.6		
t_{on}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)	At $\overline{EDET}$ Pin	25	30	35	ms
t_{off}	Energy Detect in the Dialer Mode (Detecting Call Progress Tones)		30	36	42	ms

System Performance

Symbol	Characteristic	Condition	Min	Typ	Max	Units
BER	**Bit Error Rate:** SNR required for BER = 10^{-5} @ 1200 bps on a 3002-C0 line, with 5 kHz white noise referred to 3 KHz. Figures shown are for originate mode. (Note: P_{line} values assume 4 dB net gain from line to RXIN)	P_{line} = −30 dBm P_{line} = −44 dBm		13 14		dB dB
	Telegraph Distortion	Back-to-Back, 300 bps (Low Speed Mode)		10		% Peak

Figure 2 Bit Error Rate vs Signal-to-Noise Ratio



Note
BER measured in synchronous mode, using an AEA S3A channel simulator.

Analog Line Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{line}	Output Level at TXO: Data Mode			0.7		V_{rms}
V_{tonh}	Output Level at TXO: DTMF HIGH Group			1.1		V_{rms}
V_{tonl}	Output Level at TXO: DTMF LOW Group			0.9		V_{rms}
$V_{\overline{TXSQ}}$	Output level at TXO:			0.5		mV_{rms}
P_{ext}	Extraneous frequency output relative to DTMF power.	Any DTMF digit			−20	dB
V_{oo}	Output Offset at TXO			5.0		mV

11

Masterclock Input

Symbol	Characteristic	Condition	Min	Typ	Max	Units
F_{clock}	Clock Frequency			3.6864		MHz
T_{olclk}	Clock Frequency Tolerance		-.01		+.01	%
V_{exth}	External Clock Input HIGH	XTL2 driven and XTL1 grounded	4.5			V
V_{extl}	External Clock Input LOW	XTL2 driven and XTL1 grounded			0.5	V

Digital Interface

Symbol	Characteristic	Condition	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.6	V
V_{IH}	Input Voltage HIGH		2.2			V
V_{OL}	Output Voltage LOW	$I_L = 2.0$ mA			0.6	V
V_{OH}	Output Voltage HIGH	$I_L = -2.0$ mA	3.0			V
I_L	Input Current LOW	DGND $\leqslant V_{IN} \leqslant V_{IL}$, All Digital Inputs	-100			μA
I_{IH}	Input Current HIGH	$V_{IH} \leqslant V_{IN} \leqslant V_{DD}$	-50			μA
I_{DD}	Operating Current	$V_{DD} = 5.0$ V No Analog Signals		4.3	10	mA
I_{SS}	Operating Current	$V_{SS} = -5.0$ V No Analog Signals		-2.7	-5.0	mA

Transmit Buffer (Character Asynchronous Mode)

Symbol	Characteristic	Condition	Min	Typ	Max	Units
L_{txchar}	Input Character Length	Start bit + data bits + stop bit	8		11	bits
R_{txchar}	Intracharacter Signaling Rate	At $\overline{TXD}$ pin	1170	1200	1212	bps
L_{break}	Input Break Sequence Length	At $\overline{TXD}$ pin	23			bits

Receive Buffer (Character Asynchronous Mode) Carrier Frequencies and Signaling Rates

Symbol	Characteristic	Condition	Min	Typ	Max	Units
R_{txchar}	Intracharacter Signaling Rate	At $\overline{RXD}$ pin		1219.05		bps
F_{cxr} (ORIG)	HS Cxr Freq. (Orig. Mode)	Unmodulated Carrier		1200		Hz
F_{cxr} (ANS)	HS Cxr Freq. (Ans. Mode)	Unmodulated Carrier		2400		Hz
Baud	Dibit Rate	High Speed Mode		600		Baud
F_{mark} (ORIG)	Mark Frequency Originate Mode (1270)	Low Speed Mode		1269.42		Hz
F_{space} (ORIG)	Space Frequency Originate Mode (1070)	Low Speed Mode		1066.67		Hz
F_{mark} (ANS)	Mark Frequency Answer Mode/Answer Tone (2225)	Low Speed Mode		2226.09		Hz
F_{space} (ANS)	Space Frequency Answer Mode (2025)	Low Speed Mode		2021.05		Hz
F_{tonl}	DTMF Low Frequency Tone Group	Dialer Mode		698.2 771.9 853.3 942.3		Hz
F_{tonh}	DTMF High Frequency Tone Group	Dialer Mode		1209.4 1335.7 1476.9 1634.0		Hz
T_{ol}	Tolerance of all above Frequencies/Data Rates		−0.01		+0.01	%
bps	Data Rate	Low Speed Mode	0		300	bps

FAIRCHILD

A Schlumberger Company

DTMF Dialing, the μA212A and μA212AT

Technical Bulletin M-1 April 1986

Garry Shapiro, Advanced Signal Processing Division

The μA212A — the world's first and lowest power 1200/300 b/s single-chip modem — will be joined, at about mid-year, by the μA212AT. The second in a series of Fairchild modem IC products, the μA212AT is pin-compatible with the μA212A with the addition of an *integral DTMF tone generator.* This Bulletin summarizes factors to be considered in current μA212A-based modem designs for migration to the μA212AT.

DTMF Access

The μA212AT DTMF tone generator is accessed via the *Dialer* mode, which is asserted by setting $\overline{TEST}$ = HSK1 = HSK2 = 0. In the μA212A, *Dialer* mode offers only call-progress tone detection, but, in the μA212AT, both call-progress tone detection and DTMF tone generation are provided. The DTMF output is enabled by $\overline{TXSQ}$ = 1 and disabled by $\overline{TXSQ}$ = 0; $\overline{EDET}$ should be ignored when DTMF tones are being generated. *See Table 1.1.*

Table 1.1. Dialer Mode

$\overline{TXSQ}$	μA212A	μA212AT
0	Call-progress	Call-progress
1	Call-progress	DTMF generation

DTMF Tone-Pair Selection

The μA212AT employs 4 pins (O/$\overline{A}$, HS, MOD1, and MOD2) to generate 1 each of the 4 LOW and 4 HIGH group DTMF tones; nominal tone frequencies are *shown in Table 1.2. Table 1.3* displays the DTMF Encoding matrix.

Table 1.2 Tone Frequencies (Hz)

Low Group		High Group	
F (Nom.)	F (Act.)	F (Nom.)	F (Act.)
697	698.2	1209	1209.4
770	771.9	1336	1335.7
852	853.3	1477	1476.9
941	942.3	1633	1634.0

Output Characteristics

Table 1.4 summarizes nominal output levels at the TXO pin for Data mode, and for the DTMF Low and High tone groups. Absolute values and values relative to Data mode are shown.

Mode	$V_{txo(rms)}$	Relative (dB)
Data	0.70	0
DTMF Low	0.88	+2
DTMF High	1.11	+4

Therefore, if Data mode output power to a 600 Ω load is −9 dBm, tone output power is −7 dBm (Low group) and −5 dBm (HIGH group). These levels, as well as harmonic and out-of-band energy values conform to the requirements of EIA RS-496.

μA212AT Design-In Considerations

The μA212A and μA212AT are pin-compatible and functionally identical for all modes except DTMF tone generation. The μA212AT can therefore replace the μA212A in all current and future designs, provided that the following considerations are observed:

- **Ensure Proper Control Of The $\overline{TXSQ}$ Pin When In Dialer Mode.** *See Table 1.1.*
- **Provide μController Lines For The O/$\overline{A}$, HS, MOD1 And MOD2 Pins,** if any are not presently provided.
- **Plan For Replacement Of The Present Tone Dialing Scheme.** Current μA212A designs with DTMF dialing often employ a dialer chip or a DAC. Ensure that downstream removal of such parts will not affect the design.
- **Allow ROM Space.** Since DTMF control code replaces the previous scheme, this should not usually be a problem.

Table 1.3 DTMF Encoding Matrix
($\overline{TEST}$ = HSK1 = HSK2 = 0, $\overline{TXSQ}$ = 1)

O/$\overline{A}$	H/S	MOD1	MOD2	DTMF Digit
0	0	0	0	0
		0	1	1
		1	0	2
		1	1	3
0	1	0	0	4
		0	1	5
		1	0	6
		1	1	7
1	0	0	0	8
		0	1	9
		1	0	*
		1	1	#
1	1	0	0	A
		0	1	B
		1	0	C
		1	1	D

FAIRCHILD

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μA212K 1200/300 bps Full Duplex Modem Designer's Kit

Advanced Signal Processing Division

Description

The μA212K Designer's Kit supports the Fairchild μA212A modem. The purpose of the kit is essentially threefold:

- To provide a convenient means of demonstrating the capabilities, features and performance of the μA212A- the world's first single-chip 212A modem IC.
- To facilitate the design of applications-specific control firmware for the μA212A.
- To provide a FCC registered DAA design reference and Hybrid design support.

The Designer's Kit includes the following materials:

1. The μA212A Modem Board is a 1200/300 b/s, full-duplex, originate/answer, stand alone "smart" 212A modem board. Compatible with the Hayes Smartmodem 1200™ command set, Demo Board supports features not found on Smartmodem™, including call progress tone detection (in addition to audio line monitoring) and support of the Remote Loopback test mode. Demo Board showcases all features and modes of the μA212A IC, except the use of 8 and 9 bit asynchronous characters, which are incompatible with the Hayes "AT" protocol. Synchronous operation is available, and is particularly useful for bit error rate testing. All modes and options are via software control.

Demo Board operates with received line signals from −45 to >−10 dBm, and transmits at a nominal −10 dBm into a 600 Ω load.

2. The μA212A Designer's Manual

a. *Overview and Hardware.* This part summarizes features, interface requirements (power, control, telephone line), and modem architecture. It enables the user to quickly go on-line and to become familiar with modem operation.

b. *μA212A Modem Demonstration Program (Ver. 1.27).* This is an extensive discussion of Demo Board control firmware, and is primarily intended to assist designers developing firmware for μA212A-based products. It is presented within the framework of the familiar Hayes Smartmodem 1200™ command set, and may be considered a superset of that de-facto industry standard. Although written for the 6801 microcontroller, the organization and modularization of the code are applicable to most of the microcontrollers currently available.

3. To Assist Hardware and Firmware Development

a. a circuit schematic diagram and parts list

b. Technical Bulletin M3: *DAA/Hybrid Design Programs for the μA212A*

c. a 5.25" floppy disk containing 6801 source listings and utilities. Object listings are also available to those requiring them.

Consult your local Fairtech™ Center, Salesoffice or Advanced Signal Processing Division for further details, reference materials and information regarding new modem and design support products.

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Figure 1 μA212K

Aerospace and Defense Processing

Aerospace and Defense Processing

Processing to MIL-M-38510 and MIL-STD-883 is performed by a totally dedicated Business Unit within the Linear Division of Fairchild to serve the unique Linear components requirements of our various military customers. Fairchild Linear has been committed to the Linear Hi Rel program for many years and intends to continue to maintain a leadership position in that market segment.

The Aerospace and Defense program offers four levels of processing flows as noted below. These flows would normally satisfy a majority of customer requirements.

- **Jan-Level "B" — Full compliance to MIL-M-38510 Jan program and QPL listings as published by Defense Electronics Supply Center.**
- **Military (DESC) Drawing — Conformance to Class "B" process requirements to DESC selected item drawings.**
- **"QB" Flow — Conformance to Class "B" process requirements of MIL-STD-883 to Fairchild MIL temperature range data sheet electricals.**
- **"QS" Flow — Conformance to Class "S" process requirements of MIL-STD-883 to Fairchild MIL temperature range data sheet electricals and including wafer lot acceptance per *Figure 3A.***

JAN Qualified (MIL-M-38510) Class "B" Program

The JAN Program offers the customer a standard of product processing, quality and reliability that is well documented by the manufacturer and monitored by the Defense Electronics Supply Center (DESC) of the U.S. Government. The products are manufactured in the U.S. in a government certified facility to the requirements of MIL-M-38510 and individual product specifications as called out in the MIL-M-38510 "Slash Sheets". The DESC certification is based on standardized documentation for design, processing, test methods, laboratory suitability, product assurance program, and personnel training. Facilities and documentation are audited by DESC prior to certification and periodically thereafter.

Fairchild Linear maintains a very active MIL-M-38510 Qualified Products List (QPL) Program and has maintained a leadership position in the total number of Linear QPL's for many years.

An outline of the JM35810 Class "B" flow is given in *Figure 1.*

DESC Selected Item Drawings

DESC Selected Item Drawings or Military Drawings provide and industry standard specification in compliance with Class "B" requirements for devices that are not JAN qualified. These products are dual marked with the DESC Military Drawing Number as well as the industry standard device number.

Linear "QB" Flow (MIL-STD-883 Class "B")

Fairchild's "QB" process flow can fill customer needs when a desired product is not available on JAN QPL or when system requirements call for a cost effective but reliable alternative to the full JAN program. The product is processed to MIL-STD-883 methods as specified in *Figure 1.* Electrical testing is performed to Fairchild Standard Schematic as defined on the data sheets.

"QS" Flow

Fairchild Linear offers a capability to fulfill basic processing requirements of Class "S" at wafer fabrication, assembly, environmental screening and test/finish on selected popular devices. It is our intent to standardize the processing of Class "S" products to the "QS" flow shown in *Figures 3A, 3B, and 3C* so that customer requirements for Class "S" can be accommodated. Fairchild does not currently hold a Class "S" certification from DESC.

Figure 1 "QB" and JAN Class "B" Process Flow

Description	"QB" Flow MIL-STD-883 Test Method and Description	JAN Class "B" Flow MIL-STD-883 Test Method and Description
Internal Visual	2010 Cond. B	2010 Cond. B
Stabilization Bake	1008 Cond. C (note 1)	1008 Cond. B (note 1)
Temperature Cycling	1010 Cond. C	1010 Cond. C
Constant Acceleration (Centrifuge)	2001 Cond. E Y_1 Orientation only (note 2)	2001 Cond. Y_1 Orientation only (note 2)
Interim (Pre Burn-In) Electrical Parameters	Per Applicable Test Spec.	Per Applicable Device Specification (Slash Sheet)
Burn-In Test	1015, 160 Hrs. at 125°C or Per Table 1 of Method 1015	1015, 160 Hrs. at 125°C or Per Table 1 of Method 1015
Interim (Post Burn-In) Electrical Parameters	Per Applicable Test Spec.	Per Applicable Device Specification (Slash Sheet)
Percent Defective Allowable (PDA) Calculation	5%	5%
Final Electrical Test	Per Applicable Test Spec.	Per Applicable Device Specification (Slash Sheet)
Seal (Hermiticity)	1014	1014
Quality Conformance Inspection	5005 Groups A, B, C and D Limits and Conditions Per Applicable Linear "QB" Data Sheet	5005 Groups A, B, C and D Limits and Conditions Per Applicable Device Specification (Slash Sheet)
External Visual	2009	2009

Notes:
1. Defines minimum time and temperature, greater temperature and/or longer time used for some packages types.
2. Or lower G levels as allowed for larger packages per MIL-STD-883, Method 5004.

Figure 2 JAN Part Numbering System

J M 38510/ 101 01 B G C

JAN Designator
Cannot be market with "J" unless qualified on Part I or Part II of the QPL

General Procurement Spec

Refers to Detail Spec
101 Op Amps
102 Voltage Regulators
103 Comparators
104 Interface
106 Voltage Followers
107 Positive Fixed Voltage Regulators
108 Transistor Arrays
109 Timers
110 Quad Op Amps
112 Voltage Comparator
113 D to A Converter
115 Negative Fixed Voltage Regulators
117 Positive Adjustable Voltage Regulators
118 Negative Adjustable Voltage Regulators
119 Low Power, Low Noise, Bi-Fet Op Amps

Defines Device Type

Processing Level
S
B

Package Type
A 14-lead 1/4 x 1/4 Flatpak
B 14-lead 1/4 x 1/2 Flatpak
C 14-lead 1/4 x 3/4 Dip
D 14-lead 1/4 x 3/8 Flatpak
E 16-lead 1/4 x 7/8 Dip
F 16-lead 1/4 x 3/8 Flatpak
G 8-lead Can
H 10-lead 1/4 x 1/4 Flatpak
I 10-lead Can
J 24-lead 1/2 x 1 1/4 Dip
K 24-lead 3/8 x 5/8 Flatpak
L 24-lead 3/8 x 1/2 Flatpak
X 3-lead TO-5 Can
Y 2-lead TO-3 Can
Z 24-lead 1/4 x 3/8 Flatpak
2 20 Terminal LCC

Lead Finish
A Hot Solder Dip
B Tin Plate
C Gold Plate
X Any Finish Above

Linear JAN Generic Part Numbers

M38510/	01	02	03	04	05	06	07	08	09	10
101	741	747	101A	108A	2101A	2108A	118	1558		
102	723									
103	710	711	111	2111						
104	55107	55108	9614	9615						
106	110	2110								
107	109	78M05	78M12	78M15	78M24	7805	7812	7815	7824	
108	3045									
109	555									
110	148	4156	4136	124						
112	139									
113	0802	0801								
115	79M05	79M12	79M15	79M24	7905	7912	7915	7924		
117	117H	117K	150	138						
119	771	772	774							

Note
Dated material. Please contact Fairchild for latest revisions.

"QS" Processing

The Linear Division has a standardized "QS" flow for all processing steps through Assembly, Test, Burn-In and Finish that will meet the requirements of a majority of customers and thus reduce the need for custom Class "S" process flows.

The flow charts that follow provide the major steps and acceptance criteria utilized for the processes and should form the basis for any Class "S" business negotiations with Linear Marketing. These flow charts will also provide a prospective customer with Fairchild Linear's capabilities in Class "S" processing.

Figure 3A "QS" Minimum Wafer Lot Acceptance Steps

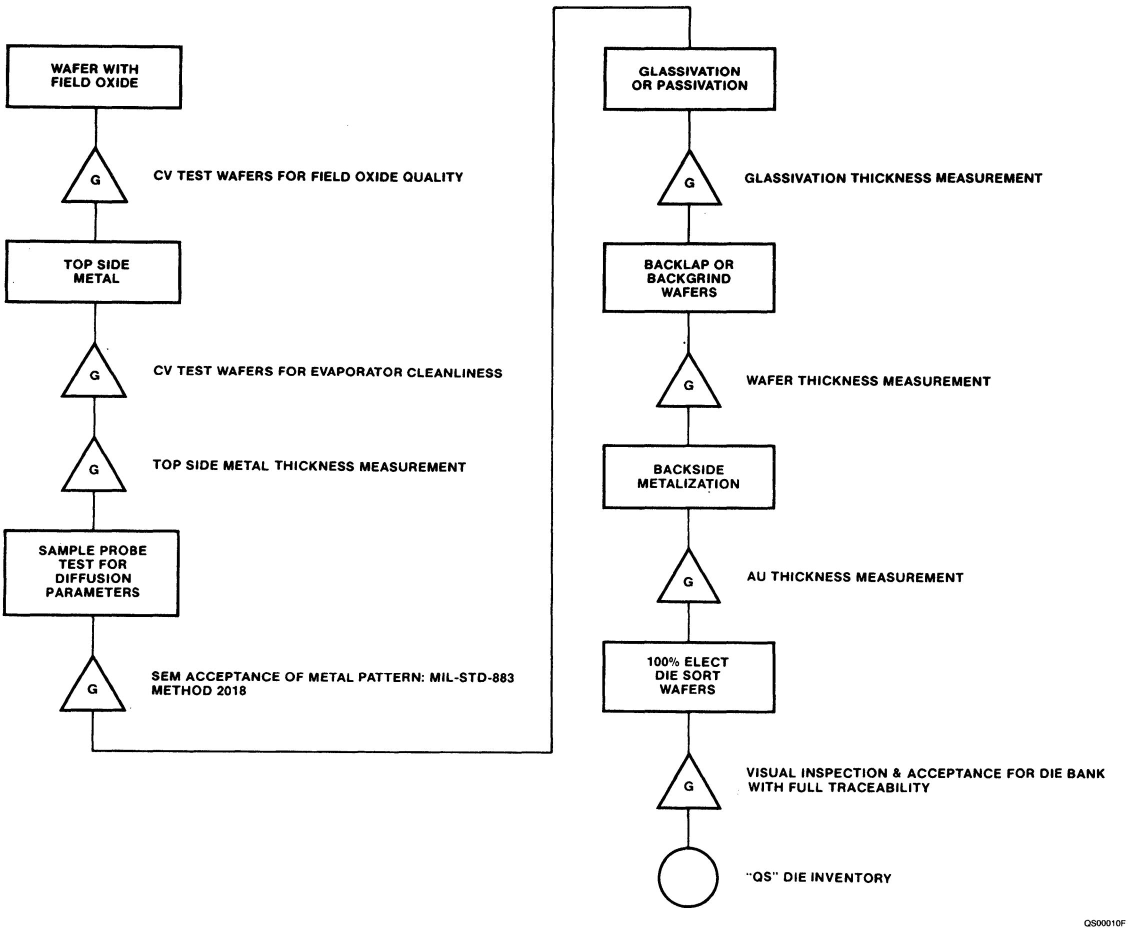
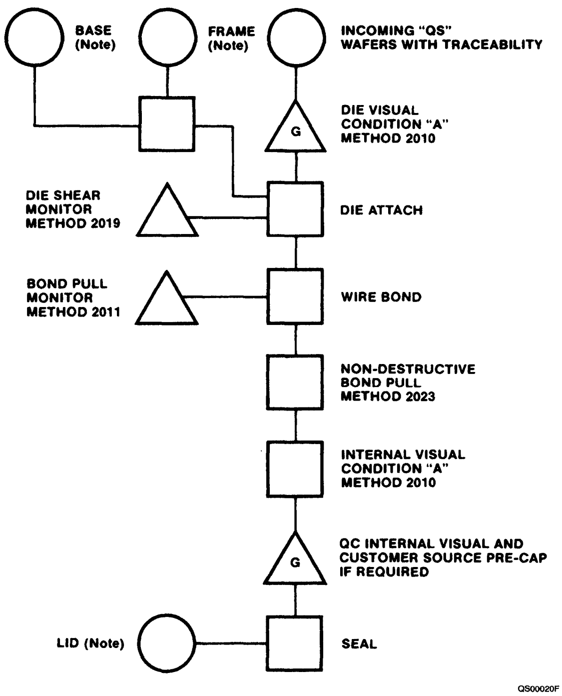
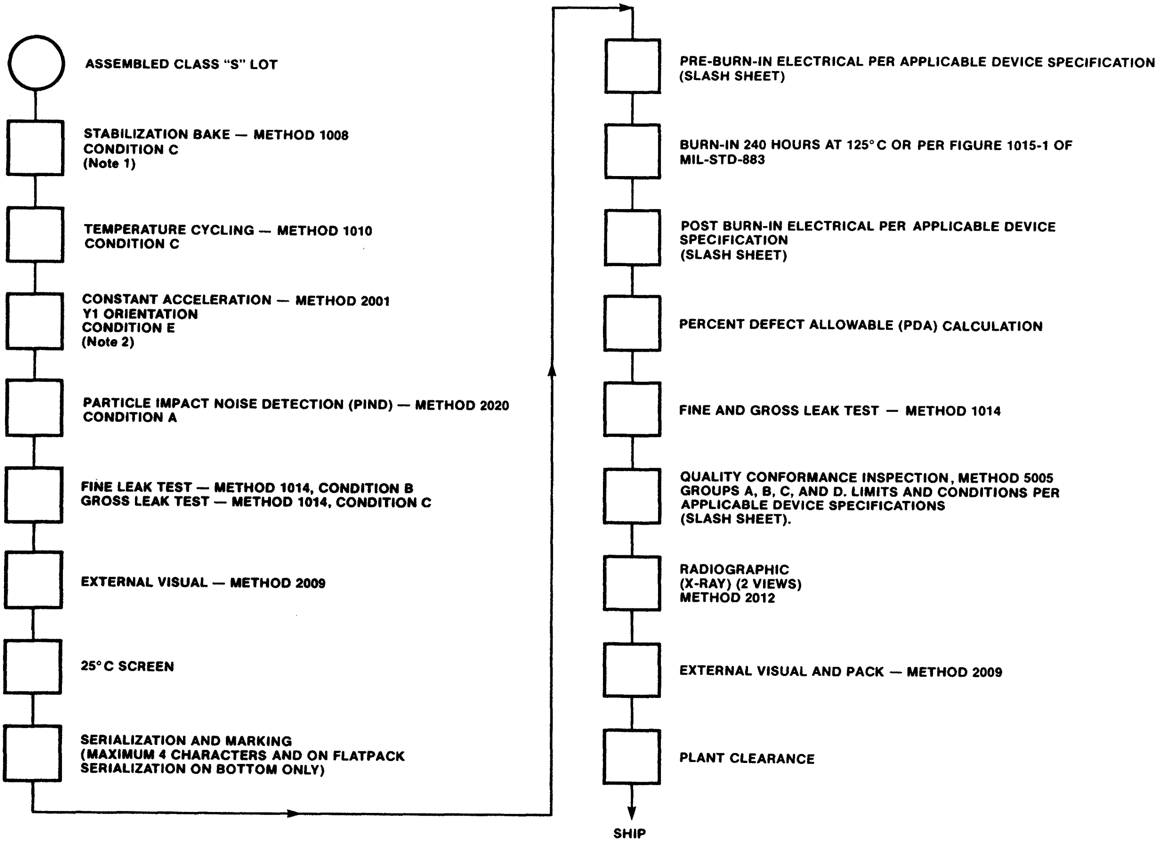


Figure 3B "QS" Assembly Flow



Note
Piece part traceability maintained when desired.

Figure 3C "QS" Environmental and Finish Processing (Typical) **"QS" Test, Burn-In and Final Acceptance (Typical)**



QS00031F

Notes

1. Defines minimum time and temperature, greater temperature and/or longer time used for some packages types.
2. Or lower G levels as allowed for larger packages per MIL-STD-883, Method 5004.

FAIRCHILD

A Schlumberger Company

μA105QB Voltage Regulator

MIL-STD-883
November 1985 – Rev 0[5]

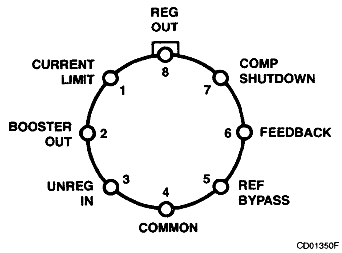
Aerospace and Defense Data Sheet
Linear Products

Description

The μA105QB is a monolithic positive voltage regulator constructed using the Fairchild Planar Epitaxial process. Applications for this device include both linear and switching regulator circuits with output voltages greater than 4.5 V. This device will not oscillate when confronted with varying resistive and reactive loads and will start reliably regardless of the load within the ratings of the circuit. It also features fast response to both load and line transients.[6]

- **Low Standby Current Drain**
- **Adjustable Output Voltage From 4.5 To 40 V**
- **High Output Current Exceeding 10 A With External Components**
- **Load Regulation Better Than 0.1%, Full Load With Current-Limiting**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA105HMQB	GC	A-1 8-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[12]	
Can	330 mW
Input Voltage	50 V
Input/Output Voltage Differential	40 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} and $V_I - V_O$ are guaranteed by the FBSV test.
8. V_{OR} is guaranteed by the FBSV and the $V_{R\ LOAD}$ tests.
9. The line and load regulation specifications are given for the condition of constant chip temperature. Temperature drift effects must be taken into account separately for high dissipation conditions.
10. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be approximately equal to the composite current gain of the added transistor.
11. With no external pass transistor.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.

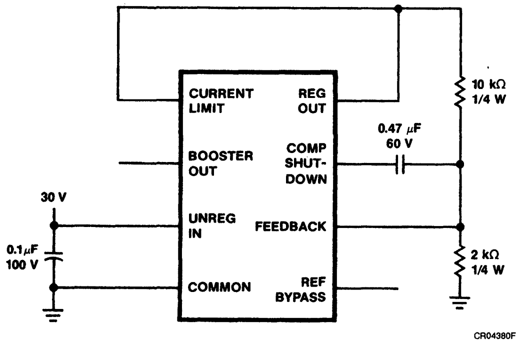
μA105QB

Electrical Characteristics These specifications apply for input and output voltages within the ranges given and for a divider impedance seen by the feedback terminal of 2 kΩ unless otherwise specified.

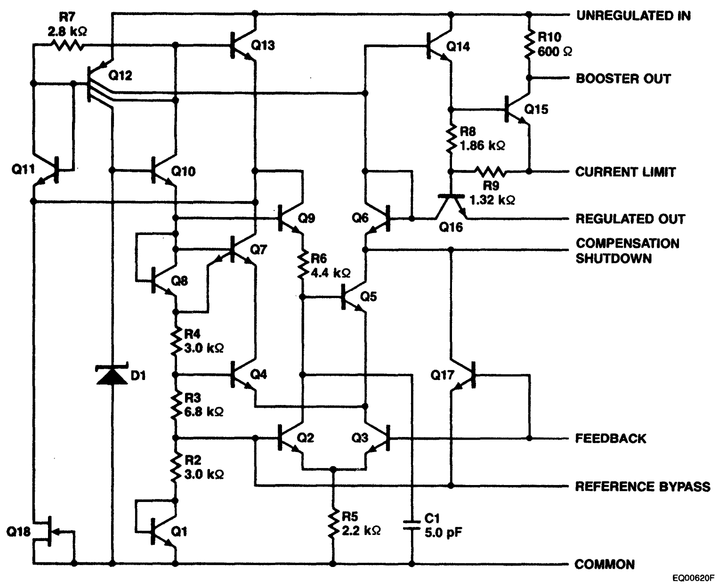
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
FBSV	Feedback Sense Voltage	$V_I = 50$ V, $V_O = 20$ V	1.63	1.81	V	1	1
		$V_I = 8.5$ V, $V_O = 4.5$ V	1.63	1.81	V	1	1
V_{IR}	Input Voltage Range[7]		8.5	50	V	1	1
V_{OR}	Output Voltage Range[8]		4.5	40	V	1	1
$V_I - V_O$	Input/Output Voltage Differential[7]		3.0	30	V	1	1
$V_{R\ LINE}$	Line Regulation[9]	$9.5\ V \leq V_I \leq 11.5\ V$, $V_O = 4.5$ V		0.03	%/V	1	1
		$25\ V \leq V_I \leq 50\ V$, $V_O = 20$ V		0.03	%/V	1	1
		$46\ V \leq V_I \leq 50\ V$, $V_O = 40$ V		0.03	%/V	1	1
		$8.5\ V \leq V_I \leq 9.5\ V$, $V_O = 4.5$ V		0.06	%/V	1	1
$V_{R\ LOAD}$	Load Regulation[9,10]	$V_I = 50$ V, $V_O = 40$ V, $0\ mA \leq I_L \leq 12\ mA$, $R_{SC} = 10\ \Omega$		0.05	%	1	1
				0.1	%	1	2,3
T_S	Temperature Stability of FBSV	$25°C \leq T_A \leq 125°C$		1.0	%	4	2
		$-55°C \leq T_A \leq 25°C$		1.0	%	4	3
I_{SCD}	Standby Current Drain	$V_I = 50$ V, $V_O = 20$ V		2.0	mA	1	1
V_{CLS}	Current Limit Sense Voltage[11]	$9.0\ V \leq V_I \leq 40\ V$, $V_O = 0$ V, $R_{SC} = 10\ \Omega$	225	375	mV	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 10 kHz		0.02	%/V	4	4
S	Long Term Stability of FBSV			1.0	%/1000 hrs	4	1

13

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

μA109QB
5 Volt Regulator

MIL-STD-883
November 1985 – Rev 0[5]

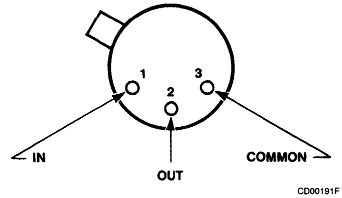
Aerospace and Defense Data Sheet
Linear Products

Description

The μA109QB is a complete 5 volt regulator constructed using the Fairchild Planar Expitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. It is intended for use as a local regulator, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, this regulator can provide over 1 A output current. The μA109QB is intended primarily for use with TTL and DTL logic and is completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 V regulator, this device can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.[6]

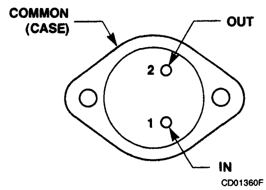
- **Output Current In Excess Of 1 A**
- **Specified To Match Worst Case TTL And DTL Requirements**
- **No Internal Components**
- **Internal Thermal Overload Protection**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Connection Diagram 2-Lead TO-3 Can (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA109HMQB	XC	3-Lead Can
μA109KMQB	YC	2-Lead Can

JAN Product Available

10701	BXC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can Without Heat Sink HMQB[11]	0.18 W
Can With Heat Sink HMQB[12]	0.5 W
Can Without Heat Sink KMQB[13]	0.71 W
Can With Heat Sink KMQB[14]	5.6 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W for HMQB and $P_D \leq 15$ W for KMQB.
9. Device shall turn-on at $V_I \leq 9$ V and shall remain on when the input is returned to 10 V.
10. Internally limited.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
13. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
14. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

μA109HQB, μA109KQB
Electrical Characteristics $C_I = 0.33 \mu F$, $C_O = 0.1\ \mu F$, unless otherwise specified.[7]

Symbol	Characteristic	Condition HMQB	Condition KMQB	Min	Max	Unit	Note	Subgrp
V_O	Output Voltage	$V_I = 10$ V		4.7	5.3	V	1	1
		$I_L = 350$ mA	$I_L = 500$ mA					
V_O	Output Voltage[8]	$8.0\ V \leq V_I \leq 20$ V, $5.0\ mA \leq I_L \leq I_{Max}$		4.6	5.4	V	1	1,2,3
		$I_{Max} = 350$ mA	$I_{Max} = 1.0$ A					
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$V_I = 7.0$ V, $I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			2.0	mV/°C	4	2
		$V_I = 7.0$ V, $I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			2.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$7.0\ V \leq V_I \leq 25$ V			50	mV	1	1
		$I_L = 200$ mA	$I_L = 500$ mA					
$V_{R\ LOAD}$	Load Regulation	$V_I = 10$ V, $5.0\ mA \leq I_L \leq I_{Max}$			100	mV	1	1
		$I_{Max} = 500$ mA	$I_{Max} = 1.0$ A					
I_{SCD}	Standby Current Drain	$7.0\ V \leq V_I \leq 25$ V			10	mA	1	1
		$I_L = 350$ mA	$I_L = 500$ mA					
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Current)	$8.0\ V \leq V_I \leq 25$ V			0.8	mA	1	1,2,3
		$I_L = 200$ mA	$I_L = 500$ mA					
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$V_I = 10$ V, $5.0\ mA \leq I_L \leq I_{Max}$			0.5	mA	1	1,2,3
		$I_{Max} = 350$ mA	$I_{Max} = 1.0$ A					
I_{OS}	Output Short Circuit Current	$V_I = 35$ V	HMQB		2.0	A	1	1
			KMQB		2.8	A	1	1
V_{START}	Voltage Start[9]			4.7		V	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 10$ V, $f = 2400$ Hz		60		dB	1	4
		$I_L = 125$ mA	$I_L = 350$ mA					
N_O	Noise	$V_I = 10$ V, $10\ Hz \leq f \leq 10$ kHz			125	μV_{rms}	4	9
		$I_L = 50$ mA	$I_L = 100$ mA					
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 10$ V ($V_{pulse} = 3.0$ V)			15	mV/V	4	9
		$I_L = 5.0$ mA	$I_L = 5.0$ mA					
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 10$ V			2.0	mV/mA	4	9
		$I_L = 50$ mA, $\Delta I_L = 200$ mA	$I_L = 100$ mA, $\Delta I_L = 400$ mA					
S	Long Term Stability of V_O	$V_I = 10$ V			0.5	%/1000 hrs	4	9

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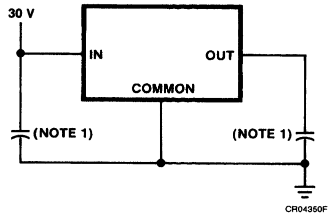
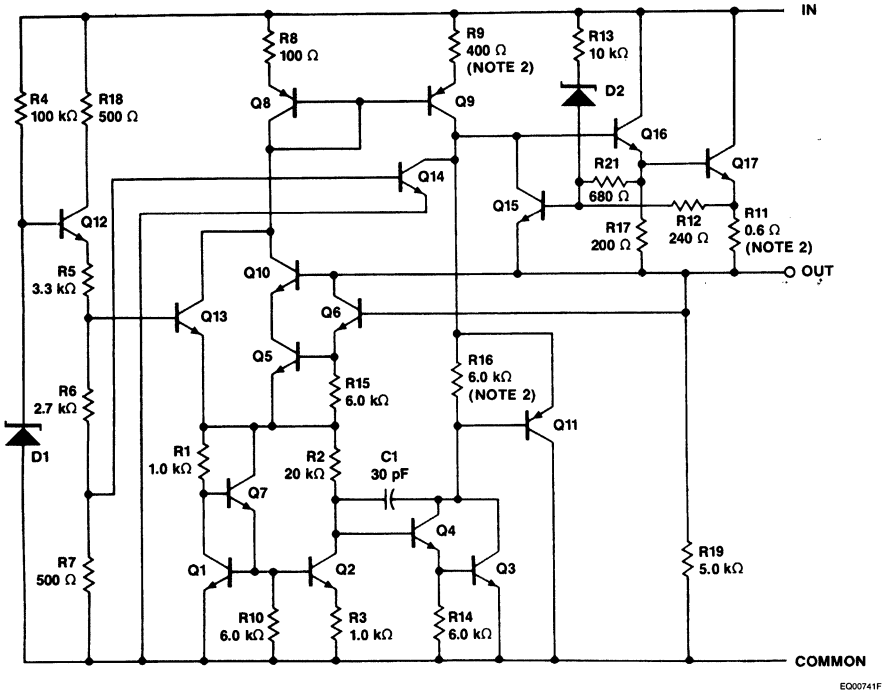
Primary Burn-In Circuit
(38510/10701 may be used by FSC as an alternate.)



Equivalent Circuit



Note
1. Capacitor value necessary to suppress oscillations.
2. μA109HMQB: R9 = 400 Ω, R11 = 0.6 Ω, R16 = 6 kΩ.
   μA109KMQB: R9 = 100 Ω, R11 = 0.3 Ω, R16 = 2 kΩ.

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MIL-STD-883
November 1985 – Rev 0[5]

μA117HQB
3-Terminal Positive Adjustable Regulator

Aerospace and Defense Data Sheet
Linear Products

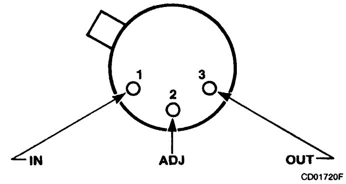
Description

The μA117HQB is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 0.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially blow-out proof.

The μA117HQB serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator; or by connecting a fixed resistor between the adjustment and output, the μA117HQB can be used as a precision current regulator.[6]

- **Output Current In Excess Of 0.5 A**
- **Output Adjustable Between 1.2 V And 37 V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting Constant Temperature**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation For High Voltage Applications**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA117HMQB	XC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
Input/Output Differential Voltage	40 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.

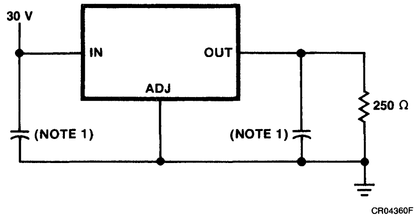
μA117HQB
Electrical Characteristics I_L = 50 mA, unless otherwise specified.[7]

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]	V_I = 4.25 V, I_L = 5.0 mA	1.2	1.3	V	4	1
		V_I = 4.25 V, I_L = 500 mA	1.2	1.3	V	1	1,2,3
		V_I = 41.3 V, I_L = 5.0 mA	1.2	1.3	V	1	1,2,3
		V_I = 41.3 V, I_L = 50 mA	1.2	1.3	V	1	1
$V_{R\ LINE}$	Line Regulation	4.25 V ≤ V_I ≤ 41.3 V		9.0	mV	1	1
				18.5	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	V_I = 6.25 V, V_O = V_{REF}, 5.0 mA ≤ I_L ≤ 500 mA		12	mV	1	1
				12	mV	1	2,3
I_{adj}	Adjustment-Lead Current	V_I = 6.25		100	μA	1	1,2,3
ΔI_{adj} (LINE)	Adjustment-Lead Current Change (vs Line Voltage)	3.75 V ≤ V_I ≤ 41.3 V, I_L = 150 mA		5.0	μA	1	1,2,3
ΔI_{adj} (LOAD)	Adjustment-Lead Current Change (vs Load Current)[8]	10 mA ≤ I_L ≤ 500 mA		5.0	μA	1	1,2,3
I_{OS}	Output Short Circuit Current	V_I = 4.25 V	0.5	1.8	A	4	1
		V_I = 40 V	0.05	0.5	A	4	1
V_{REF}	Reference Voltage[8]	4.25 V ≤ V_I ≤ 41.3 V, 10 mA ≤ I_L ≤ 500 mA	1.2	1.3	V	1	1,2,3
I_Q	Minimum Load Current to Maintain Regulation	V_I = 41.3 V		5.0	mA	1	1,2,3
		4.25 V ≤ V_I ≤ 14.25 V	0.5	3.0	mA	4	1
I_{Max}	Maximum Output Current[8]	V_I = 12 V		600	mA	1	1,2,3
		V_I = 41.3 V	50		mA	1	1
V_{RTH}	Thermal Regulation	V_I = 19.5 V, I_L = 550 mA, 0.5 ms ≤ t ≤ 20 ms	−40	40	mV	1	1
V_{START}	Voltage Start	V_I = 4.3 V	1.2	1.3	V	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I - V_O$ = 5.0 V, I_L = 125 mA, e_i = 1.0 V_{rms}, f = 2400 Hz	65		dB	1	1,2,3
N_O	Noise	I_L = 50 mA, 10 Hz ≤ f ≤ 10 kHz		120	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I - V_O$ = 5.0 V, I_L = 10 mA, ΔV_I = 3.0 V		6.0	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I - V_O$ = 5.0 V, I_L = 50 mA, ΔI_L = 200 mA		0.6	mV/mA	4	9
S	Long Term Stability of V_O			1.0	%/1000 hrs	4	1

13

Primary Burn-In Circuit

(38510/11703 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit

Refer to the Fairchild Linear Data Book Commercial Section

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MIL-STD-883

November 1985 – Rev 0[5]

μA117KQB 3-Terminal Positive Adjustable Regulator

Aerospace and Defense Data Sheet

Linear Products

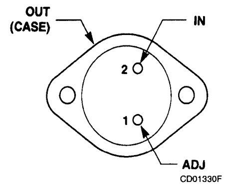
Description

The μA117KQB is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially blow-out proof.

The μA117KQB serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator; or by connecting a fixed resistor between the adjustment and output, the μA117KQB can be used as a precision current regulator.[6]

- **Output Current In Excess Of 1.5 A**
- **Output Adjustable Between 1.2 V And 37 V**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting Constant Temperature**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation For High Voltage Applications**

Connection Diagram 2-Lead TO-3 Can (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA117KMQB	YC	2-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input/Output Differential Voltage	40 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 20$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA117KQB
Electrical Characteristics I_L = 500 mA, unless otherwise specified.[7]

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]	V_I = 4.25 V, I_L = 5.0 mA	1.2	1.3	V	4	1
		V_I = 4.25 V, I_L = 1.5 A	1.2	1.3	V	1	1,2,3
		V_I = 41.3 V, I_L = 5.0 mA	1.2	1.3	V	1	1,2,3
		V_I = 41.3 V, I_L = 250 mA	1.2	1.3	V	1	1
$V_{R\ LINE}$	Line Regulation	4.25 V ≤ V_I ≤ 41.3 V		9.2	mV	1	1
				18.5	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	V_I = 6.25 V, V_O = V_{REF}, 10 mA ≤ I_L ≤ 1.5 A		3.8	mV	1	1
				12.5	mV	1	2,3
I_{adj}	Adjustment-Lead Current	V_I = 6.25 V		100	μA	1	1,2,3
ΔI_{adj} (LINE)	Adjustment-Lead Current Change (vs Line Voltage)	3.75 V ≤ V_I ≤ 41.3 V, I_L = 150 mA		5.0	μA	1	1,2,3
ΔI_{adj} (LOAD)	Adjustment-Lead Current Change (vs Load Current)[8]	V_I = 6.25 V, 10 mA ≤ I_L ≤ 1.5 A		5.0	μA	1	1,2,3
I_{OS}	Output Short Circuit Current	V_I = 4.25 V	1.5	3.5	A	4	1
		V_I = 40 V	0.18	1.0	A	4	1
V_{REF}	Reference Voltage[8]	4.25 V ≤ V_I ≤ 41.3 V, 10 mA ≤ I_L ≤ 1.5 A	1.2	1.3	V	1	1,2,3
I_Q	Minimum Load Current to Maintain Regulation	V_I = 41.3 V		5.0	mA	1	1,2,3
		4.25 V ≤ V_I ≤ 14.25 V	0.5	3.0	mA	4	1
I_{Max}	Maximum Output Current[8]	V_I = 12 V		1.5	A	1	1,2,3
		V_I = 41.3 V	0.25		A	1	1
V_{RTH}	Thermal Regulation	V_I = 19.5 V, I_L = 1.2 A, 0.5 ms ≤ t ≤ 20 ms	−40	40	mV	1	1
V_{START}	Voltage Start	V_I = 4.3 V	1.2	1.3	V	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I - V_O$ = 5.0 V, I_L = 500 mA, e_i = 1.0 V_{rms}, f = 2400 Hz	65		dB	1	1,2,3
N_O	Noise	I_L = 100 mA, 10 Hz ≤ f ≤ 10 kH z		120	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I - V_O$ = 5.0 V, I_L = 10 mA, ΔV_I = 3.0 V		6.0	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I - V_O$ = 5.0 V, I_L = 100 mA, ΔI_L = 400 mA		0.3	mV/mA	4	9
S	Long Term Stability of V_O			1.0	%/1000 hrs	4	1

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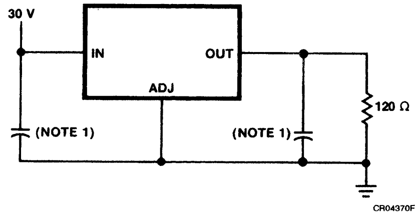
Primary Burn-In Circuit
(38510/11704 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit
Refer to the Fairchild Linear Data Book Commercial Section

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MIL-STD-883

November 1985 – Rev 0[1]

μA138QB 5-Amp Positive Adjustable Regulator

Aerospace and Defense Data Sheet

Linear Products

Description

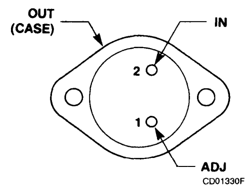
The μA138QB is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 5.0 A over a 1.2 V to 32 V output range. It is exceptionally easy to use and requires only two resistors to set the output voltage. A unique feature of the μA138QB is time dependent current-limiting. The current-limit circuitry allows peak currents of up to 12 A to be drawn from the regulator for short periods of time. This allows it to be used with heavy transient loads and also speeds start-up under full-load conditions. Under sustained loading conditions, the current-limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe-area protection for the power transistor. Overload protection remains functional even if the adjustment lead is accidentally disconnected.[2]

- **High Peak Output Current**
- **High Output Current**
- **Output Adjustable Between 1.2 V And 32 V**
- **Low Load Regulation**
- **Low Line Regulation**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation For High Voltage Applications**

Notes

1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA138KMQB	YC	2-Lead Can

13

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MIL-STD-883
November 1985 – Rev 0[1]

μA150QB 3-Amp Positive Adjustable Regulator

Aerospace and Defense Data Sheet
Linear Products

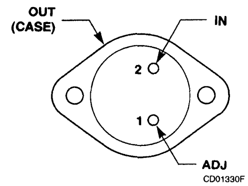
Description

The μA150QB is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 3.0 A over a 1.2 V to 33 V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. A unique feature of the μA150QB is time dependent current-limiting. The current-limit circuitry allows peak currents of up to 6.0 A to be drawn from the regulator for short periods of time. This allows it to be used with heavy transient loads and also speeds start-up under full-load conditions. Under sustained loading conditions, the current-limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe-area protection for the power transistor. Overload protection remains functional even if the adjustment lead is accidentally disconnected.[2]

- **High Output Current**
- **Output Adjustable Between 1.2 V And 33 V**
- **Low Load Regulation**
- **Low Line Regulation**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**
- **Floating Operation For High Voltage Applications**

Notes
1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram 2-Lead TO-3 Can (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA150KMQB	YC	2-Lead Can

FAIRCHILD

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MIL-STD-883
July 1986—Rev 0[1]

μA431QB Adjustable Precision Shunt Regulator

Aerospace and Defense Data Sheet
Linear Products

Description

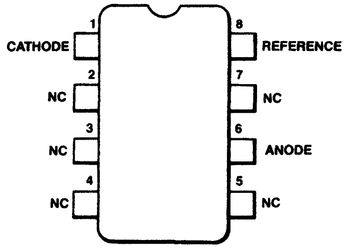
The μA431QB is a 3-lead adjustable shunt regulator with guaranteed temperature stability over the entire temperature range. The output voltage may be set at any level greater than 2.5 V (V_{REF}) up to 36 V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.[2]

- **Typical Temperature Coefficient 50 ppm/°C**
- **Temperature Compensated For Operation Over The Full Temperature Range**
- **Programmable Output Voltage**
- **Fast Turn-On Response**
- **Low Output Noise**

Notes

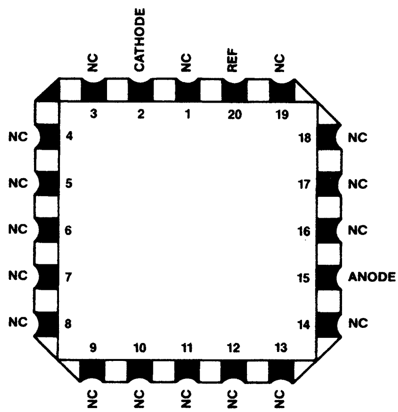
1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram 8-Lead DIP (Top View)



CD02220F

Connection Diagram 20-Terminal CCP (Top View)



CR05340F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA431RMQB	PA	D-4 8-Lead DIP
μA431LMQB	2C	C-2 20-Terminal CCP

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MIL-STD-883

July 1986—Rev 0[1]

μA494QB Pulse Width Modulated Control Circuit

Aerospace and Defense Data Sheet

Linear Products

Description

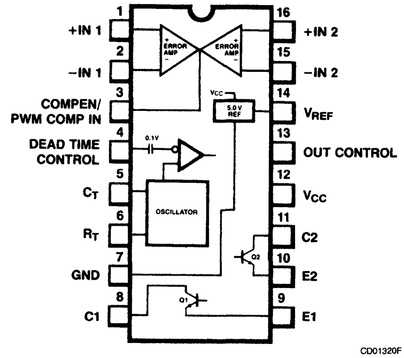
The μA494QB is a monolithic integrated circuit which includes all the necessary building blocks for the design of pulse width modulated (PWM) switching power supplies, including push-pull, bridge, and series configurations. The device can operate at switching frequencies between 1.0 kHz and 300 kHz and output voltages up to 40 V.[2]

- **Uncommitted Output Transistors Capable Of 200 mA Source Or Sink**
- **On-Chip Error Amplifiers**
- **On-Chip 5.0 V Reference**
- **Internal Protection From Double Pulsing Of Outputs With Narrow Pulse Widths Or With Supply Voltages Below Specified Limits**
- **Dead Time Control Comparator**
- **Output Control Selects Single-Ended Or Push-Pull Operation**
- **Easily Synchronized (Slaved) To Other Circuits**

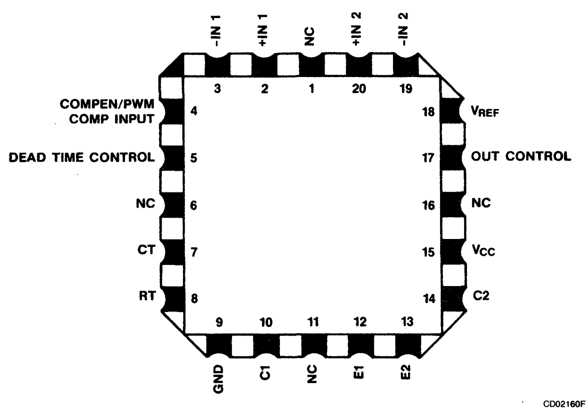
Notes

1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram 16-Lead DIP (Top View)



Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA494DMQB	EB	D-2 16-Lead DIP
μA494LMQB	2C	C-2 20-Terminal CCP

FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 2[5]

μA723QB Precision Voltage Regulator

Aerospace and Defense Data Sheet

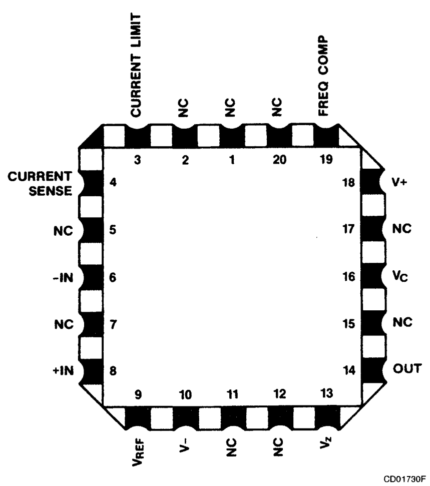
Linear Products

Description

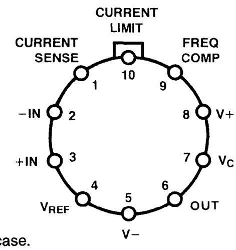
The μA723QB is a monolithic voltage regulator constructed using the Fairchild Planar Epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current-limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723QB is intended for use with positive or negative supplies as a series, shunt, switching, or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems, and other power supplies for digital and linear circuits.[6]

- **Positive Or Negative Supply Operation**
- **Series, Shunt, Switching, Or Floating Operation**
- **Low Line And Load Regulation**
- **Output Voltage Adjustable From 2 V To 37 V**
- **Output Current To 150 mA Without External Pass Transistor**

Connection Diagram 20-Terminal CCP (Top View)

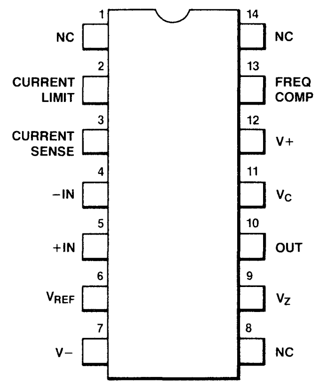


Connection Diagram 10-Lead Can (Top View)



Lead 5 connected to case.

Connection Diagram 14-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA723DMQB	CA	D-1 14-Lead DIP
μA723HMQB	IC	A-2 10-Lead Can
μA723LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10201	BCA	D-1 14-Lead DIP
10201	BCB	D-1 14-Lead DIP
10201	BIA	A-2 10-Lead Can
10201	BIC	A-2 10-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
Can	350 mW
DIP and CCP	400 mW
Pulse Voltage from V+ to V–, (50 ms)	50 V
Continuous Voltage from V+ to V–	40 V
Input/Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V–	8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. The line and load regulation specifications are given for the condition of constant chip temperature. Temperature drift effects must be taken into account separately for high dissipation conditions.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Can and 120°C/W for the DIP and CCP.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at –55°C
4. Dynamic tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA723QB

Electrical Characteristics $V_I = V+ = V_C \leq 12$ V, $V- = 0$ V, $V_O = 5.0$ V, $I_L = 1.0$ mA, $R_{SC} = 0\ \Omega$, C1 = 100 pF, $C_{REF} = 0\ \mu F$, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{REF}	Reference Voltage			6.95	7.35	V	1	1,2,3
ΔV_{REF} (LOAD)	Reference Voltage Change With Load	$0\ mA \leq I_{REF} \leq 5.0\ mA$			20	mV	1	1
V_{IR}	Input Voltage Range			9.5	40	V	1	1
V_{OR}	Output Voltage Range			2.0	37	V	1	1
$V_I - V_O$	Input/Output Voltage Diff.			3.0	38	V	1	1
V_Z	Zener Voltage	$I_Z = 1.0$ mA		5.8	7.2	V	1	1
$V_{R\ LINE}$	Line Regulation[7]	$12\ V \leq V_I \leq 15\ V$			0.1	$\%V_O$	1	1
		$12\ V \leq V_I \leq 40\ V$			0.2	$\%V_O$	1	1
		$12\ V \leq V_I \leq 15\ V$			0.3	$\%V_O$	1	2,3
$V_{R\ LOAD}$	Load Regulation[7]	$1.0\ mA \leq I_L \leq 50\ mA$			0.15	$\%V_O$	1	1
					0.6	$\%V_O$	1	2,3
$T_C\ V_O$	Average Temp. Coefficient of Output Voltage	$25°C \leq T_A \leq 125°C$		-0.010	+0.010	%/°C	4	2
		$-55°C \leq T_A \leq 25°C$		-0.015	+0.015	%/°C	4	3
I_{SCD}	Standby Current Drain	$V_I = 30$ V, $I_L = 0$ mA			3.5	mA	1	1
					4.0	mA	4	2
					2.4	mA	4	3
I_{OS}	Output Short Circuit Current	$V_O = 0$ V, $R_{SC} = 10\ \Omega$		45	85	mA	4	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	f = 10 kHz, $C_{REF} = 0\ \mu F$		64		dB	3	4
		f = 10 kHz, $C_{REF} = 5.0\ \mu F$		76		dB	3	4
N_O	Noise	$100\ Hz \leq f \leq 10\ kHz$	$C_{REF} = 0\ \mu F$		120	μV_{rms}	3	4
			$C_{REF} = 5.0\ \mu F$		7.0	μV_{rms}	3	4
$\Delta V_O/\Delta V_I$	Line Transient Response	$\Delta V_I = 3.0$ V			10	mV/V	3	4
$\Delta V_O/\Delta I_L$	Load Transient Response	$I_L = 40$ mA, $\Delta I_L = 10$ mA		-1.5		mV/mA	3	4

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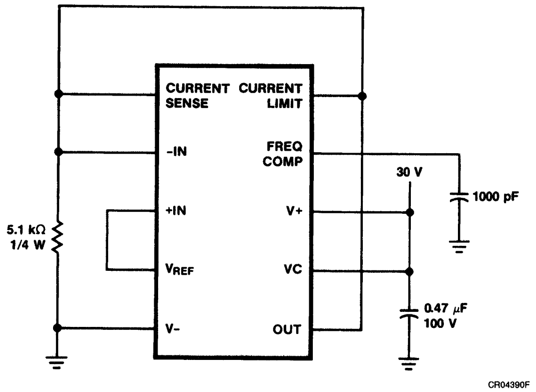
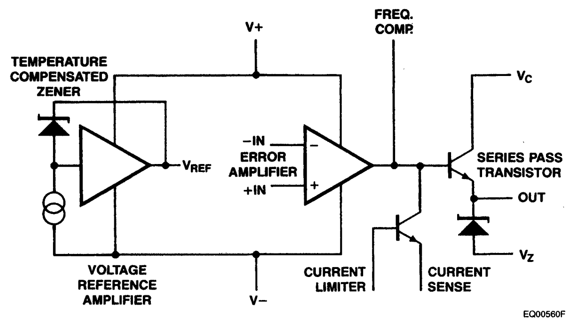
Primary Burn-In Circuit

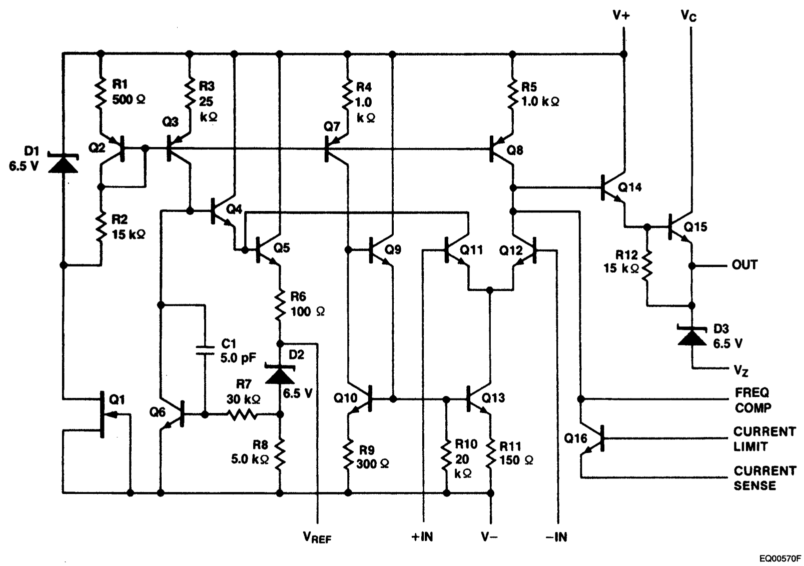
(38510/10201 may be used by FSC as an alternate)



Block Diagram



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA78M05QB 3-Terminal Positive Voltage Regulator

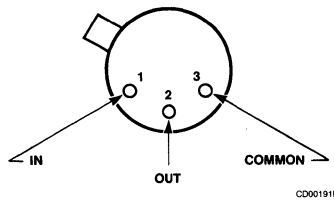
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M05QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

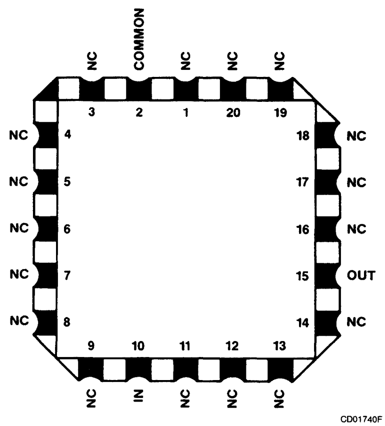
- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Lead 3 connected to case.

Connection Diagram
20-Terminal CCP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M05HMQB	XC	3-Lead Can
μA78M05LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10702	BXC	3-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
CCP Without Heat Sink[12]	0.4 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

μA78M05QB

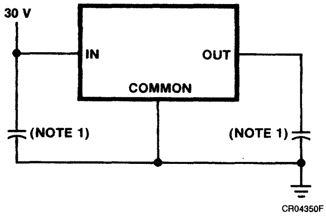
Electrical Characteristics $V_I = 10$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			4.8	5.2	V	1	1
		5.0 mA ≤ I_L ≤ 350 mA	$V_I = 8.0$ V	4.7	5.3	V	1	1,2,3
			$V_I = 20$ V	4.7	5.3	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			1.5	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			2.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	7.0 V ≤ V_I ≤ 25 V, $I_L = 200$ mA			50	mV	1	1
		8.0 V ≤ V_I ≤ 25 V, $I_L = 200$ mA			50	mV	1	2,3
		8.0 V ≤ V_I ≤ 20 V, $I_L = 200$ mA			25	mV	1	1
					40	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 500 mA			50	mV	1	1
					100	mV	1	2,3
		5.0 mA ≤ I_L ≤ 200 mA			25	mV	1	1
					50	mV	1	2,3
I_{SCD}	Standby Current Drain				7.0	mA	1	1,2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	8.0 V ≤ V_I ≤ 25 V, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 350 mA			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 12$ V		0.5	2.0	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 10$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		62		dB	1	4
N_O	Noise	$V_I = 10$ V, $I_L = 50$ mA, 10 Hz ≤ f ≤ 10 kHz			125	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 10$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 10$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

13

Primary Burn-In Circuit

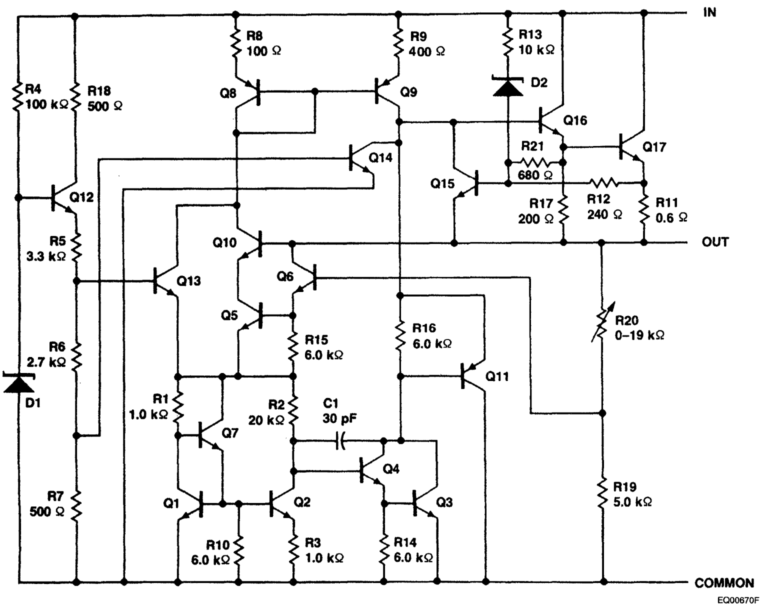
(38510/10702 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA78M06QB 3-Terminal Positive Voltage Regulator

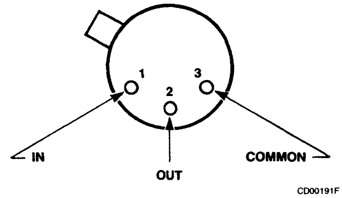
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M06QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Lead 3 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M06HMQB	XC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

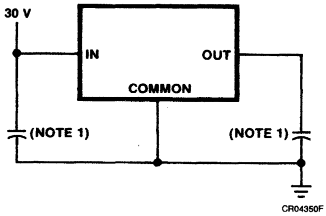
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.

μA78M06QB

Electrical Characteristics $V_I = 11$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

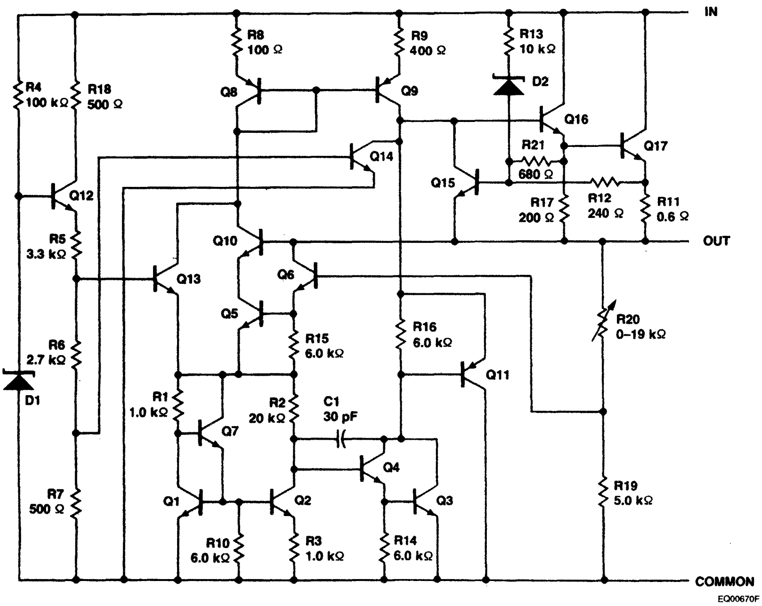
Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			5.75	6.25	V	1	1
		$5.0\ mA \leq I_L \leq 350\ mA$	$V_I = 9.0$ V	5.7	6.3	V	1	1,2,3
			$V_I = 21$ V	5.7	6.3	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			1.5	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			2.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$8.0\ V \leq V_I \leq 25\ V$, $I_L = 200$ mA			60	mV	1	1
		$9.0\ V \leq V_I \leq 20\ V$, $I_L = 200$ mA			30	mV	1	1
$V_{R\ LOAD}$	Load Regulation	$5.0\ mA \leq I_L \leq 500\ mA$			60	mV	1	1
		$5.0\ mA \leq I_L \leq 200\ mA$			30	mV	1	1
I_{SCD}	Standby Current Drain				7.0	mA	1	1
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$9.0\ V \leq V_I \leq 25\ V$, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0\ mA \leq I_L \leq 350\ mA$			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1
I_{OL}	Overload Current	$V_I = 13$ V		0.5	2.0	A	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 11$ V, $I_L = 125$ mA, $e_i = 1.0\ V_{rms}$, $f = 2400$ Hz		59		dB	1	4
N_O	Noise	$V_I = 11$ V, $I_L = 50$ mA, $10\ Hz \leq f \leq 10\ kHz$			125	μV_{rms}	4	9

Primary Burn-In Circuit



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



FAIRCHILD

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MIL-STD-883
July 1986—Rev 2[5]

μA78M08QB 3-Terminal Positive Voltage Regulator

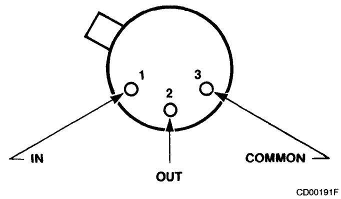
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M08QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Lead 3 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M08HMQB	XC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.

μA78M08QB

Electrical Characteristics $V_I = 14$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			7.7	8.3	V	1	1
		5.0 mA $\leqslant I_L \leqslant$ 350 mA	$V_I = 11.5$ V	7.6	8.4	V	1	1,2,3
			$V_I = 23$ V	7.6	8.4	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C $\leqslant T_A \leqslant$ 125°C			2.5	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C $\leqslant T_A \leqslant$ 25°C			2.5	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	10.5 V $\leqslant V_I \leqslant$ 25 V, $I_L = 200$ mA			60	mV	1	1
		11 V $\leqslant V_I \leqslant$ 20 V, $I_L = 200$ mA			30	mV	1	1
$V_{R\ LOAD}$	Load Regulation	5.0 mA $\leqslant I_L \leqslant$ 500 mA			80	mV	1	1
		5.0 mA $\leqslant I_L \leqslant$ 200 mA			40	mV	1	1
I_{SCD}	Standby Current Drain				7.0	mA	1	1
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	11.5 V $\leqslant V_I \leqslant$ 25 V, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA $\leqslant I_L \leqslant$ 350 mA			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1
I_{OL}	Overload Current	$V_I = 15$ V		0.5	2.0	A	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 14$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		56		dB	1	4
N_O	Noise	$V_I = 14$ V, $I_L = 50$ mA, 10 Hz $\leqslant$ f $\leqslant$ 10 kHz			175	μV_{rms}	4	9

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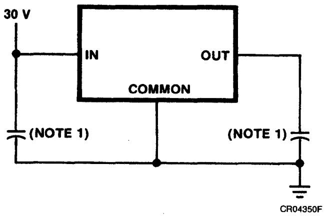
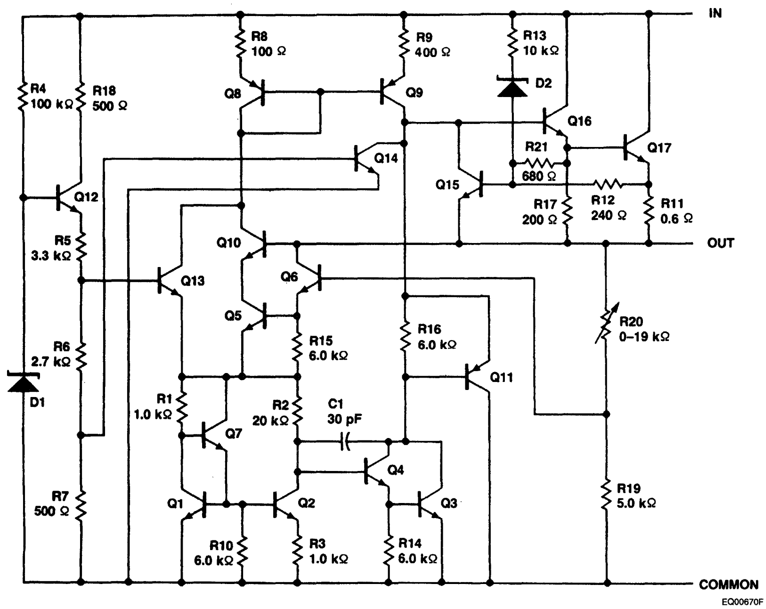
Primary Burn-In Circuit



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA78M12QB 3-Terminal Positive Voltage Regulator

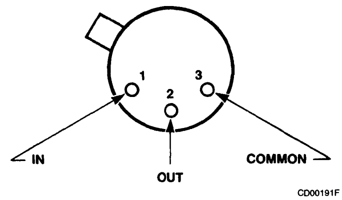
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M12QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

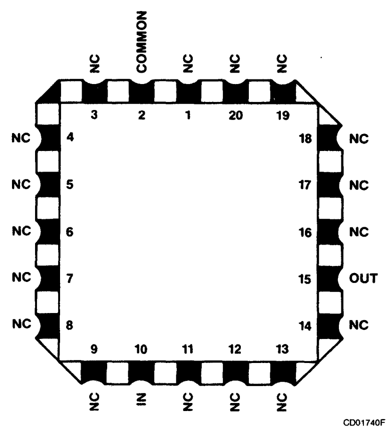
- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M12HMQB	XC	3-Lead Can
μA78M12LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10703	BXC	3-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
CCP Without Heat Sink[12]	0.4 W
Input Voltage	35 V

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA78M12QB
Electrical Characteristics $V_I = 19$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			11.5	12.5	V	1	1
		$5.0\text{ mA} \leq I_L \leq 350\text{ mA}$	$V_I = 15.5$ V	11.4	12.6	V	1	1,2,3
			$V_I = 27$ V	11.4	12.6	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			3.0	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			3.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$14.5\text{ V} \leq V_I \leq 30$ V, $I_L = 200$ mA			60	mV	1	1
		$15\text{ V} \leq V_I \leq 30$ V, $I_L = 200$ mA			120	mV	1	2,3
		$16\text{ V} \leq V_I \leq 25$ V, $I_L = 200$ mA			30	mV	1	1
					60	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	$5.0\text{ mA} \leq I_L \leq 500$ mA			120	mV	1	1
					240	mV	1	2,3
		$5.0\text{ mA} \leq I_L \leq 200$ mA			60	mV	1	1
					120	mV	1	2,3
I_{SCD}	Standby Current Drain				7.0	mA	1	1,2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$15\text{ V} \leq V_I \leq 30$ V, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0\text{ mA} \leq I_L \leq 350$ mA			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 17$ V		0.5	2.0	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 17$ V, $I_L = 125$ mA, $e_i = 1.0\ V_{rms}$, f = 2400 Hz		55		dB	1	4
N_O	Noise	$V_I = 17$ V, $I_L = 50$ mA, $10\text{ Hz} \leq f \leq 10$ kHz			125	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 17$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 17$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

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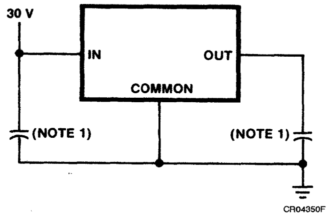
Primary Burn-In Circuit

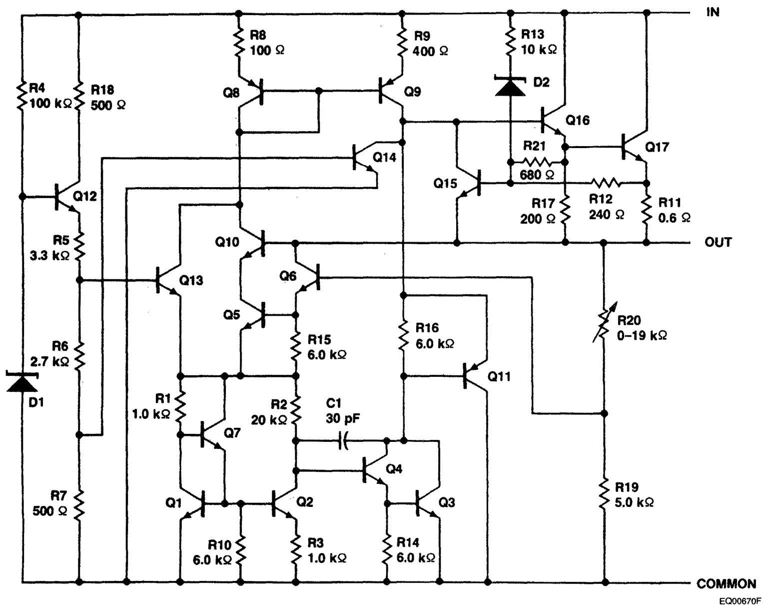
(38510/10703 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA78M15QB 3-Terminal Positive Voltage Regulator

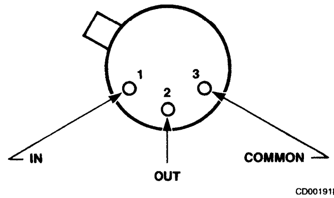
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M15QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

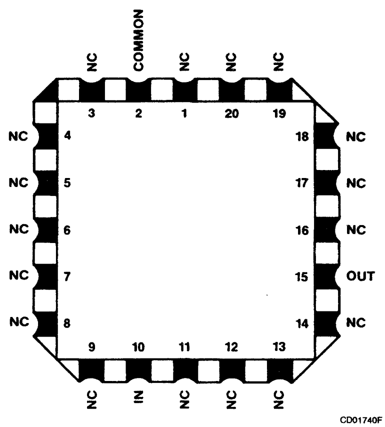
- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Lead 3 connected to case.

Connection Diagram
20-Terminal CCP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M15HMQB	XC	3-Lead Can
μA78M15LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10704	BXC	3-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
CCP Without Heat Sink[12]	0.4 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

μA78M15QB

Electrical Characteristics $V_I = 23$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			14.4	15.6	V	1	1
		$5.0\ mA \leq I_L \leq 350\ mA$	$V_I = 18.5$ V	14.25	15.75	V	1	1,2,3
			$V_I = 30$ V	14.25	15.75	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			3.75	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			3.75	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$17.5\ V \leq V_I \leq 30$ V, $I_L = 200$ mA			60	mV	1	1
		$18.5\ V \leq V_I \leq 30$ V, $I_L = 200$ mA			120	mV	1	2,3
		$20\ V \leq V_I \leq 30$ V, $I_L = 200$ mA			30	mV	1	1
					60	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	$5.0\ mA \leq I_L \leq 500$ mA			150	mV	1	1
					300	mV	1	2,3
		$5.0\ mA \leq I_L \leq 200$ mA			75	mV	1	1
					150	mV	1	2,3
I_{SCD}	Standby Current Drain				7.0	mA	1	1,2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$18.5\ V \leq V_I \leq 30$ V, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0\ mA \leq I_L \leq 350$ mA			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 22$ V		0.5	2.0	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 20$ V, $I_L = 125$ mA, $e_i = 1.0\ V_{rms}$, $f = 2400$ Hz		54		dB	1	4
N_O	Noise	$V_I = 20$ V, $I_L = 50$ mA, $10\ Hz \leq f \leq 10$ kHz			300	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 20$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 20$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

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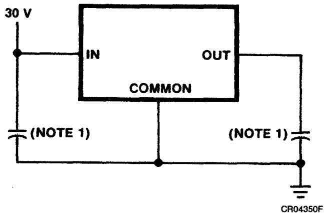
Primary Burn-In Circuit

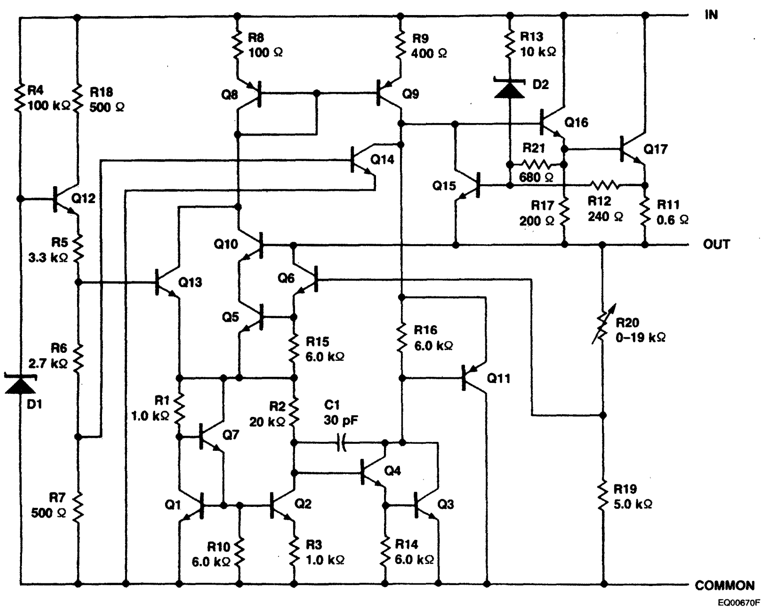
(38510/10704 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA78M24QB 3-Terminal Positive Voltage Regulator

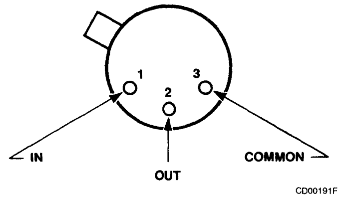
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78M24QB 3-Terminal Medium Current Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver in excess of 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 0.5 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78M24HMQB	XC	3-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.

μA78M24QB

Electrical Characteristics $V_I = 33$ V, $I_L = 350$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			23	25	V	1	1
		5.0 mA ≤ I_L ≤ 350 mA	$V_I = 28$ V	22.8	25.2	V	1	1,2,3
			$V_I = 38$ V	22.8	25.2	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			6.0	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			6.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	27 V ≤ V_I ≤ 38 V, $I_L = 200$ mA			60	mV	1	1
		28 V ≤ V_I ≤ 38 V, $I_L = 200$ mA			120	mV	1	2,3
		30 V ≤ V_I ≤ 36 V			30	mV	1	1
					60	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 500 mA			240	mV	1	1
					480	mV	1	2,3
		5.0 mA ≤ I_L ≤ 200 mA			120	mV	1	1
					240	mV	1	2,3
I_{SCD}	Standby Current Drain				7.0	mA	1	1,2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	28 V ≤ V_I ≤ 38 V, $I_L = 200$ mA			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 350 mA			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			1.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 31$ V		0.5	2.0	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 30$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		50		dB	1	4
N_O	Noise	$V_I = 30$ V, $I_L = 50$ mA, 10 Hz ≤ f ≤ 10 kHz			500	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 30$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 30$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

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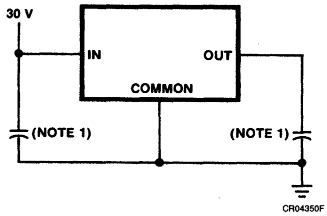
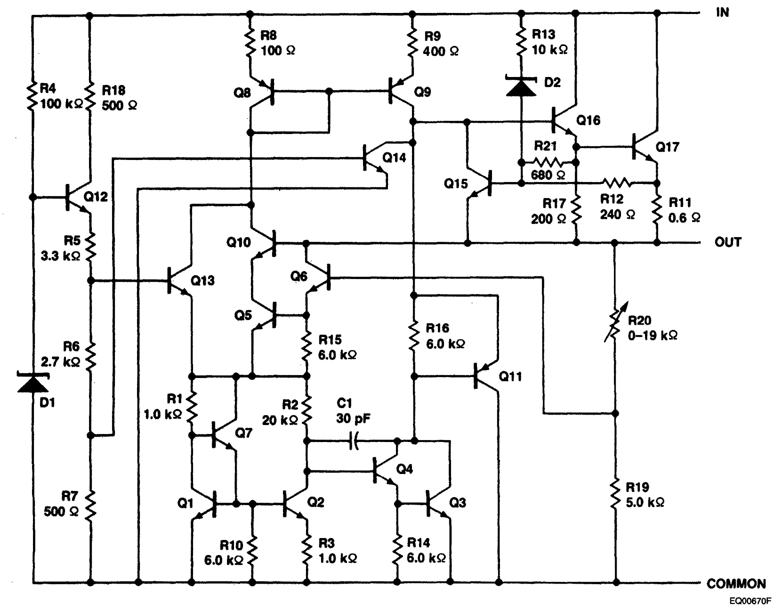
Primary Burn-In Circuit
(38510/10705 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA78S40QB Universal Switching Regulator Subsystem

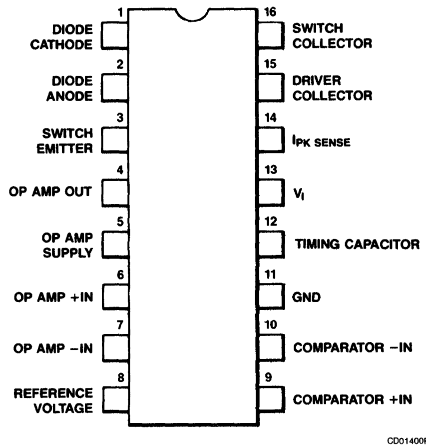
Aerospace and Defense Data Sheet
Linear Products

Description

The μA78S40QB is a monolithic regulator subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high current, high voltage output switch, a power diode and an uncommitted operational amplifier. The device can drive external NPN or PNP transistors when currents in excess of 1.5 A or voltages in excess of 40 V are required. The device can be used for step down, step up or inverting switching regulators as well as for series pass regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand alone, low part count switching system and works extremely well in battery operated systems.[6]

- **Step Up, Step Down Or Inverting Switching Regulators**
- **Output Adjustable From 1.25 To 40 V**
- **Peak Currents To 1.5 A Without External Transistors**
- **Operation From 2.5 To 40 V Input**
- **Low Standby Current Drain**
- **80 dB Excellent Line And Load Regulation**
- **High Gain, High Current, Independent Op Amp**
- **Pulse Width Modulation With No Double Pulsing**

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA78S40DMQB	EA	D-2 16-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Input Voltage from V+ to V−	40 V
Input Voltage from V+ (Op Amp) to V−	40 V
Input Voltage Range (Error Amplifier and Op Amp)	−0.3 to V+
Differential Input Voltage[9]	±30 V
Short Circuit Duration (Op Amp)	Indefinite
Current from V_{REF}	10 mA
Voltage from Switch Collectors to GND	40 V
Voltage from Switch Emitters to GND	40 V
Voltage from Switch Collectors to Emitter	40 V
Voltage from Power Diode to GND	40 V
Reverse Power Diode Voltage	40 V
Current through Power Switch	1.5 A
Current through Power Diode	1.5 A

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} is guaranteed by the CMR test.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
9. The differential input voltage shall not exceed the supply voltage.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

μA78S40QB
Electrical Characteristics V_I = 5.0 V, V+ (Op Amp) = 5.0 V, unless otherwise specified.

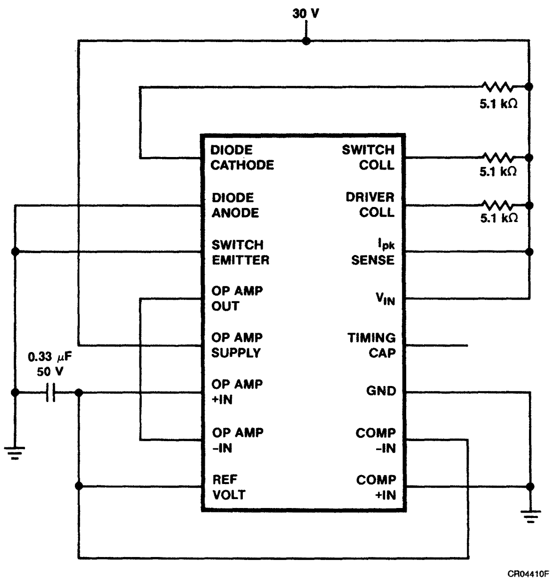
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
General Characteristics							
I_{CC}	Supply Current (Op Amp Disconnected)	V_I = 5.0 V		3.5	mA	1	1,2,3
		V_I = 40 V		5.0	mA	1	1,2,3
I_{CC}	Supply Current (Op Amp Connected)	V_I = 5.0 V		4.0	mA	1	1,2,3
		V_I = 40 V		5.5	mA	1	1,2,3
Reference Section							
V_{REF}	Reference Voltage	I_{REF} = 1.0 mA	1.18	1.31	V	1	1,2,3
$V_{R\ LINE}$	Reference Voltage Line Regulation	3.0 V $\leqslant V_I \leqslant$ 40 V, I_{REF} = 1.0 mA		0.2	mV/V	1	1
$V_{R\ LOAD}$	Reference Voltage Load Regulation	1.0 mA $\leqslant I_{REF} \leqslant$ 10 mA		0.5	mV/mA	1	1
Oscillator Section							
I_{CHG}	Charging Current	V_I = 5.0 V	20	50	μA	1	1
		V_I = 40 V	20	70	μA	1	1
I_{DIS}	Discharge Current	V_I = 5.0 V	150	250	μA	1	1
		V_I = 40 V	150	350	μA	1	1
Current Limit Section							
V_{CLS}	Current Limit Sense Voltage	I_{CT} = 200 μA	250	350	mV	1	1
Output Switch Section							
$V_{SAT}1$	Output Saturation Voltage 1	I_{sw} = 1.0 A		1.3	V	1	1,2,3
$V_{SAT}2$	Output Saturation Voltage 2	I_{sw} = 1.0 A		0.7	V	1	1,2,3
I_L	Output Leakage Current	V_O = 40 V		10	μA	1	1
Power Diode							
V_{FD}	Forward Voltage Drop	I_D = 1.0 A		1.5	V	1	1, 2,3
I_{LD}	Diode Leakage Current	V_D = 40 V		10	μA	1	1
Comparator							
V_{IO}	Input Offset Voltage	$V_{CM} = V_{REF}$		15	mV	1	1,2,3
I_{IB}	Input Bias Current	$V_{CM} = V_{REF}$		200	nA	1	1,2,3
I_{IO}	Input Offset Current	$V_{CM} = V_{REF}$		75	nA	4	1,2,3
V_{IR}	Input Voltage Range		0	V_I-2.0	V	1	1
PSRR	Power Supply Rejection Ratio	3.0 V $\leqslant V_I \leqslant$ 40 V		316	μV/V	4	1

μA78S40QB (Cont.)

Electrical Characteristics $V_I = 5.0$ V, V+ (Op Amp) = 5.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
Output Operational Amplifier							
V_{IO}	Input Offset Voltage	$V_{CM} = 2.5$ V		15	mV	1	1,2,3
I_{IB}	Input Bias Current	$V_{CM} = 2.5$ V		200	nA	1	1,2,3
I_{IO}	Input Offset Current	$V_{CM} = 2.5$ V		75	nA	1	1,2,3
A_{VS+}	Large Signal Voltage Gain +	$1.0\ V \leqslant V_O \leqslant 2.5\ V$, $R_L = 2.0\ k\Omega$ to GND	25		V/mV	1	1
A_{VS-}	Large Signal Voltage Gain −	$1.0\ V \leqslant V_O \leqslant 2.5\ V$, $R_L = 2.0\ k\Omega$ to V+ (Op Amp)	25		V/mV	1	1
CMR	Common Mode Rejection	$0\ V \leqslant V_{CM} \leqslant 3.0\ V$	76		dB	1	1
V_{IR}	Input Voltage Range[7]		0	3.0	V	1	1
PSRR	Power Supply Rejection Ratio	$3.0\ V \leqslant V+$ (Op Amp) $\leqslant 40$ V		158	μV/V	1	1
I_{SOU}	Output Source Current			−75	mA	1	1
I_{SIN}	Output Sink Current		10		mA	1	1
V_{OL}	Output Voltage LOW	$I_{OL} = 5.0$ mA		1.0	V	1	1
V_{OH}	Output Voltage HIGH	$I_{OH} = -50$ mA	2.0		V	1	1

Primary Burn-In Circuit



Equivalent Circuit

Refer to the Fairchild Linear Data Book Commercial Section

FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 2[5]

μA7805QB 3-Terminal Positive Voltage Regulator

Aerospace and Defense Data Sheet

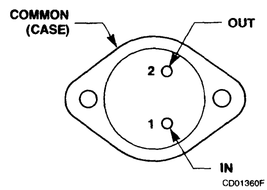
Linear Products

Description

The μA7805QB 3-Terminal Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation making it essentially indestructible. If adequate heat sinking is provided, it can deliver over 1 A output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 1 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7805KMQB	YC	2-Lead Can

JAN Product Available

10706	BYA	2-Lead Can
10706	BYC	2-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 15$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

μA7805QB

Electrical Characteristics $V_I = 10$ V, $I_L = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			4.8	5.2	V	1	1
		$5.0\text{ mA} \leq I_L \leq 1.0\text{ A}$	$V_I = 8.0$ V	4.65	5.35	V	1	1,2,3
			$V_I = 20$ V	4.65	5.35	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			1.5	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			2.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$7.0\text{ V} \leq V_I \leq 25\text{ V}$			50	mV	1	1
		$8.0\text{ V} \leq V_I \leq 25\text{ V}$			50	mV	1	2,3
		$8.0\text{ V} \leq V_I \leq 12\text{ V}$			25	mV	1	1
					50	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	$5.0\text{ mA} \leq I_L \leq 1.5\text{ A}$			100	mV	1	1,2,3
		$250\text{ mA} \leq I_L \leq 750\text{ mA}$			25	mV	1	1
					50	mV	1	2,3
I_{SCD}	Standby Current Drain				6.0	mA	1	1
					7.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$8.0\text{ V} \leq V_I \leq 25\text{ V}$			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0\text{ mA} \leq I_L \leq 1.0\text{ A}$			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A			2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			2.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 12$ V		1.3	3.3	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 10$ V, $I_L = 350$ mA, $e_i = 1.0\ V_{rms}$, $f = 2400$ Hz		60		dB	1	4
N_O	Noise	$V_I = 10$ V, $I_L = 100$ mA, $10\text{ Hz} \leq f \leq 10\text{ kHz}$			125	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 10$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 10$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA			2.5	mV/mA	4	9

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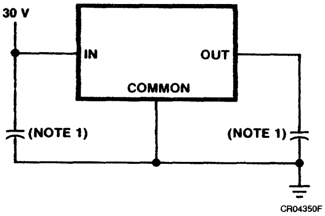
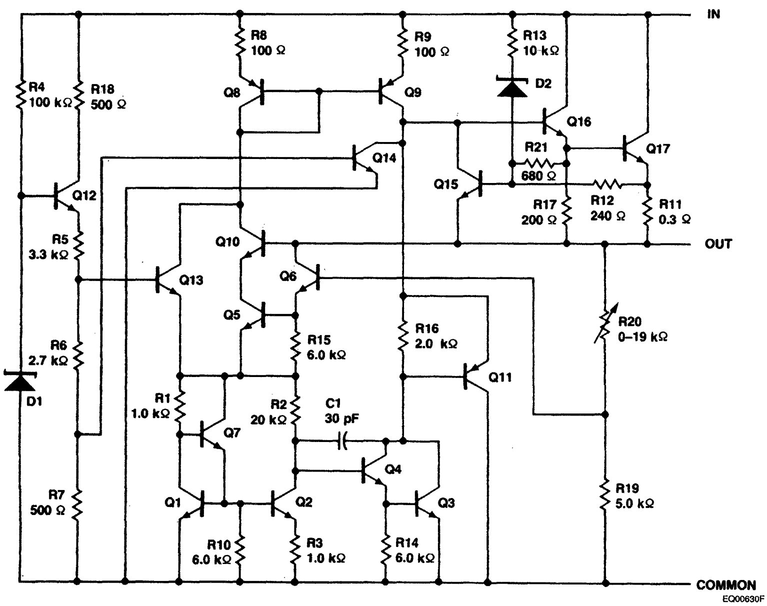
Primary Burn-In Circuit
(38510/10706 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA7812QB 3-Terminal Positive Voltage Regulator

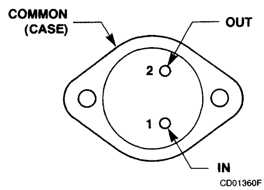
Aerospace and Defense Data Sheet
Linear Products

Description

The μA7812QB 3-Terminal Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation making it essentially indestructible. If adequate heat sinking is provided, it can deliver over 1 A output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 1 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7812KMQB	YC	2-Lead Can

JAN Product Available

10707	BYA	2-Lead Can
10707	BYC	2-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 15$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

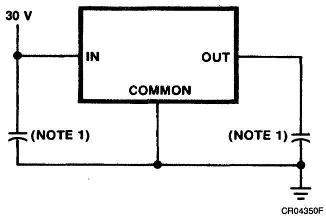
μA7812QB
Electrical Characteristics $V_I = 19$ V, $I_L = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]		11.5	12.5	V	1	1
		$5.0\ mA \leq I_L \leq 1.0\ A$, $V_I = 15.5$ V	11.4	12.6	V	1	2,3
		$V_I = 27$ V	11.4	12.6	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$		3.0	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$		3.0	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$14.5\ V \leq V_I \leq 30\ V$		120	mV	1	1
		$15\ V \leq V_I \leq 30\ V$		120	mV	1	2,3
		$16\ V \leq V_I \leq 22\ V$		60	mV	1	1
				100	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	$5.0\ mA \leq I_L \leq 1.5\ A$		120	mV	1	1
				240	mV	1	2,3
		$250\ mA \leq I_L \leq 750\ mA$		60	mV	1	1
				120	mV	1	2,3
I_{SCD}	Standby Current Drain			6.0	mA	1	1
				7.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$15\ V \leq V_I \leq 30\ V$		0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0\ mA \leq I_L \leq 1.0\ A$		0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A		2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V		2.0	A	1	1,2,3,
I_{OL}	Overload Current	$V_I = 19$ V	1.3	3.3	A	1	1,2,3,
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 19$ V, $I_L = 350$ mA, $e_i = 1.0\ V_{rms}$, $f = 2400$ Hz	60		dB	1	4
N_O	Noise	$V_I = 17$ V, $I_L = 100$ mA, $10\ Hz \leq f \leq 10\ kHz$		250	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 17$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V		30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 17$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA		2.5	mV/mA	4	9

13

Primary Burn-In Circuit

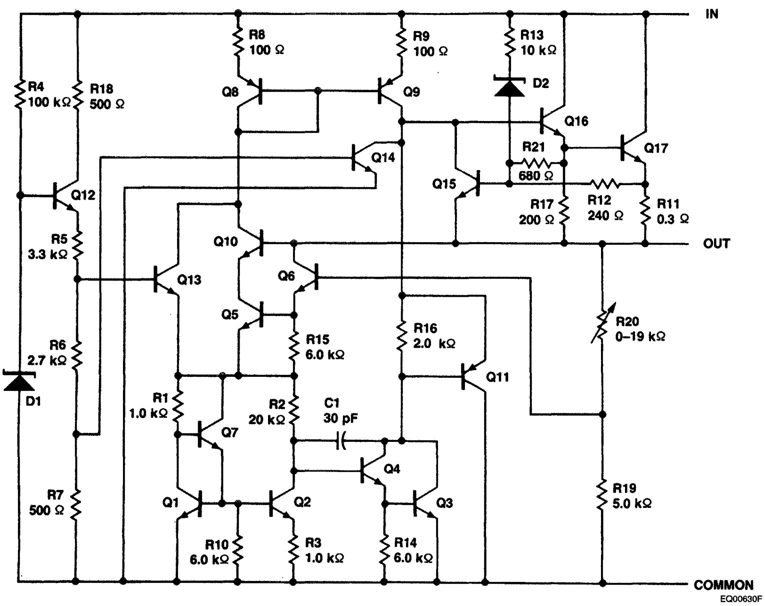
(38510/10707 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA7815QB 3-Terminal Positive Voltage Regulator

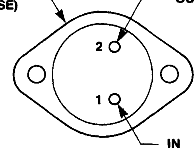
Aerospace and Defense Data Sheet
Linear Products

Description

The μA7815QB 3-Terminal Positive Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation making it essentially indestructible. If adequate heat sinking is provided, it can deliver over 1 A output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 1 A**
- **No External Components**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7815KMQB	YC	2-Lead Can

JAN Product Available

10708	BYA	2-Lead Can
10708	BYC	2-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	35 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

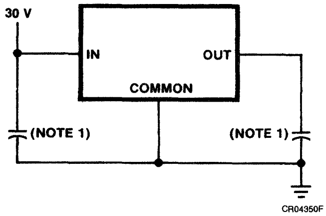
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques (t_W10 ms, duty cycle $\leqslant$5%). Output Voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 15$ W
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

μA7815QB
Electrical Characteristics $V_I = 23$ V, $I_L = 500$ mA, $C_I = 0.33$ μF, $C_O = 0.1$ μF, unless otherwise specified.[7]

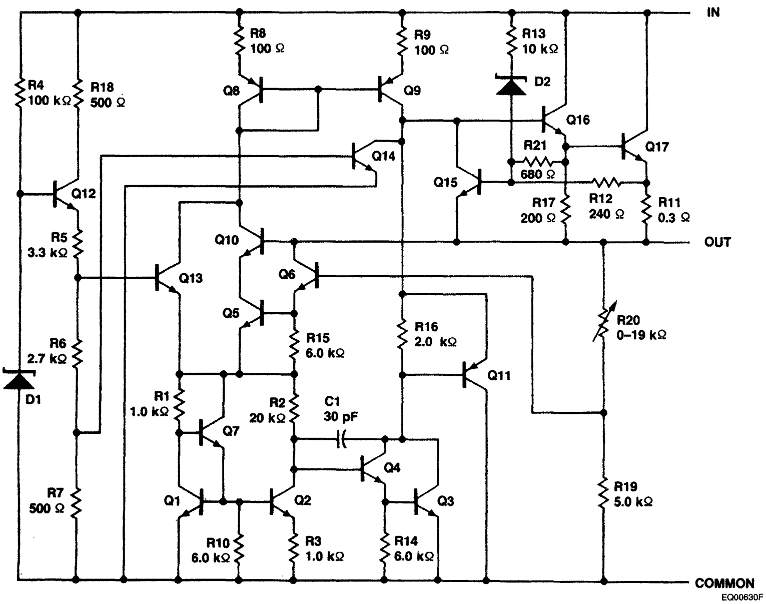
Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			14.4	15.6	V	1	1
		5.0 mA ≤ I_L ≤ 1.0 A	$V_I = 18.5$ V	14.25	15.75	V	1	1,2,3
			$V_I = 30$ V	14.25	15.75	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			3.75	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			3.75	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	17.5 V ≤ V_I ≤ 30 V			150	mV	1	1
		18.5 V ≤ V_I ≤ 30 V			150	mV	1	2,3
		20 V ≤ V_I ≤ 26 V			75	mV	1	1
					120	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 1.5 A			150	mV	1	1
					300	mV	1	2,3
		250 mA ≤ I_L ≤ 750 mA			75	mV	1	1
					150	mV	1	2,3
I_{SCD}	Standby Current Drain				6.0	mA	1	1
					7.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	18.5 V ≤ V_I ≤ 30 V			0.8	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 1.0 A			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A			2.5	V	1	1
I_{OS}	Output Short Circuit Current	$V_I = 35$ V			2.0	A	1	1,2,3
I_{OL}	Overload Current	$V_I = 22$ V		1.3	3.3	A	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = 23$ V, $I_L = 350$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		60		dB	1	4
N_O	Noise	$V_I = 20$ V, $I_L = 100$ mA, 10 Hz ≤ f ≤ 10 kHz			300	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = 20$ V, $I_L = 5.0$ mA, $V_{pulse} = 3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = 20$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA			2.5	mV/mA	4	9

Primary Burn-In Circuit
(38510/10708 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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MIL-STD-883
July 1986—Rev 2[5]

μA79M05QB 3-Terminal Negative Voltage Regulator

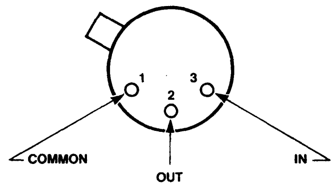
Aerospace and Defense Data Sheet
Linear Products

Description

The μA79M05QB 3-Terminal Medium Current Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver up to 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

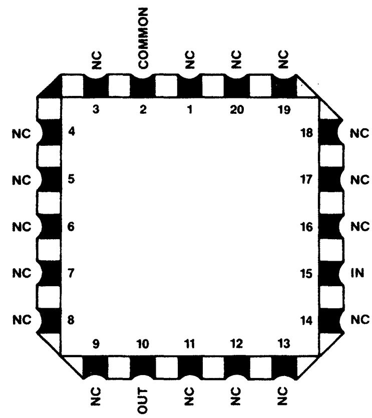
- **Output Current In Excess Of 0.5 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA79M05HMQB	XC	3-Lead Can
μA79M05LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

11501	BXC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can Without Heat Sink[11]	0.18 W
Can With Heat Sink[12]	0.5 W
CCP Without Heat Sink[13]	0.4 W
Input Voltage	−35 V

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 4$ W.
9. Slowly ramp input voltage up to −8.0 V, When circuit starts, output voltage will be as specified.
10. Internally limited.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
13. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

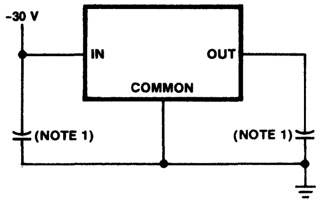
Group C and D Endpoints: Group A, Subgroup 1

μA79M05QB

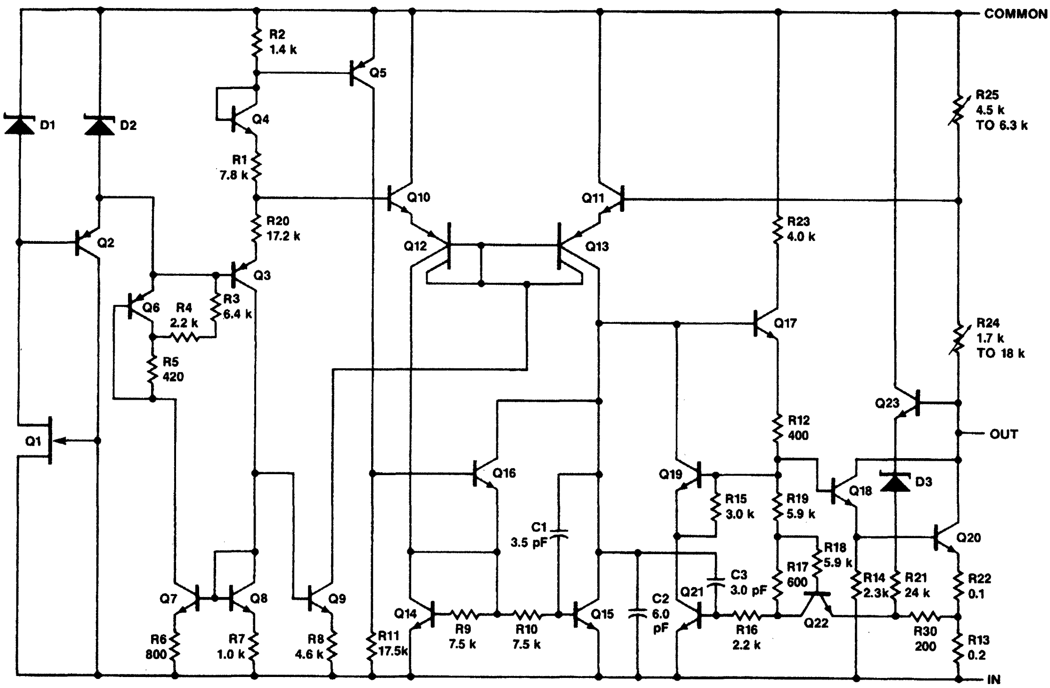
Electrical Characteristics $V_I = -10$ V, $I_L = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			-5.2	-4.8	V	1	1
		5.0 mA $\leq I_L \leq$ 350 mA	$V_I = -7.0$ V	-5.25	-4.75	V	1	1,2,3
			$V_I = -25$ V	-5.25	-4.75	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C $\leq T_A \leq$ 125°C			1.5	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C $\leq T_A \leq$ 25°C			1.5	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	−25 V $\leq V_I \leq$ −7.0 V			50	mV	1	1
		−25 V $\leq V_I \leq$ −8 V			50	mV	1	2,3
		−18 V $\leq V_I \leq$ −8.0 V			30	mV	1	1
					60	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA $\leq I_L \leq$ 500 mA			100	mV	1	1,2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	−25 V $\leq V_I \leq$ −8.0 V			0.4	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA $\leq I_L \leq$ 350 mA			0.4	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			1.0	A	1	1,2,3
I_{pk}	Peak Output Current	$V_I - V_O = -10$ V		0.5	2.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -15$ V, $I_L = 1.0$ A			50	mV	3	1
V_{START}	Voltage Start[9]				-4.75	V	1	1,2,3,
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -10$ V, $I_L = 125$ mA, $e_i = 1.0\ V_{rms}$, f = 2400 Hz		50		dB	1	4,5,6
N_O	Noise	$V_I = -10$ V, $I_L = 50$ mA, 10 Hz $\leq f \leq$ 10 kHz			250	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -10$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -10$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

Primary Burn-In Circuit
(38510/11501 may be used by FSC as an alternate)



Equivalent Circuit (Note 2)



Notes
1. Capacitor value necessary to suppress oscillations.
2. All resistor values in ohms.

EQ00890F

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MIL-STD-883

July 1986—Rev 2[5]

μA79M08QB 3-Terminal Negative Voltage Regulator

Aerospace and Defense Data Sheet

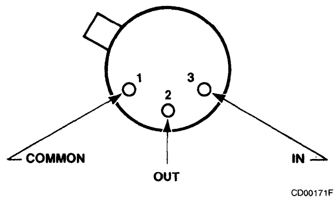
Linear Products

Description

The μA79M08QB 3-Terminal Medium Current Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver up to 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

- **Output Current In Excess Of 0.5 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
3-Lead TO-39 Can
(Top View)



Lead 3 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA79M08HMQB	XC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.18 W
Can With Heat Sink[11]	0.5 W
Input Voltage	−35 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 4$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

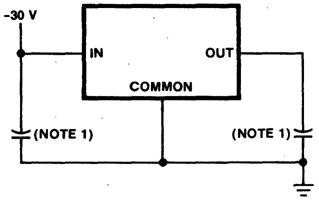
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA79M08QB
Electrical Characteristics $V_I = -14$ V, $I_L = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			-8.3	-7.7	V	1	1
		5.0 mA ≤ I_L ≤ 350 mA	$V_I = -10.5$ V	-8.4	-7.6	V	1	1,2,3
			$V_I = -25$ V	-8.4	-7.6	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			2.4	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			2.4	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	−25 V ≤ V_I ≤ −10.5 V			80	mV	1	1
		−21 V ≤ V_I ≤ −11 V			50	mV	1	1
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 500 mA			160	mV	1	1
I_{SCD}	Standby Current Drain				2.0	mA	1	1
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	−25 V ≤ V_I ≤ −10.5 V			0.4	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 350 mA			0.4	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			1.0	A	1	1
I_{pk}	Peak Output Current	$V_I - V_O = -10$ V		0.5	2.0	A	1	1
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -13$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		50		dB	1	4
N_O	Noise	$V_I = -13$ V, $I_L = 50$ mA, 10 Hz ≤ f ≤ 10 kHz			400	μV_{rms}	4	9

Primary Burn-In Circuit



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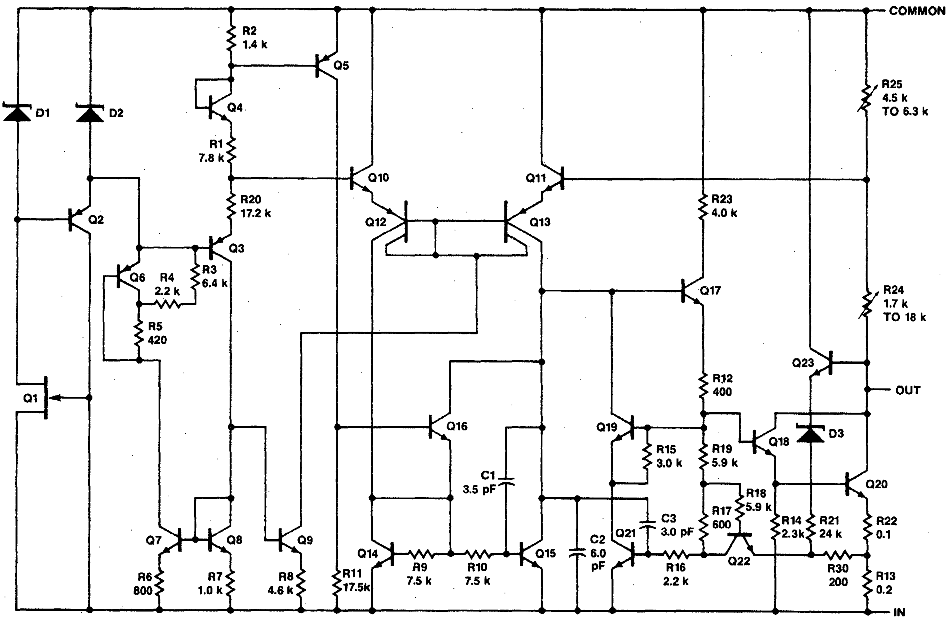
Equivalent Circuit (Note 2)



Notes
1. Capacitor value necessary to suppress oscillations.
2. All resistor values in ohms.

EQ00900F

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MIL-STD-883
July 1986—Rev 2[5]

μA79M12QB 3-Terminal Negative Voltage Regulator

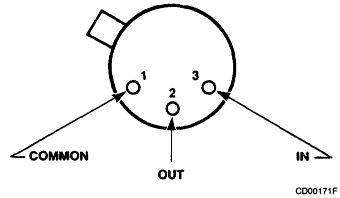
Aerospace and Defense Data Sheet
Linear Products

Description

The μA79M12QB 3-Terminal Medium Current Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver up to 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

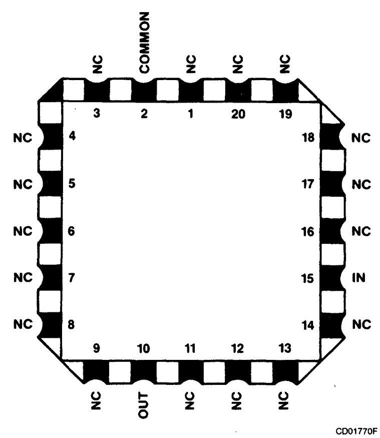
- **Output Current In Excess Of 0.5 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA79M12HMQB	XC	3-Lead Can
μA79M12LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

11502	BXC	3-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can Without Heat Sink[11]	0.18 W
Can With Heat Sink[12]	0.5 W
CCP Without Heat Sink[13]	0.4 W
Input Voltage	-35 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 4$ W.
9. Slowly ramp input voltage up to -8.0 V. When circuit starts, output voltage will be as specified.
10. Internally limited.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
13. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

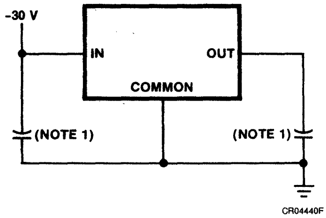
Group C and D Endpoints: Group A, Subgroup 1

μA79M12QB

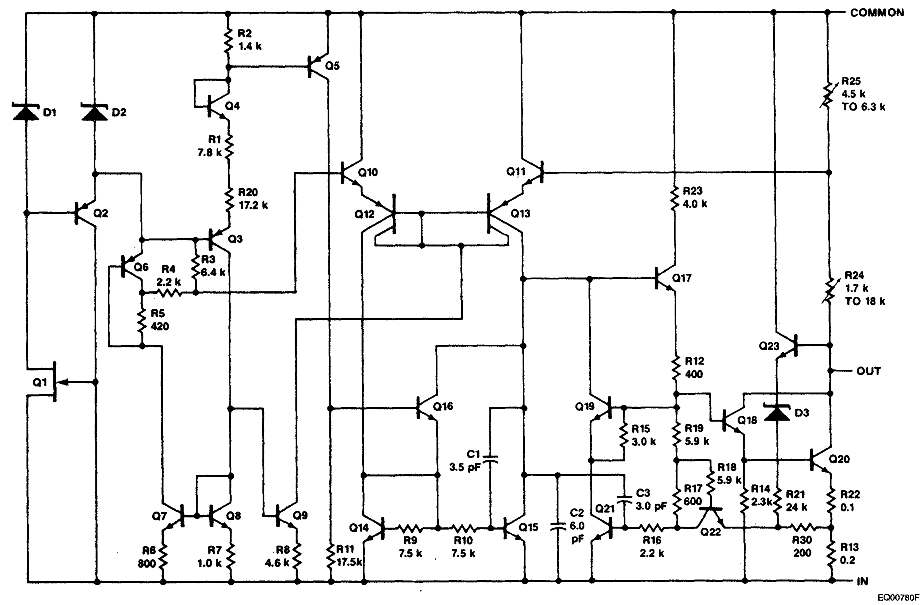
Electrical Characteristics $V_I = -19$ V, $I_L = 350$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			-12.5	-11.5	V	1	1
		$5.0 \text{ mA} \leq I_L \leq 350 \text{ mA}$	$V_I = -14.5$ V	-12.6	-11.4	V	1	1,2,3
			$V_I = -30$ V	-12.6	-11.4	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, $25°C \leq T_A \leq 125°C$			3.6	mV/°C	4	2
		$I_L = 5.0$ mA, $-55°C \leq T_A \leq 25°C$			3.6	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	$-30 \text{ V} \leq V_I \leq -14.5 \text{ V}$			80	mV	1	1
		$-30 \text{ V} \leq V_I \leq 15 \text{ V}$			120	mV	1	2,3
		$-25 \text{ V} \leq V_I \leq -15 \text{ V}$			50	mV	1	1
					75	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	$5.0 \text{ mA} \leq I_L \leq 500 \text{ mA}$			240	mV	1	1,2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	$-30 \text{ V} \leq V_I \leq -14.5 \text{ V}$			0.4	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	$5.0 \text{ mA} \leq I_L \leq 350 \text{ mA}$			0.4	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			1.0	A	1	1,2,3
I_{pk}	Peak Output Current	$V_I - V_O = -10$ V		0.5	2.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -22$ V, $I_L = 500$ mA			120	mV	3	1
V_{START}	Voltage Start[9]				-4.75	V	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -17$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		50		dB	1	4,5,6
N_O	Noise	$V_I = -17$ V, $I_L = 50$ mA, 10 Hz ≤ f ≤ 10 kHz			600	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -17$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -17$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

Primary Burn-In Circuit
(38510/11502 may be used by FSC as an alternate)



Equivalent Circuit (Note 2)



Notes
1. Capacitor value necessary to suppress oscillations.
2. All resistor values in ohms.

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MIL-STD-883
July 1986—Rev 2[5]

μA79M15QB 3-Terminal Negative Voltage Regulator

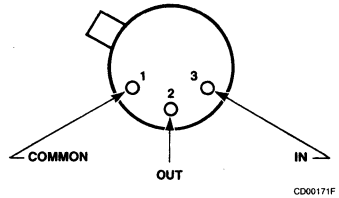
Aerospace and Defense Data Sheet
Linear Products

Description

The μA79M15QB 3-Terminal Medium Current Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making it essentially indestructible. If adequate heat sinking is provided, it can deliver up to 500 mA output current. It is intended as a fixed voltage regulator in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as a fixed voltage regulator, this device can be used with external components to obtain adjustable output voltages and currents.[6]

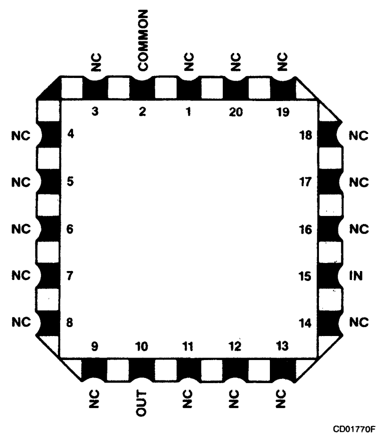
- **Output Current In Excess Of 0.5 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 3-Lead TO-39 Can (Top View)



Lead 3 connected to case.

Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA79M15HMQB	XC	3-Lead Can
μA79M15LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

11503	BXC	3-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can Without Heat Sink[11]	0.18 W
Can With Heat Sink[12]	0.5 W
CCP Without Heat Sink[13]	0.4 W
Input Voltage	−35 V

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 4$ W.
9. Slowly ramp input voltage up to −8.0 V. When circuit starts, output voltage will be as specified.
10. Internally limited.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 140°C/W.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 50°C/W.
13. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA79M15QB
Electrical Characteristics $V_I = -23$ V, 350 mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			−15.6	−14.4	V	1	1
		5.0 mA $\leq I_L \leq$ 350 mA	$V_I = -17.5$ V	−15.75	−14.25	V	1	1,2,3
			$V_I = -30$ V	−15.75	−14.25	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C $\leq T_A \leq$ 125°C			4.5	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C $\leq T_A \leq$ 25°C			4.5	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	−30 V $\leq V_I \leq$ −17.5 V			80	mV	1	1
		−30 V $\leq V_I \leq$ 18.5 V			150	mV	1	2,3
		−28 V $\leq V_I \leq$ −18 V			50	mV	1	1
					80	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA $\leq I_L \leq$ 500 mA			240	mV	1	1
					300	mV	1	2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	−30 V $\leq V_I \leq$ −17.5 V			0.4	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA $\leq I_L \leq$ 350 mA			0.4	mA	1	1,2,3
V_{DO}	Dropout Voltage				2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			1.0	A	1	1,2,3,
I_{pk}	Peak Output Current	$V_I - V_O = -10$ V		0.5	2.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -25$ V, $I_L = 500$ mA			150	mV	4	1
V_{START}	Voltage Start[9]				−4.75	V	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -20$ V, $I_L = 125$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		50		dB	1	4,5,6
N_O	Noise	$V_I = -20$ V, $I_L = 50$ mA, 10 Hz $\leq f \leq$ 10 kHz			700	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -20$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -20$ V, $I_L = 50$ mA, $\Delta I_L = 200$ mA			2.5	mV/mA	4	9

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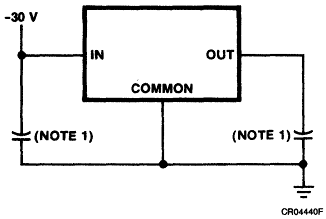
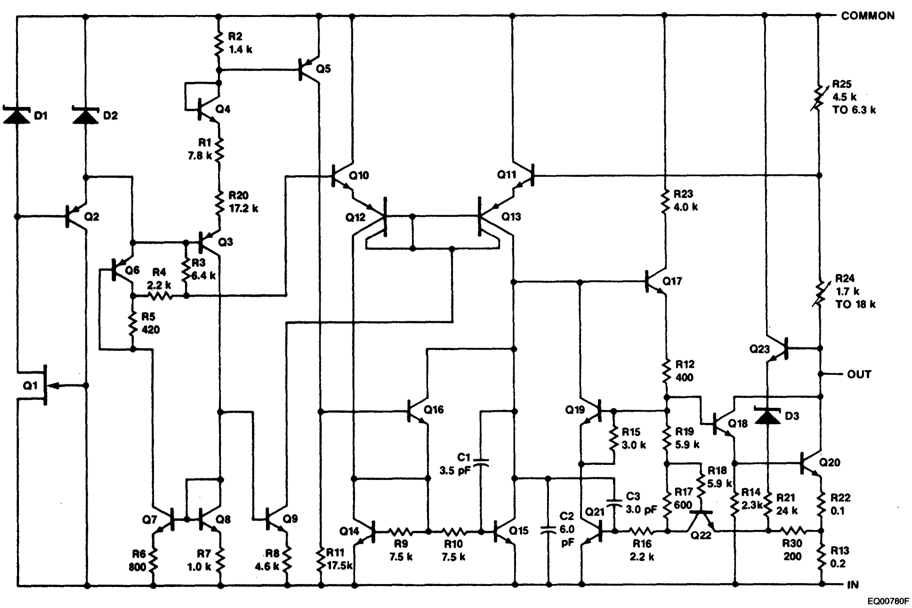
Primary Burn-In Circuit
(38510/11503 may be used by FSC as an alternate)



Equivalent Circuit (Note 2)



Notes

1. Capacitor value necessary to suppress oscillations.
2. All resistor values in ohms.

FAIRCHILD

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MIL-STD-883
July 1986—Rev 1[5]

μA7905QB 3-Terminal Negative Voltage Regulator

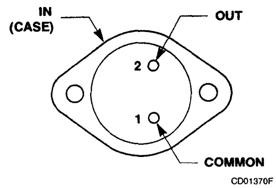
Aerospace and Defense Data Sheet
Linear Products

Description

The μA7905QB 3-Terminal Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This negative regulator is intended as a complement to the popular μA7805QB Positive Voltage Regulator. The μA7905QB employs internal current-limiting, safe-area protection, and thermal shutdown, making it virtually indestructible.[6]

- **Output Current In Excess Of 1 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram 2-Lead TO-3 Can (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7905KMQB	YC	2-Lead Can

JAN Product Available

11505	BYA	2-Lead Can
11505	BYC	2-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	−35 V

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 15$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA7905QB
Electrical Characteristics $V_I = -10$ V, $I_L = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			-5.2	-4.8	V	1	1
		5.0 mA ≤ I_L ≤ 1.0 A	$V_I = -8.0$ V	-5.3	-4.7	V	1	1,2,3
			$V_I = -20$ V	-5.3	-4.7	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			1.5	mV/°C	4	2
		$I_L = 5.0$ mA, -55°C ≤ T_A ≤ 25°C			1.5	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	-25 V ≤ V_I ≤ -7.0 V			50	mV	1	1
		-25 V ≤ V_I ≤ -8.0 V			75	mV	1	2,3
		-12 V ≤ V_I ≤ -8.0 V			25	mV	1	1
					50	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 1.5 A			100	mV	1	1,2,3
		250 mA ≤ I_L ≤ 750 mA			35	mV	1	1
					60	mV	1	2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	-25 V ≤ V_I ≤ -8.0 V			1.3	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 1.0 A			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A			2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			2.0	A	1	1,2,3
I_{pk}	Peak Output Current	$V_I = -8.0$ V, $\Delta V_O = 0.48$ V		1.0	4.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -15$ V, $I_L = 1.0$ A			50	mV	1	1
V_{START}	Voltage Start	$V_I = -20$ V, $R_L = 5.0$ Ω		-5.25	-4.75	V	4	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -10$ V, $I_L = 350$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		45		dB	1	4,5,6
N_O	Noise	$V_I = -10$ V, $I_L = 100$ mA, 10 Hz ≤ f ≤ 10 kHz			250	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -10$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -10$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA			2.5	mV/mA	4	9

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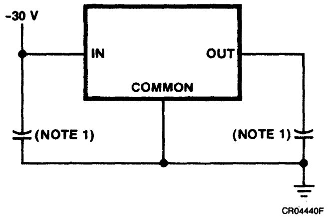
Primary Burn-In Circuit

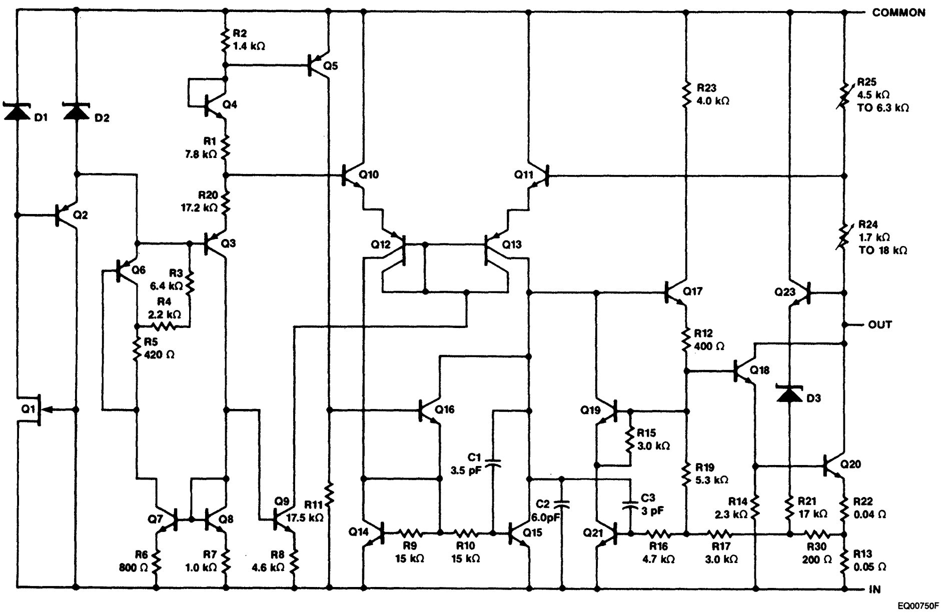
(38510/11505 may be used by FSC as an alternate)



Note

1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA7912QB 3-Terminal Negative Voltage Regulator

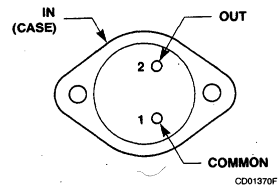
Aerospace and Defense Data Sheet
Linear Products

Description

The μA7912QB 3-Terminal Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This negative regulator is intended as a complement to the popular μA7812QB Positive Voltage Regulator. The μA7912QB employs internal current-limiting, safe-area protection, and thermal shutdown, making it virtually indestructible.[6]

- **Output Current In Excess Of 1 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7912KMQB	YC	2-Lead Can

JAN Product Available

11506	BYA	2-Lead Can
11506	BYC	2-Lead Can

13

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	−35 V

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leqslant 10$ ms, duty cycle $\leqslant 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leqslant 15$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

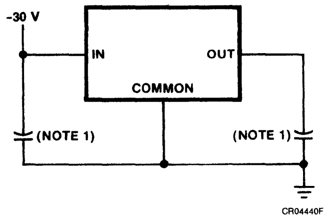
Group C and D Endpoints: Group A, Subgroup 1

μA7912QB
Electrical Characteristics $V_I = -19$ V, $I_L = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			−12.5	−11.5	V	1	1
		5.0 mA ≤ I_L ≤ 1.0 A	$V_I = -15.5$ V	−12.6	−11.4	V	1	1,2,3
			$V_I = -27$ V	−12.6	−11.4	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			3.6	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			3.6	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	−30 V ≤ V_I ≤ −14.5 V			120	mV	1	1
		−30 V ≤ V_I ≤ −15 V			120	mV	1	2,3
		−22 V ≤ V_I ≤ −16 V			60	mV	1	1
					90	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 1.5 A			120	mV	1	1
					240	mV	1	2,3
		250 mA ≤ I_L ≤ 750 mA			84	mV	1	1
					160	mV	1	2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	−30 V ≤ V_I ≤ −15 V			1.0	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 1.0 A			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A			2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			2.0	A	1	1,2,3
I_{pk}	Peak Output Current	$V_I = -15$ V, $\Delta V_O = 1.13$ V		1.0	4.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -22$ V, $I_L = 1.0$ A			120	mV	1	1
V_{START}	Voltage Start	$V_I = -27$ V, $R_L = 12\ \Omega$		−12.6	−11.4	V	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -17$ V, $I_L = 350$ mA, $e_i = 1.0\ V_{rms}$, f = 2400 Hz		50		dB	1	4,5,6
N_O	Noise	$V_I = -17$ V, $I_L = 100$ mA, 10 Hz ≤ f ≤ 10 kHz			600	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -17$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -17$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA			2.5	mV/mA	4	9

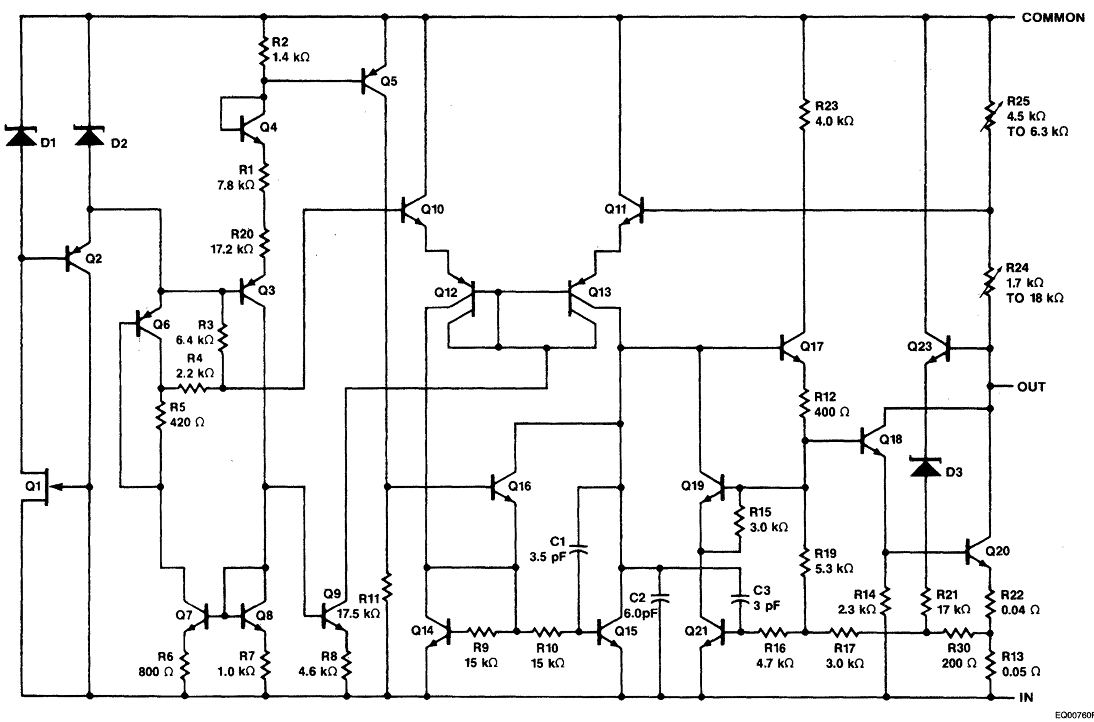
13

Primary Burn-In Circuit
(38510/11506 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



MIL-STD-883
July 1986—Rev 1[5]

μA7915QB 3-Terminal Negative Voltage Regulator

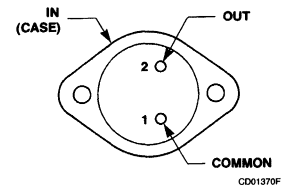
Aerospace and Defense Data Sheet
Linear Products

Description

The μA7915QB 3-Terminal Negative Voltage Regulator is constructed using the Fairchild Planar Epitaxial process. This negative regulator is intended as a complement to the popular μA7815QB Positive Voltage Regulator. The μA7915QB employs internal current-limiting, safe-area protection, and thermal shutdown, making it virtually indestructible.[6]

- **Output Current In Excess Of 1 A**
- **Internal Thermal Overload Protection**
- **Internal Short Circuit Current-Limiting**
- **Output Transistor Safe-Area Compensation**

Connection Diagram
2-Lead TO-3 Can
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA7915KMQB	YC	2-Lead Can

JAN Product Available

11507	BYA	2-Lead Can
11507	BYC	2-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can Without Heat Sink[10]	0.71 W
Can With Heat Sink[11]	5.6 W
Input Voltage	−35 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. All characteristics except line and load transient response and noise are measured using pulse techniques ($t_W \leq 10$ ms, duty cycle $\leq 5\%$). Output voltage changes due to changes in the internal temperature must be taken into account separately.
8. Conditions given will result in the following: $P_D \leq 15$ W.
9. Internally limited.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 35°C/W.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C, derate linearly at 4.46°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

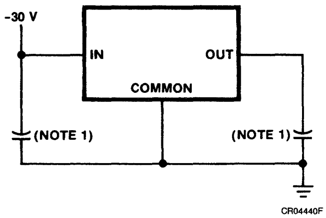
μA7915QB

Electrical Characteristics $V_I = -23$ V, $I_L = 500$ mA, $C_I = 2.0$ μF, $C_O = 1.0$ μF, unless otherwise specified.[7]

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_O	Output Voltage[8]			−15.6	−14.4	V	1	1
		5.0 mA ≤ I_L ≤ 1.0 A	$V_I = -18.5$ V	−15.75	−14.25	V	1	1,2,3
			$V_I = -30$ V	−15.75	−14.25	V	1	1,2,3
$\Delta V_O/\Delta T$	Average Temperature Coefficient of Output Voltage	$I_L = 5.0$ mA, 25°C ≤ T_A ≤ 125°C			4.5	mV/°C	4	2
		$I_L = 5.0$ mA, −55°C ≤ T_A ≤ 25°C			4.5	mV/°C	4	3
$V_{R\ LINE}$	Line Regulation	−30 V ≤ V_I ≤ −17.5 V			150	mV	1	1
		−30 V ≤ V_I ≤ −18.5 V			150	mV	1	2,3
		−26 V ≤ V_I ≤ −20 V			75	mV	1	1
					120	mV	1	2,3
$V_{R\ LOAD}$	Load Regulation	5.0 mA ≤ I_L ≤ 1.5 A			150	mV	1	1
					300	mV	1	2,3
		250 mA ≤ I_L ≤ 750 mA			105	mV	1	1
					180	mV	1	2,3
I_{SCD}	Standby Current Drain				2.0	mA	1	1
					3.0	mA	1	2,3
ΔI_{SCD} (LINE)	Standby Current Drain Change (vs Line Voltage)	−30 V ≤ V_I ≤ −18.5 V			1.0	mA	1	1,2,3
ΔI_{SCD} (LOAD)	Standby Current Drain Change (vs Load Current)	5.0 mA ≤ I_L ≤ 1.0 A			0.5	mA	1	1,2,3
V_{DO}	Dropout Voltage	$I_L = 1.0$ A			2.3	V	1	1
I_{OS}	Short Circuit Current	$V_I = -35$ V			2.0	A	1	1,2,3
I_{pk}	Peak Output Current	$V_I = -18.5$ V, $\Delta V_O = 1.43$ V		1.0	4.0	A	1	1,2,3
V_{RTH}	Thermal Regulation	$V_I = -25$ V, $I_L = 1.0$ A			150	mV	1	1
V_{START}	Voltage Start	$V_I = -30$ V, $R_L = 15$ Ω		−15.75	−14.25	V	1	1,2,3
$\Delta V_I/\Delta V_O$	Ripple Rejection	$V_I = -20$ V, $I_L = 350$ mA, $e_i = 1.0$ V_{rms}, f = 2400 Hz		50		dB	1	4,5,6
N_O	Noise	$V_I = -20$ V, $I_L = 100$ mA, 10 Hz ≤ f ≤ 10 kHz			700	μV_{rms}	4	9
$\Delta V_O/\Delta V_I$	Line Transient Response	$V_I = -20$ V, $I_L = 5.0$ mA, $V_{pulse} = -3.0$ V			30	mV/V	4	9
$\Delta V_O/\Delta I_L$	Load Transient Response	$V_I = -20$ V, $I_L = 100$ mA, $\Delta I_L = 400$ mA			2.5	mV/mA	4	9

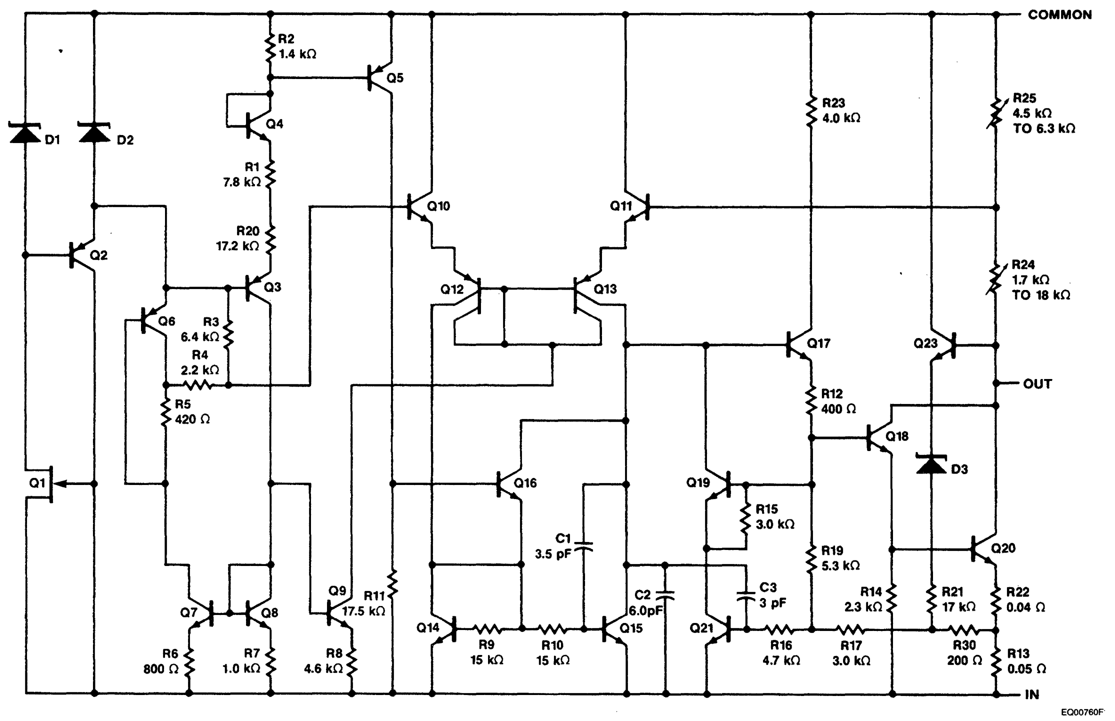
13

Primary Burn-In Circuit
(38510/11507 may be used by FSC as an alternate)



Note
1. Capacitor value necessary to suppress oscillations.

Equivalent Circuit



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MIL-STD-883
July 1986—Rev 0[1]

Advance Information

μA1524AQB Advanced Regulating Pulse Width Modulator

Aerospace and Defense Data Sheet
Linear Products

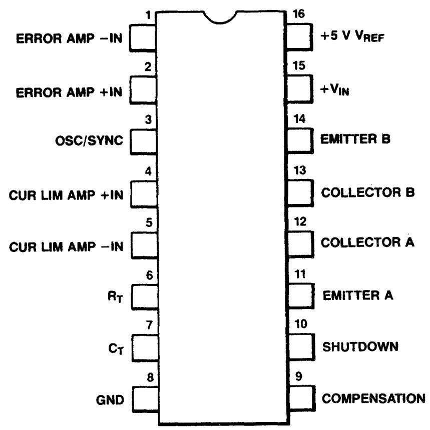
Description

The μA1524AQB is an advanced regulating pulse width modulator which includes a precise 5.0 V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5.0 V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60 V, 200 mA uncommitted transistor switches which greatly enhance output versatility. Included is an under voltage lockout circuit which disables all the internal circuitry except the reference, until the input voltage has risen to 8.0 V. This holds standby current low until turn-on, simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600 mV of hysteresis for jitter free activation. Also, included is a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments; logic to eliminate double pulsing on a single output; and a 200 ns external shutdown capability. The oscillator circuit is usable beyond 500 kHz and is easy to synchronize with an external clock pulse.[2]

- **Precision Reference Internally Trimmed To ±1%**
- **High Performance Current-Limit Function**
- **Under Voltage Lockout With Hysteristic Turn-On**
- **Start-Up Supply Current Less Than 4.0 mA**
- **Output Current To 200 mA**
- **60 V Output Capability**
- **Wide Common Mode Input Range For Both Error And Current Limit Amplifiers**
- **PWM Latch Insures Single Pulse Per Period**
- **Double Pulse Suppression Logic**
- **200 ns Shutdown Through PWM Latch**
- **Guaranteed Frequency Accuracy**

Notes
1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram 16-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA1524ADMQB	EA	D-2 16-Lead DIP

13

μA101AQB General Purpose Operational Amplifier

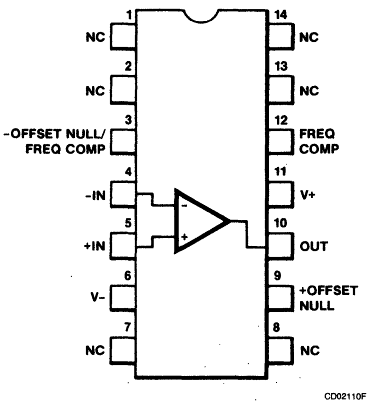
Aerospace and Defense Data Sheet
Linear Products

Description

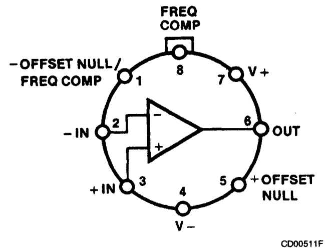
The μA101AQB is a general purpose monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. This integrated circuit is intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers, and sample and hold circuits is improved due to the low drift and low bias currents. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of 'latch-up' coupled with internal short circuit protection make the μA101AQB virtually foolproof.[6]

- **Low Offset Current And Voltage**
- **Low Offset Current Drift**
- **Low Bias Current**
- **Short Circuit Protected**
- **Low Power Consumption**

Connection Diagram 14-Lead DIP (Top View)

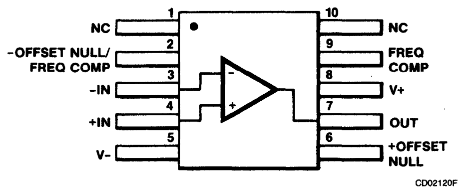


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA101ADMQB	CA	D-1 14-Lead DIP
μA101AHMQB	GC	A-1 8-Lead Can
μA101AFMQB	HA	F-4 10-Lead Flatpak

JAN Product Available

10103	BCA	D-1 14-Lead DIP
10103	BCB	D-1 14-Lead DIP
10103	BGA	A-1 8-Lead Can
10103	BGC	A-1 8-Lead Can
10103	BHA	F-4 10-Lead Flatpak
10103	BHB	F-4 10-Lead Flatpak
10103	BPA	D-4 8-Lead DIP
10103	BPB	D-4 8-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[12]	±20 V
Short Circuit Duration[13]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

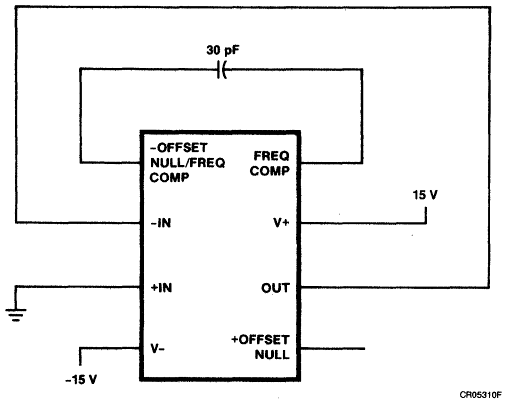
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C and 19 mV at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 40\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. BW is guaranteed by t_r: $BW = 0.35/t_r$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA101AQB

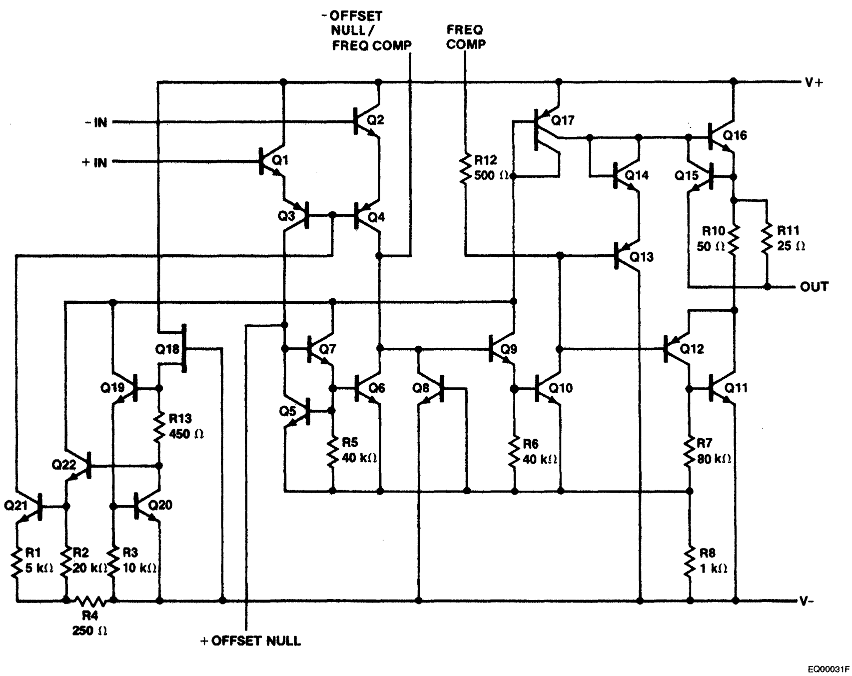
Electrical Characteristics $V_{CC} = \pm 20$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, $R_S = 50\ \Omega$, $V_{CM} = 0\ V$		2.0	mV	1	1
				3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		25	μV/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		25	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_{adj} = 5.1\ M\Omega$	1.0		mV	1	1,2,3
I_{IO}	Input Offset Current	$V_{CM} = 0\ V$		10	nA	1	1
				20	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		0.1	nA/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		0.2	nA/°C	4	3
I_{IB}	Input Bias Current	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, $V_{CM} = 0\ V$		68	nA	1	1
				100	nA	1	2,3
Z_I	Input Impedance[7]		1.5		MΩ	1	1
I_{CC}	Supply Current			3.0	mA	1	1
				2.5	mA	1	2
				3.5	mA	1	3
P_c	Power Consumption[8]			120	mW	1	1
				100	mW	1	2
CMR	Common Mode Rejection	$V_{CM} = \pm 15\ V$, $R_S = 50\ \Omega$	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]		±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, $R_S = 50\ \Omega$		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current	$V_{CC} = \pm 15\ V$		60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L = 2.0\ k\Omega$	50		V/mV	1	4
			25		V/mV	1	5,6
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±12		V	1	4,5,6
		$R_L = 2.0\ k\Omega$	±10		V	1	4,5,6
$TR(t_r)$	Transient Response — Rise Time	$V_I = 50\ mV$, $R_L = 2.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$	Transient Response — Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[10]		0.437		MHz	3	9, 10, 11
SR	Slew Rate	$R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.3		V/μs	3	9, 10
			0.2		V/μs	3	11
N_I (BB)	Noise Broadband	BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn	BW = 5.0 kHz		80	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10103 may be used by FSC as an alternate)



Equivalent Circuit



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MIL-STD-883

July 1986—Rev 1[5]

μA101QB General Purpose Operational Amplifier

Aerospace and Defense Data Sheet

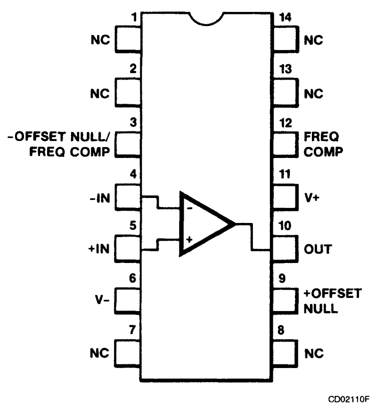
Linear Products

Description

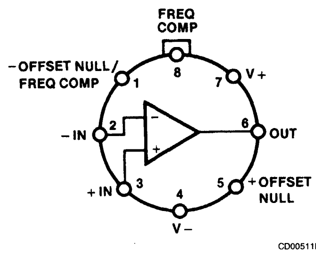
The μA101QB is a general purpose monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. This integrated circuit is intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers, and sample and hold circuits is improved due to the low drift and low bias currents. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of 'latch-up' coupled with internal short circuit protection make the μA101QB virtually foolproof.[6]

- **Low Offset Current And Voltage**
- **Low Offset Current Drift**
- **Low Bias Current**
- **Short Circuit Protected**
- **Low Power Consumption**

Connection Diagram 14-Lead DIP (Top View)

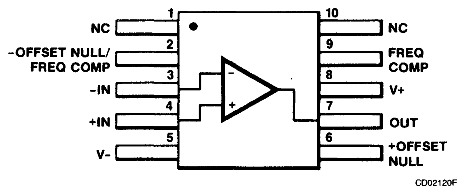


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA101DMQB	CA	D-1 14-Lead DIP
μA101HMQB	GC	A-1 8-Lead Can
μA101FMQB	HA	F-4 10-Lead Flatpak

JAN Product Available

10103	BCA	D-1 14-Lead DIP
10103	BCB	D-1 14-Lead DIP
10103	BGA	A-1 8-Lead Can
10103	BGC	A-1 8-Lead Can
10103	BHA	F-4 10-Lead Flatpak
10103	BHB	F-4 10-Lead Flatpak
10103	BPA	D-4 8-Lead DIP
10103	BPB	D-4 8-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[12]	±20 V
Short Circuit Duration[13]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

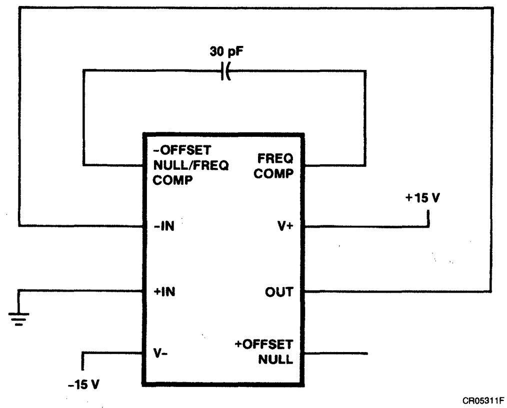
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 40\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. BW is guaranteed by t_r: $BW = 0.35/t_r$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

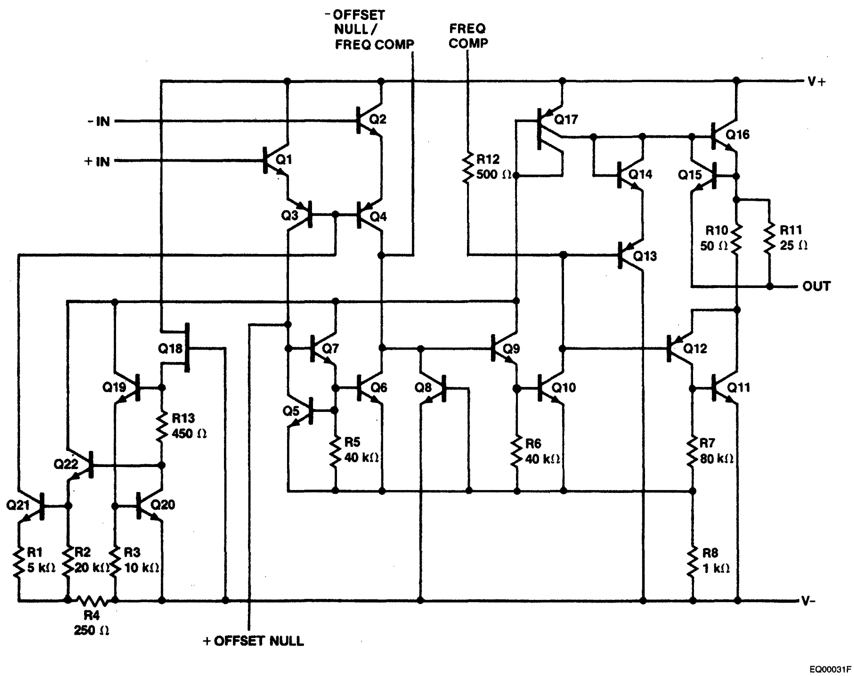
μA101QB
Electrical Characteristics $V_{CC} = \pm 20$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$\pm 5.0\ V \leq V_{CC} \leq \pm 20$ V, $R_S = 50\ \Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
				6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25°C \leq T_A \leq 125°C$		25	μV/°C	4	2
		$-55°C \leq T_A \leq +25°C$		25	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$R_{adj} = 5.1$ MΩ	1.0		mV	1	1,2,3
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		200	nA	1	1,2
				500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leq T_A \leq 125°C$		0.1	nA/°C	4	2
		$-55°C \leq T_A \leq +25°C$		0.2	nA/°C	4	3
I_{IB}	Input Bias Current	$\pm 5.0\ V \leq V_{CC} \leq \pm 20$ V, $V_{CM} = 0$ V		340	nA	1	1
				750	nA	1	2,3
Z_I	Input Impedance[7]		0.3		MΩ	1	1
I_{CC}	Supply Current			3.0	mA	1	1
				2.5	mA	1	2
				3.5	mA	1	3
P_c	Power Consumption[8]			120	mW	1	1
				100	mW	1	2
CMR	Common Mode Rejection	$V_{CM} = \pm 15$ V, $R_S = 50\ \Omega$	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]		±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 5.0\ V \leq V_{CC} \leq \pm 20$ V, $R_S = 50\ \Omega$		316	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current	$V_{CC} = \pm 15$ V		60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15$ V, $V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
			25		V/mV	1	5,6
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15$ V, $R_L = 10$ kΩ	±12		V	1	4,5,6
		$V_{CC} = \pm 15$ V, $R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response — Rise Time	$V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$	Transient Response — Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[10]		0.437		MHz	3	9, 10, 11
SR	Slew Rate	$R_L = 2.0$ kΩ, $A_V = 1.0$	0.3		V/μs	3	9, 10
			0.2		V/μs	3	11
N_I (BB)	Noise Broadband	BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn	BW = 5.0 kHz		80	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10103 may be used by FSC as an alternate)



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 2[5]

μA108AQB Super Beta Operational Amplifier

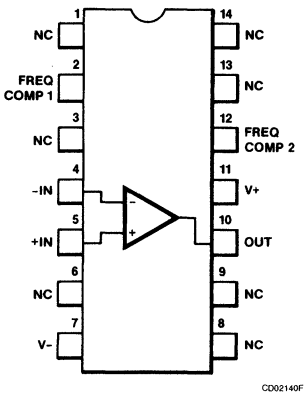
Aerospace and Defense Data Sheet
Linear Products

Description

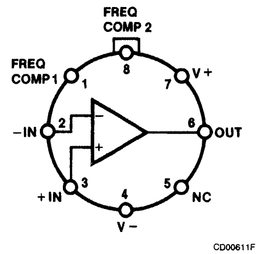
The μA108AQB Super Beta Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low noise, low input offsets, and low temperature drifts are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA108AQB is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.[6]

- **Guaranteed Low Input Offset Characteristics**
- **High Input Impedance**
- **Low Offset Current**
- **Low Bias Current**
- **Operation Over Wide Supply Range**

Connection Diagram 14-Lead DIP (Top View)

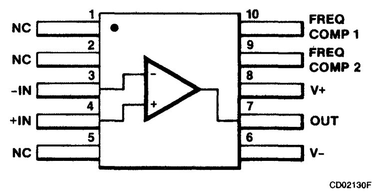


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA108ADMQB	CA	D-1 14-Lead DIP
μA108AHMQB	GC	A-1 8-Lead Can
μA108AFMQB	HA	F-4 10-Lead Flatpak

JAN Product Available

10104	BCA	D-1 14-Lead DIP
10104	BCC	D-1 14-Lead DIP
10104	BGA	A-1 8-Lead Can
10104	BGC	A-1 8-Lead Can
10104	BHA	F-4 10-Lead Flatpak
10104	BHB	F-4 10-Lead Flatpak

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite
Differential Input Current[12]	±10 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

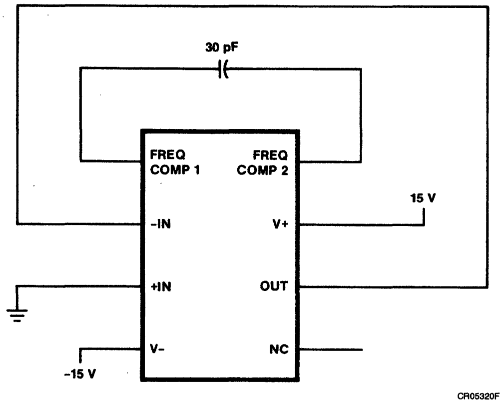
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2[(V_T/I_{IB}) + 1001R_E(10^{-6})]$, $V_T = 26$ mV at 25°C, $R_E = 1700\ \Omega$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.
12. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless adequate limiting resistance is used.

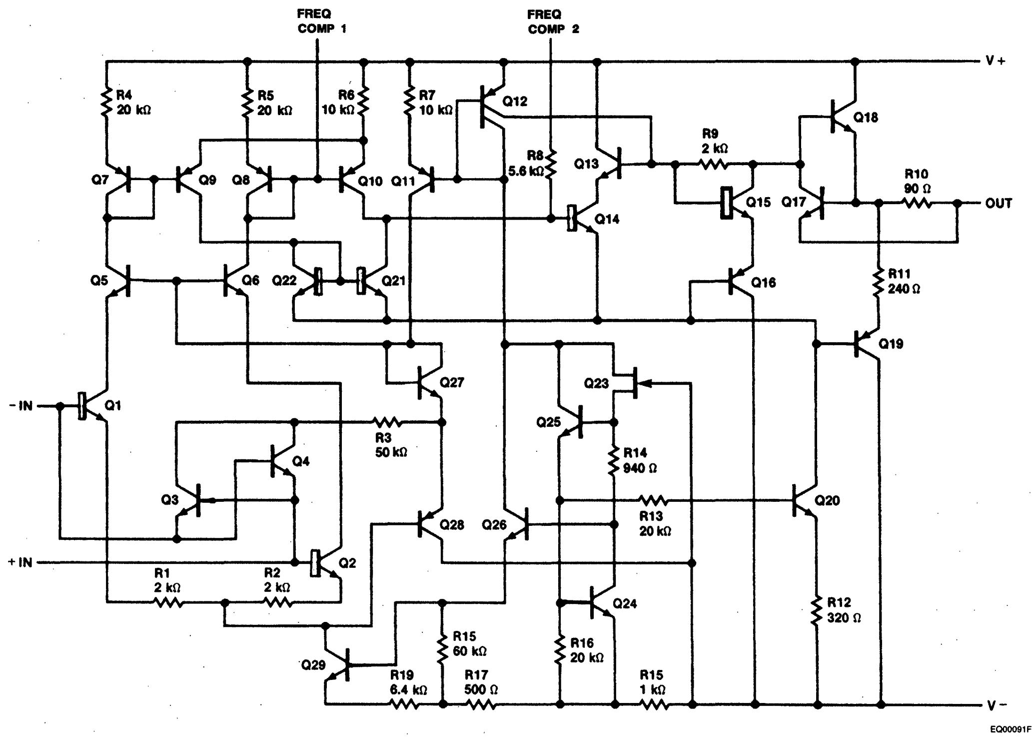
μA108AQB
Electrical Characteristics $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20V$, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0\ V$		0.5	mV	1	1
					1.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		5.0	μV/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		5.0	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0\ V$		0.2	nA	1	1
					0.4	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		2.5	pA/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		5.0	pA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0\ V$		1.9	nA	1	1
					3.0	nA	1	2,3
Z_I	Input Impedance[7]			30		MΩ	1	1
I_{CC}	Supply Current		$V_{CC} = \pm 20\ V$		0.6	mA	1	1,2
					0.8	mA	1	3
CMR	Common Mode Rejection		$V_{CC} = \pm 15\ V$, $V_{CM} = \pm 13.5\ V$, $R_S = 50\ \Omega$	96		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]		$V_{CC} = \pm 15\ V$	±13.5		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, $R_S = 50\ \Omega$		16	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current		$V_{CC} = \pm 15\ V$		15	mA	3	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L = 10\ k\Omega$	80		V/mV	1	4
				40		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±13		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20\ V$, $V_I = 50\ mV$, $R_L = 2.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		1000	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20\ V$, $R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.05		V/μs	3	9, 10, 11
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20\ V$, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20\ V$, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10104 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 2[5]

μA108QB Super Beta Operational Amplifier

Aerospace and Defense Data Sheet

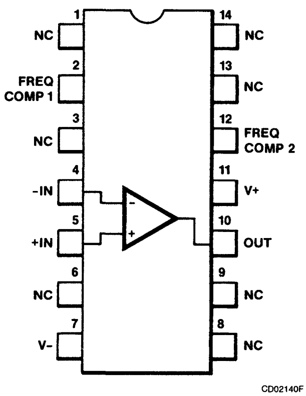
Linear Products

Description

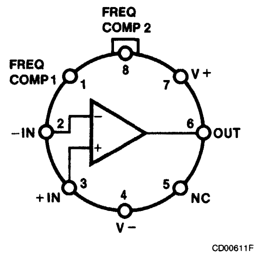
The μA108QB Super Beta Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low noise, low input offsets, and low temperature drifts are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA108QB is specially selected for low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.[6]

- **Guaranteed Low Input Offset Characteristics**
- **High Input Impedance**
- **Low Offset Current**
- **Low Bias Current**
- **Operation Over Wide Supply Range**

Connection Diagram 14-Lead DIP (Top View)

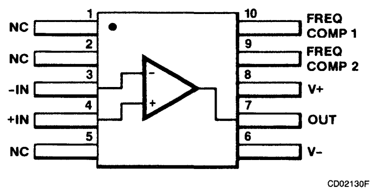


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA108DMQB	CA	D-1 14-Lead DIP
μA108HMQB	GC	A-1 8-Lead Can
μA108FMQB	HA	F-4 10-Lead Flatpak

JAN Product Available

10104	BCA	D-1 14-Lead DIP
10104	BCC	D-1 14-Lead DIP
10104	BGA	A-1 8-Lead Can
10104	BGC	A-1 8-Lead Can
10104	BHA	F-4 10-Lead Flatpak
10104	BHB	F-4 10-Lead Flatpak

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite
Differential Input Current[12]	±10 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

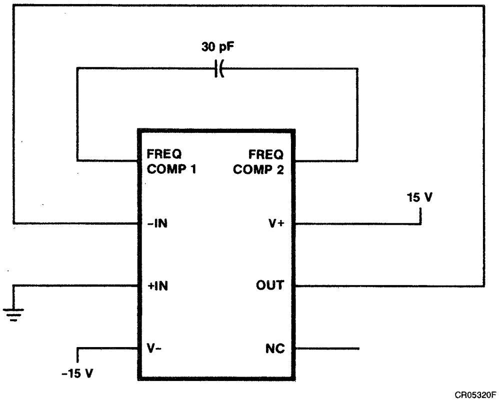
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2[(V_T/I_{IB}) + 1001R_E(10^{-6})]$, $V_T = 26$ mV at 25°C, $R_E = 1700\ \Omega$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.
12. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless adequate limiting resistance is used.

μA108QB
Electrical Characteristics $\pm 5.0 \leqslant V_{CC} \leqslant \pm 20$ V, unless otherwise specified.

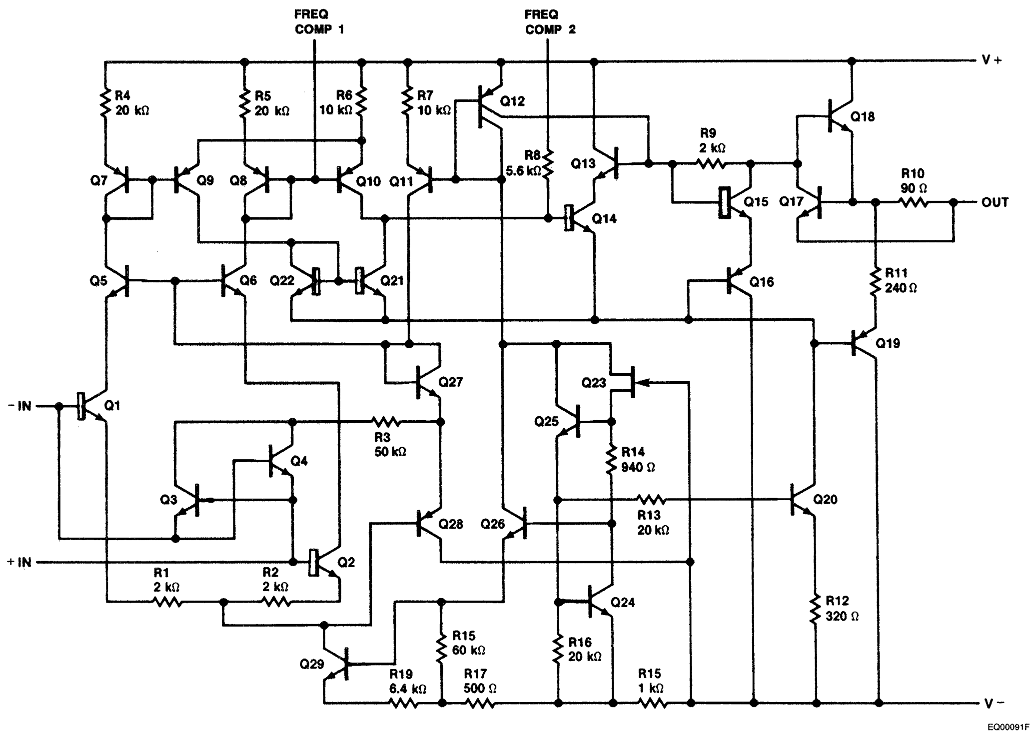
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		2.0	mV	1	1
					3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		15	μV/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		15	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		0.2	nA	1	1
					0.4	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		2.5	pA/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		5.0	pA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		1.9	nA	1	1
					3.0	nA	1	2,3
Z_I	Input Impedance[7]			30		MΩ	1	1
I_{CC}	Supply Current		$V_{CC} = \pm 20$ V		0.6	mA	1	1,2
					0.8	mA	1	3
CMR	Common Mode Rejection		$V_{CC} = \pm 15$ V, $V_{CM} = \pm 13.5$ V, $R_S = 50\ \Omega$	85		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]		$V_{CC} = \pm 15$ V	±13.5		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20$ V, $R_S = 50\ \Omega$		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current		$V_{CC} = \pm 15$ V		15	mA	3	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15$ V, $V_O = \pm 10$ V, $R_L = 10$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15$ V, $R_L = 10$ kΩ	±13		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		1000	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$	0.05		V/μs	3	9, 10, 11
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit

(38510/10104 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

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μA110QB Voltage Follower

MIL-STD-883
July 1986—Rev 1[5]

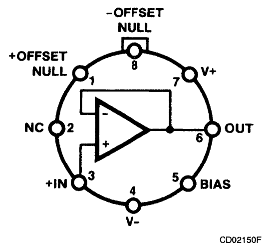
Aerospace and Defense Data Sheet
Linear Products

Description

The μA110QB is a monolithic operational amplifier internally connected as a unity gain non-inverting amplifier. It is constructed using the Fairchild Planar Epitaxial process. This circuit is ideal for such applications as fast sample-and-hold circuits, active filters, or as general purpose buffers. Super beta transistors are used interchangeably with the μA101QB and the μA741QB in voltage follower applications. It features low, offset voltage, drift, bias current, noise; plus high speed and a wide operating voltage range.[6]

- **High Slew Rate**
- **Low Input Current**
- **Internally Compensated**
- **Plug-In Replacement For Both The μA101QB And μA741QB Voltage Follower Applications**
- **Wide Range Of Supply Voltage**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 Connected case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA110HMQB	GC	A-1 8-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
Can	330 mW
Supply Voltage	±18 V
Input Voltage[9]	±15 V
Short Circuit Duration[10]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

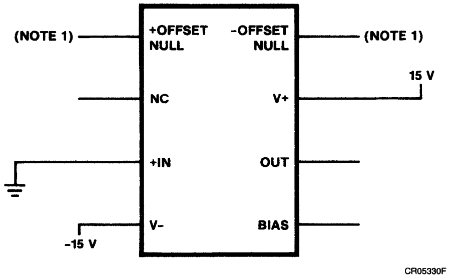
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. BW is guaranteed by t_r: $BW = 0.35/t_r$
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate at 150°C/CW.
9. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
10. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature. It is necessary to insert a resistor greater than 2.0 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

μA110QB
Electrical Characteristics $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 18\ V$, unless otherwise specified.

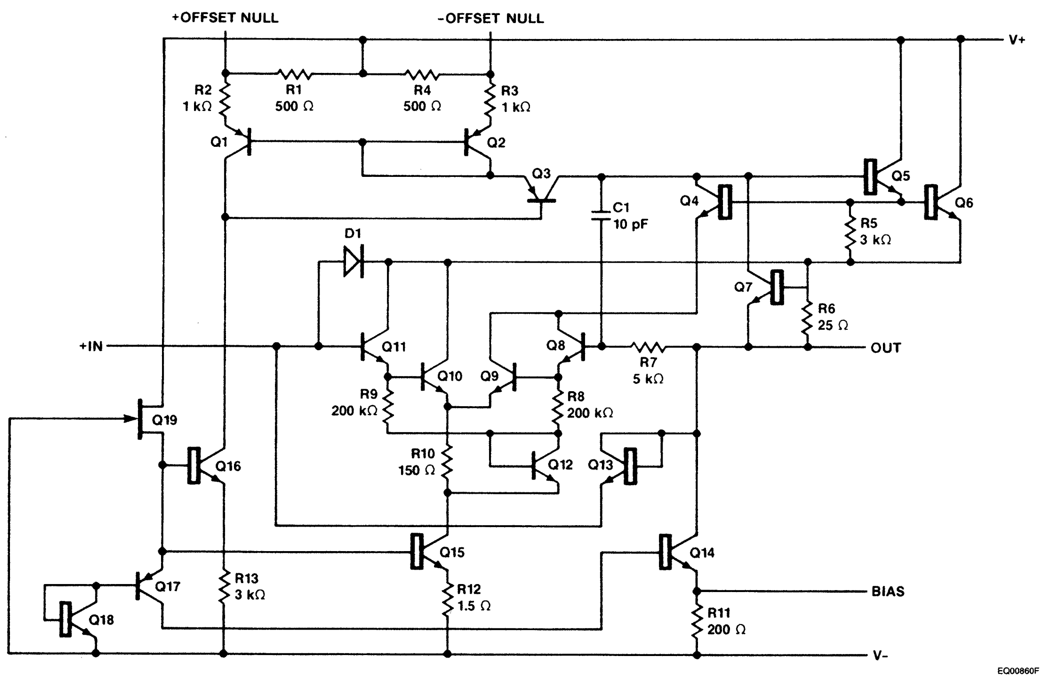
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$V_{CM} = 0\ V$		4.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Offset Voltage Temperature Drift		$25°C \leqslant T_A \leqslant 125°C$		15	μV/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		15	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		$V_{CC} = \pm 18\ V$	7.5		mV	1	1,2,3
I_{IB}	Input Bias Current		$V_{CM} = 0\ V$		3.0	nA	1	1
					10	nA	1	2,3
Z_I	Input Impedance		$V_{CC} = \pm 18\ V$	10000		MΩ	1	1
I_{CC}	Supply Current		$V_{CC} = \pm 18\ V$		5.5	mA	1	1
					4.0	mA	1	2
					8.0	mA	1	3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 18\ V$		316	μV/V	1	1,2,3
I_{OS} +	Positive Output Short Circuit Current		$V_{CC} = \pm 18\ V$, $V_I = +15\ V$	10	35	mA	4	1,2,3
I_{OS} −	Negative Output Short Circuit Current		$V_{CC} = \pm 18\ V$, $V_I = -15\ V$	1.5	10	mA	4	1,2,3
R_O	Output Resistance		$V_{CC} = \pm 18\ V$		2.5	Ω	1	1
					4.0	Ω	1	2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L = 8.0\ k\Omega$	0.999		V/V	1	4,5,6
			$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L = 10\ k\Omega$	0.999		V/V	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$, $R_L = 10\ k\Omega$	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 18\ V$		60	ns	4	9, 10, 11
$TR(o_s)$		Overshoot			50	%	4	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 18\ V$	15		V/μs	4	9, 10, 11
BW	Bandwidth[7]		$V_{CC} = \pm 18\ V$	6.0		MHz	4	9, 10, 11

Primary Burn-In Circuit



Note
1. A 30 pF connected between the two offset null leads is optional.

Equivalent Circuit



FAIRCHILD
A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA124QB Quad Operational Amplifier

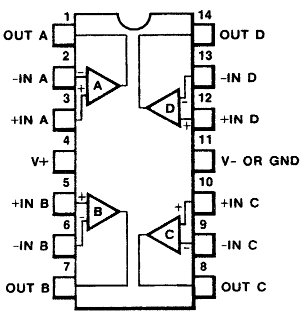
Aerospace and Defense Data Sheet
Linear Products

Description

The μA124QB Quad Operational Amplifier consists of four independent high gain, internal frequency-compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. It is constructed using the Fairchild Planar Epitaxial process. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.[6]

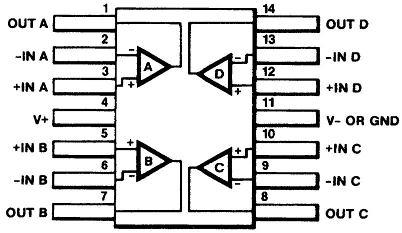
- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**
- **Output Voltage Can Swing To Ground Or Negative Supply**
- **Four Internally Compensated Operational Amplifiers In A Single Package**
- **Wide Power Supply Range**
- **Power Drain Suitable For Battery Operation**

Connection Diagram 14-Lead DIP (Top View)



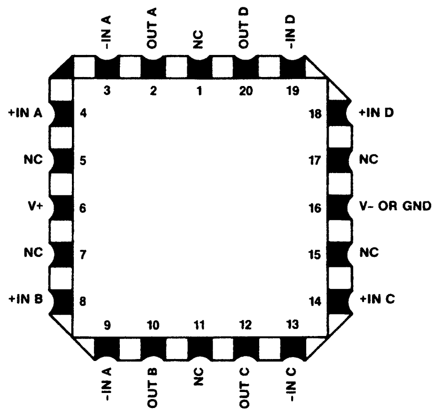
CD00661F

Connection Diagram 14-Lead Flatpak (Top View)



CD02090F

Connection Diagram 20-Terminal CCP (Top View)



CD02100F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA124DMQB	CA	D-1 14-Lead DIP
μA124FMQB	AA	F-1 14-Lead Flatpak
μA124LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

11005	BCA	D-1 14-Lead DIP
11005	BCB	D-1 14-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
Flatpak	350 mW
DIP and CCP	400 mW
Supply Voltage	±18 V or 36 V
Differential Input Voltage[9]	36 V
Input Voltage[10]	−0.3 V to +36 V
Input Current	10 mA
Short Circuit Duration[11]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

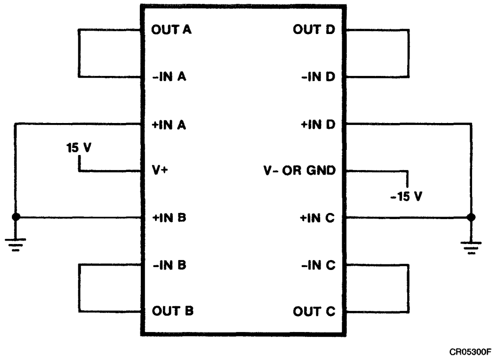
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} is guaranteed by the V_{IO} test.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Flatpak and 120°C/W for the DIP and CCP.
9. The differential input voltage shall not exceed the supply voltage.
10. For supply voltages less than 36 V, the absolute maximum input voltage is equal to the supply voltage. The input common mode voltage or either signal input voltage should not be allowed to go negative more than 0.3 V.
11. Short circuit may be to ground or negative supply. Rating applies to 125°C case temperature or 75°C ambient temperature. Short circuits from the output to V+ can cause excessive heating and eventual destruction. No more than one amplifier should be shorted at the same time as the maximum junction temperature will be exceeded.

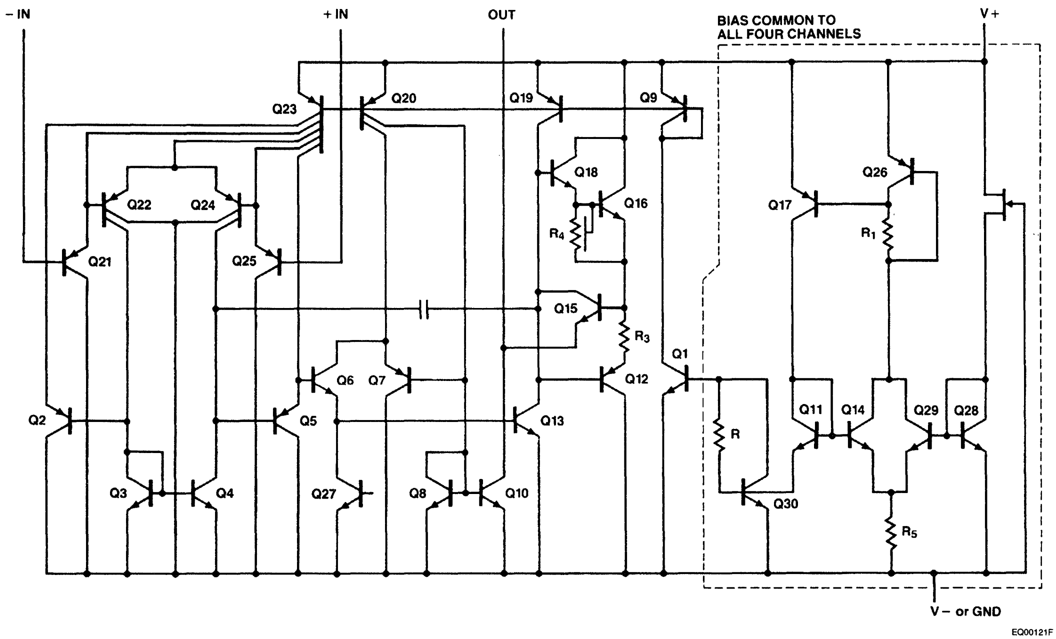
μA124QB
Electrical Characteristics V+ = 5.0 V, V− = 0 V, unless otherwise specified.

Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		5.0 V ≤ V+ ≤ 30 V, R_S = 10 kΩ, V_O = 1.4 V	0 V ≤ V_{CM} ≤ V+ −1.5 V		5.0	mV	1	1
				0 V ≤ V_{CM} ≤ V+ −2.0 V		7.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			30	μV/°C	4	2
			−55°C ≤ T_A ≤ 25°C			30	μV/°C	4	3
I_{IO}	Input Offset Current		V_{CM} = 0 V			30	nA	1	1
						100	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			400	pA/°C	4	2
			−55°C ≤ T_A ≤ +25°C			700	pA/°C	4	3
I_{IB}	Input Bias Current		V_{CM} = 0 V		−150		nA	1	1
					−300		nA	1	2,3
I_{CC}	Supply Current (Total)		R_L = ∞ on all Op Amps	V+ = 5.0 V		1.2	mA	1	1,2,3
				V+ = 30 V		3.0	mA	1	1,2,3
CMR	Common Mode Rejection		V+ = 30 V, R_S = 50 Ω	V_{CM} = 28.5 V	70		dB	1	1
				V_{CM} = 28 V	68		dB	1	2,3
V_{IR}	Input Voltage Range[7]		5.0 V ≤ V+ ≤ 30 V, V_O = 1.4 V		0	V+ −1.5	V	1	1
					0	V+ −2.0	V	1	2,3
PSRR	Power Supply Rejection Ratio		5.0 V ≤ V+ ≤ 32 V, R_S = 50 Ω			562	μV/V	1	1
I_{OS}	Output Short Circuit Current				−70		mA	1	1,2,3
I_{OH}	Output Source Current		V+ = 15 V, V_O = GND			−20	mA	1	1,2,3
						−10	mA	1	2,3
I_{OL}	Output Sink Current		V_O = 200 mV		12		μA	1	1
			V+ = 15 V, V_O = 15 V		10		mA	1	1
					5.0		mA	1	2,3
A_{VS}	Large Signal Voltage Gain		V+ = 15 V, R_L = 2.0 kΩ		50		V/mV	1	4
					25		V/mV	1	5,6
V_{OH}	High Level Output Voltage		V+ = 30 V	R_L = 10 kΩ	27		V	1	4,5,6
				R_L = 2.0 kΩ	26		V	1	4,5,6
V_{OL}	Low Level Output Voltage		R_L = 10 kΩ			20	mV	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	V+ = 30 V, V_I = 50 mV, R_L = 2.0 kΩ, C_L = 100pF, A_V = 1.0			1.0	μs	3	9,10,11
$TR(o_S)$		Overshoot				50	%	3	9,10,11
SR	Slew Rate		V+ = 30 V, R_L = 2.0 kΩ, A_V = 1.0		0.1		V/μs	3	9,10,11
CS	Channel Separation		V+ = 30 V		80		dB	4	9
N_I (BB)	Noise Broadband		V_{CC} = ±15 V, R_S = 50 Ω			15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		V_{CC} = ±15 V, R_S = 20 kΩ			50	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/11005 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of circuit shown)



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MIL-STD-883
July 1986—Rev 1[5]

μA148QB Quad Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

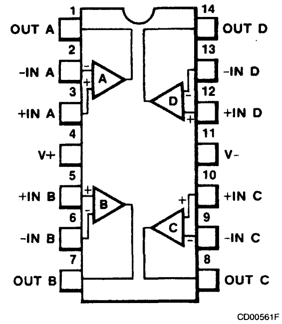
Description

The μA148QB is a true quad μA741QB. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar μA741QB Operational Amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single μA741QB type op amp.

Other features include input offset currents and input bias currents which are much less than those of a standard μA741QB. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.[6]

- **μA741QB Op Amp Operating Characteristics**
- **Low Supply Current Drain**
- **Class AB Output Stage — No Crossover Distortion**
- **Lead Compatible With The μA124QB**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Low Input Bias Current**
- **Gain Bandwidth Product For μA148QB (Unity Gain) — 1 MHz Typical**
- **High Degree Of Isolation Between Amplifiers**
- **Overload Protection For Inputs And Outputs**

Connection Diagram
14-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA148DMQB	CA	D-1 14-Lead DIP

JAN Product Available

11001	BCA	D-1 14-Lead DIP
11001	BCB	D-1 14-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage[10]	±30 V
Input Voltage[11]	±20 V
Input Current	10 mA
Short Circuit Duration[12]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

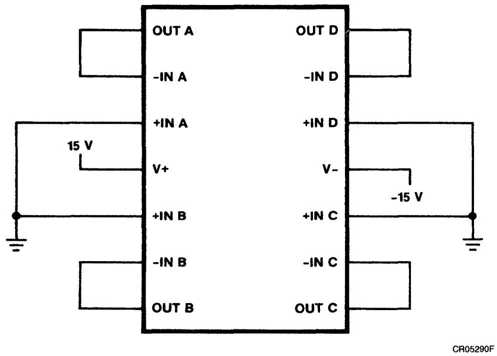
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C and 19 mV at −55°C.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
10. The differential input voltage shall not exceed the supply voltage.
11. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature. No more than one amplifier should be shorted simultaneously as the maximum junction temperature will be exceeded.

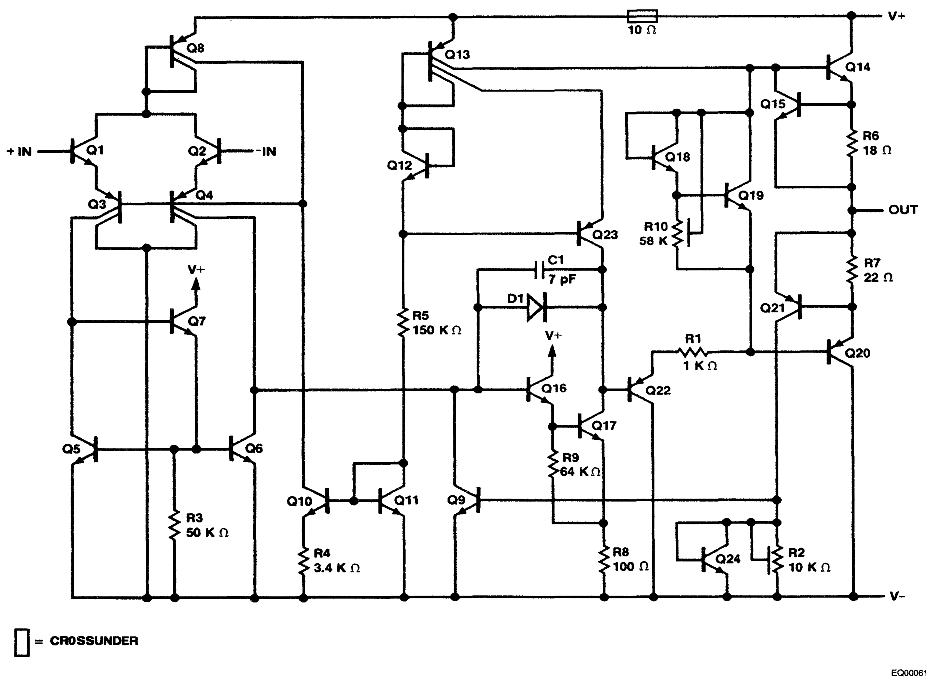
μA148QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 10$ kΩ, $V_{CM} = 0$ V		5.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		25	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		25	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		25	nA	1	1
					75	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		200	pA/°C	4	2
			$-55°C \leq T_A \leq +25°C$		400	pA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		100	nA	1	1
					325	nA	1	2,3
Z_I	Input Impedance[7]			0.8		MΩ	1	1
				0.4		MΩ	1	2
I_{CC}	Supply Current (Total)				3.6	mA	1	1,2
					4.2	mA	1	3
CMR	Common Mode Rejection		$V_{CM} = \pm 12$ V, $R_S = 50$ Ω	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]			±12		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0 \text{ V} \leq V_{CC} \leq \pm 22$ V, $R_S = 50$ Ω		142	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				55	mA	1	1,2
					75	mA	1	3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
			$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		1.0	μs	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$	0.2		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20$ V	80		dB	4	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/11001 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of Circuit)



MIL-STD-883
July 1986—Rev 1[5]

μA1558QB
Dual Internally Compensated Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

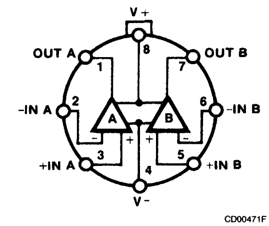
Description

The μA1558QB is a monolithic pair of internally compensated, high performance amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA1558QB ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.

The μA1558QB is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll off insures stability in closed loop applications.[6]

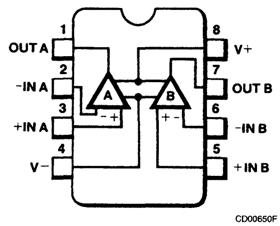
- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Large Common Mode And Differential Voltage Range**
- **Low Power Consumption**
- **No Latch-Up**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA1558HMQB	GC	A-1 8-Lead Can
μA1558RMQB	PA	D-4 8-Lead DIP

JAN Product Available

10108	BGA	A-1 8-Lead Can
10108	BGC	A-1 8-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can	350 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[12]	±20 V
Short Circuit Duration[13]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

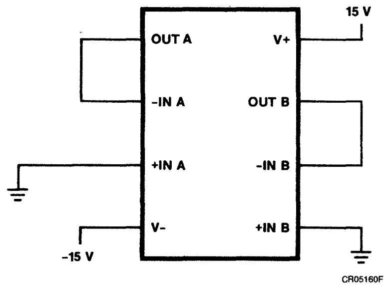
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. BW is guaranteed by t_r: $BW = 0.35/t_r$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Can and 120°C/W for the DIP.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

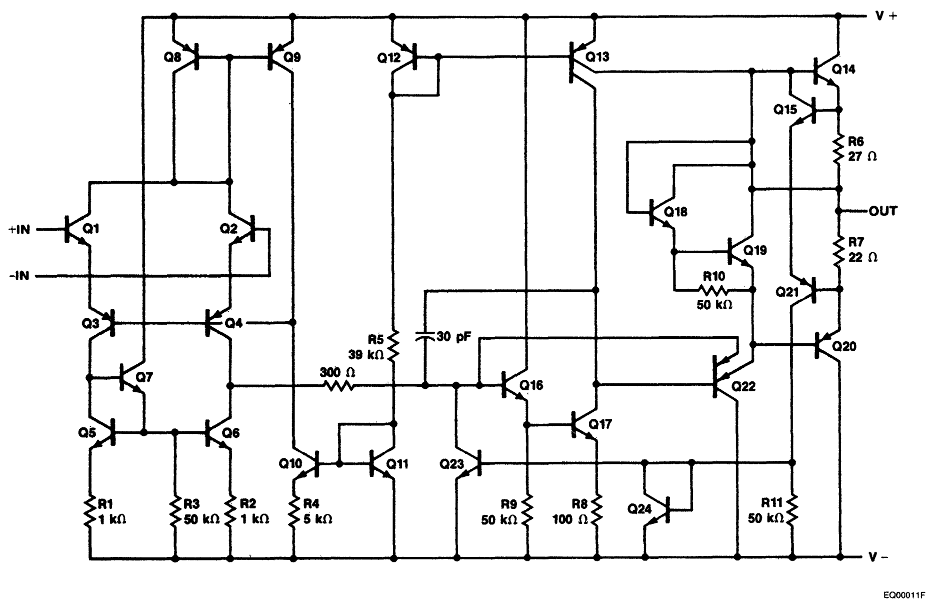
μA1558QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 10$ kΩ, $V_{CM} = 0$ V		5.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		15	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		15	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		200	nA	1	1
					500	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		1.0	nA/°C	4	2
			$-55°C \leq T_A \leq +25°C$		1.0	nA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		340	nA	1	1
					1500	nA	1	2,3
Z_I	Input Impedance[7]			0.3		MΩ	1	1
				0.2		MΩ	1	2
I_{CC}	Supply Current (Total)				5.6	mA	1	1
					5.0	mA	1	2
					6.6	mA	1	3
P_c	Power Consumption (Total)[8]				150	mW	1	1
CMR	Common Mode Rejection		$V_{CM} = \pm 12$ V, $R_S = 50$ Ω	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]			±12		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\text{ V} \leq V_{CC} \leq \pm 22$ V, $R_S = 50$ Ω		150	μV/V	1	1,2,3,
I_{OS}	Output Short Circuit Current				60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
			$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[10]			0.437		MHz	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$	0.3		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20$ V	80		dB	1	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10108 may be used by FSC as an alternate)



Equivalent Circuit (1/2 of circuit)



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MIL-STD-883
July 1986—Rev 1[5]

μA2101AQB Dual General Purpose Operational Amplifier

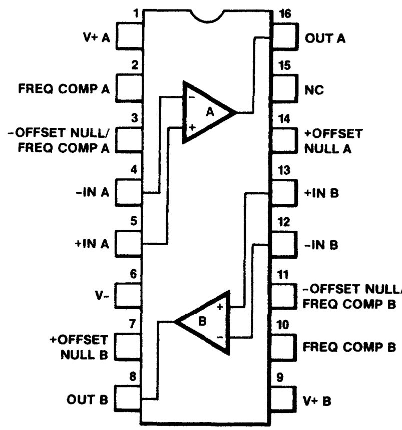
Aerospace and Defense Data Sheet
Linear Products

Description

The μA2101AQB is a dual general purpose monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. This integrated circuit is intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers, and sample-and-hold circuits is improved due to the low drift and low bias currents. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of latch-up coupled with internal short circuit protection make the μA2101AQB virtually foolproof.[6]

- **Low Offset Current And Voltage**
- **Low Offset Current Drift**
- **Low Bias Current**
- **Short Circuit Protected**
- **Low Power Consumption**

Connection Diagram 16-Lead DIP (Top View)



CD02010F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA2101ADMQB	EA	D-2 16-Lead DIP

JAN Product Available

10105	BEA	D-2 16-Lead DIP
10105	BEB	D-2 16-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} is guaranteed by the CMR test.
8. BW is guaranteed by t_r: BW = $0.35/t_r$.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA2101AQB

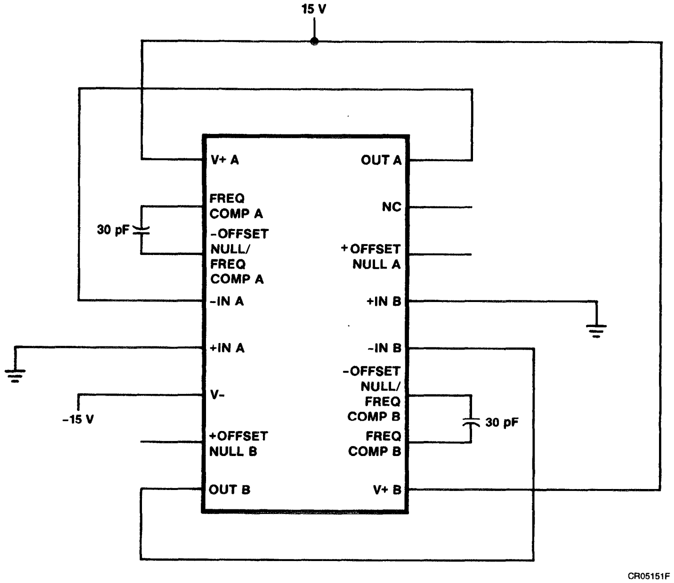
Electrical Characteristics $\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 20\ V$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = \pm 15\ V$		2.0	mV	1	1
				3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		15	μV/°C	2	2
		$-55°C \leqslant T_A \leqslant +25°C$		18	μV/°C	2	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range	$V_{CC} = \pm 20\ V$	4.0		mV	1	1,2,3
I_{IO}	Input Offset Current	$V_{CM} = \pm 15\ V$		10	nA	1	1,2
				20	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		0.1	nA/°C	2	2
		$-55°C \leqslant T_A \leqslant +25°C$		0.2	nA/°C	2	3
I_{IB}	Input Bias Current	$V_{CM} = \pm 15\ V$		75	nA	1	1,2
				100	nA	1	3
I_{CC}	Supply Current (Total)	$V_{CC} = \pm 15\ V$		6.0	mA	1	1
				5.0	mA	1	2
				7.0	mA	1	3
CMR	Common Mode Rejection	$V_{CC} = \pm 20\ V$, $V_{CM} = \pm 15\ V$, $R_S = 50\ \Omega$	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[7]	$V_{CC} = \pm 20\ V$	±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	V+ = 10 V, V− = −20 V to V+ = 20 V, V− = 10 V, $R_S = 50\ \Omega$		50	μV/V	1	1
				100	μV/V	1	2,3
I_{OS}	Output Short Circuit Current	$V_{CC} = \pm 15\ V$, $t \leqslant 25$ ms		60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 20\ V$, $V_O = \pm 15\ V$, $R_L = 2.0\ k\Omega$	50		V/mV	1	4
			25		V/mV	1	5,6
		$V_{CC} = \pm 5.0\ V$, $V_O = \pm 2.0\ V$, $R_L = 2.0\ k\Omega$	10		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 20\ V$, $R_L = 10\ k\Omega$	±16		V	1	4,5,6
		$R_L = 2.0\ k\Omega$	±15		V	1	4,5,6
$TR(t_r)$	Transient Response — Rise Time	$V_I = 50$ mV, $R_L = 2.0\ k\Omega$, $C_L = 100$ pF, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$	Transient Response — Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[8]		0.437		MHz	3	9, 10, 11
SR	Slew Rate	$R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.3		V/μs	3	9, 10
			0.2		V/μs	3	11
CS	Channel Separation	$V_{CC} = \pm 20\ V$	80		dB	1	9
N_I (BB)	Noise Broadband	BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn	BW = 5.0 kHz		80	μV_{pk}	4	9

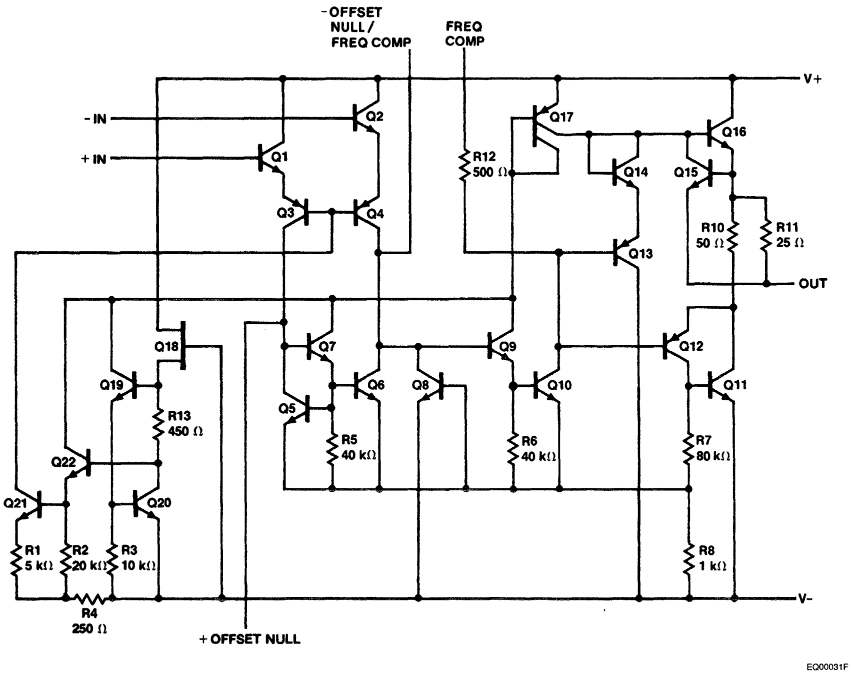
14

Primary Burn-In Circuit

(38510/10105 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA2101QB Dual General Purpose Operational Amplifier

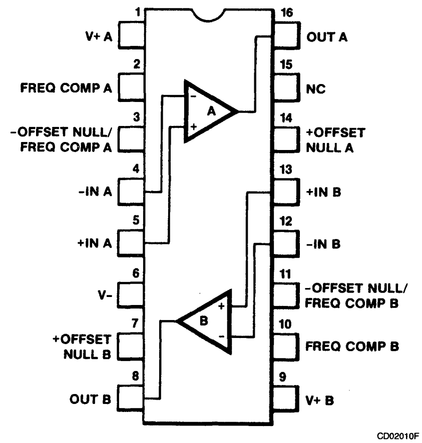
Aerospace and Defense Data Sheet
Linear Products

Description

The μA2101QB is a dual general purpose monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. This integrated circuit is intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers, and sample-and-hold circuits is improved due to the low drift and low bias currents. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of latch-up coupled with internal short circuit protection make the μA2101QB virtually foolproof.[6]

- **Low Offset Current And Voltage**
- **Low Offset Current Drift**
- **Low Bias Current**
- **Short Circuit Protected**
- **Low Power Consumption**

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA2101DMQB	EA	D-2 16-Lead DIP

JAN Product Available

10105	BEA	D-2 16-Lead DIP
10105	BEB	D-2 16-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

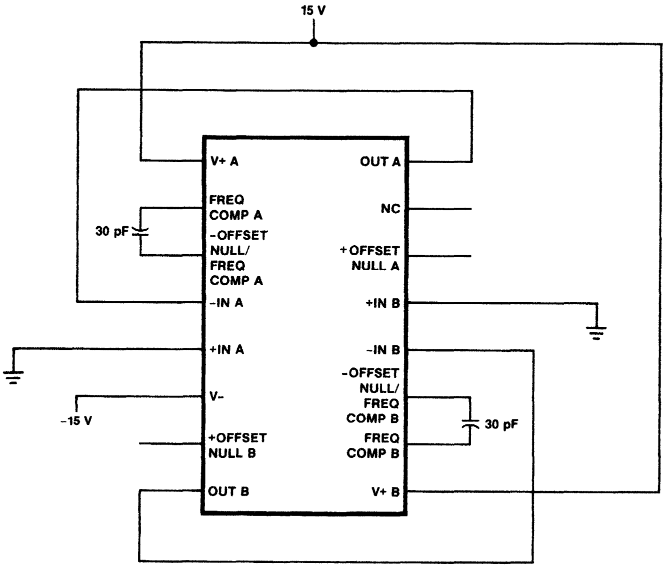
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} is guaranteed by the CMR test.
8. BW is guaranteed by t_r: $BW = 0.35/t_r$.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA2101QB
Electrical Characteristics ±5.0 V ≤ V_{CC} ≤ ±20 V, unless otherwise specified.

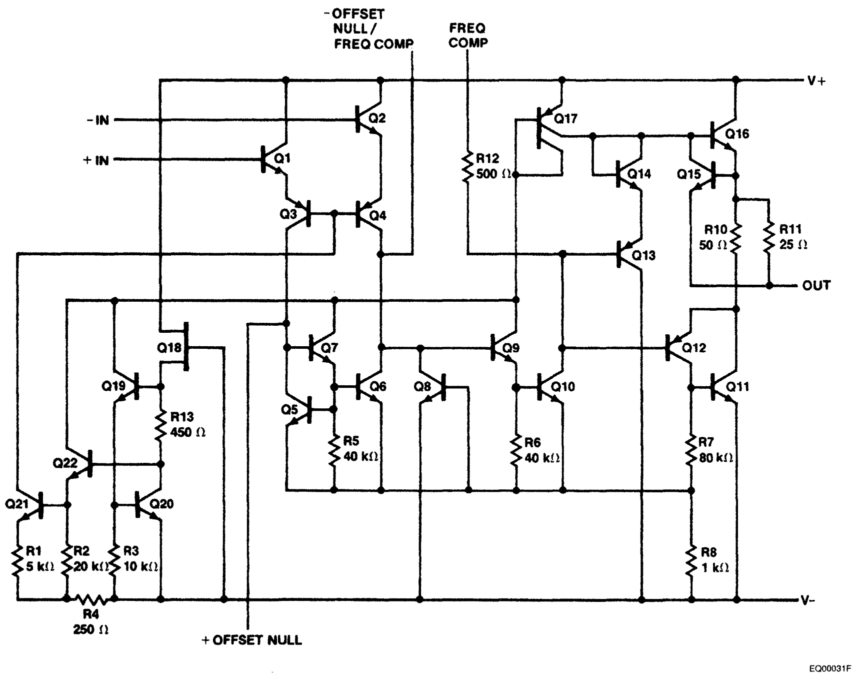
Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		R_S = 50 Ω, V_{CM} = ±15 V			4.0	mV	1	1
						5.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			15	μV/°C	4	2
			−55°C ≤ T_A ≤ +25°C			18	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		V_{CC} = ±20 V		4.0		mV	1	1,2,3
I_{IO}	Input Offset Current		V_{CM} = ±15 V			100	nA	1	1,2
						200	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			0.1	nA/°C	4	2
			−55°C ≤ T_A ≤ +25°C			0.2	nA/°C	4	3
I_{IB}	Input Bias Current		V_{CM} = ±15 V			200	nA	1	1,2
						300	nA	1	3
I_{CC}	Supply Current (Total)		V_{CC} = ±15 V			6.0	mA	1	1
						5.0	mA	1	2
						7.0	mA	1	3
CMR	Common Mode Rejection		V_{CC} = ±20 V, V_{CM} = ±15 V R_S = 50 Ω		75		dB	1	1,2,3
V_{IR}	Input Voltage Range[7]		V_{CC} = ±20 V		±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 10 V, V− = −20 V to V+ = 20 V, V− = 10 V, R_S = 50 Ω			100	μV/V	1	1
						178	μV/V	1	2,3
I_{OS}	Output Short Circuit Current		V_{CC} = ±15 V, t ≤ 25 ms			70	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		V_{CC} = ±20 V, V_O = ±15 V, R_L = 2.0 kΩ		50		V/mV	1	4
					25		V/mV	1	5,6
			V_{CC} = ±5.0 V, V_O = ±2.0 V, R_L = 2.0 kΩ		10		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		V_{CC} = ±20 V	R_L = 10 kΩ	±16		V	1	4,5,6
				R_L = 2.0 kΩ	±15		V	1	4,5,6
TR(t_r)	Transient Response	Rise Time	V_I = 50 mV, R_L = 2.0 kΩ, C_L = 100 pF, A_V = 1.0			800	ns	3	9, 10, 11
TR(o_s)		Overshoot				25	%	3	9, 10, 11
BW	Bandwidth[8]				0.437		MHz	3	9, 10, 11
SR	Slew Rate		R_L = 2.0 kΩ, A_V = 1.0		0.3		V/μs	3	9, 10
					0.2		V/μs	3	11
CS	Channel Separation		V_{CC} = ±20 V		80		dB	1	9
N_I (BB)	Noise Broadband		BW = 5.0 kHz			15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		BW = 5.0 kHz			80	μV_{pk}	4	9

Primary Burn-In Circuit

(38510/10105 may be used by FSC as an alternate)



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA2108AQB Dual Super Beta Operational Amplifier

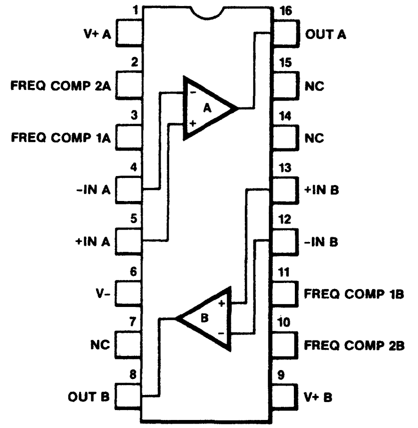
Aerospace and Defense Data Sheet
Linear Products

Description

The μA2108AQB Dual Super Beta Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low noise, low input offsets, and low temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA2108AQB is specially selected for low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.[6]

- **Guaranteed Low Input Offset Characteristics**
- **High Input Impedance**
- **Low Offset Current**
- **Low Bias Current**
- **Operation Over Wide Supply Range**

Connection Diagram 16-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA2108ADMQB	EC	D-2 16-Lead DIP

JAN Product Available

10106	BEC	D-2 16-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite
Differential Input Current[12]	±10 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

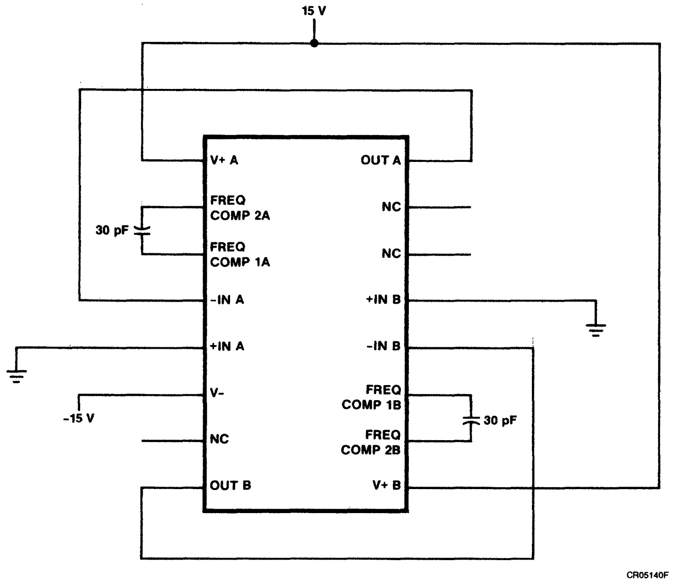
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2[(V_T/I_{IB}) + 1001R_E(10^{-6})]$, $V_T = 26$ mV at 25°C, $R_E = 1700\ \Omega$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.
12. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless adequate limiting resistance is used.

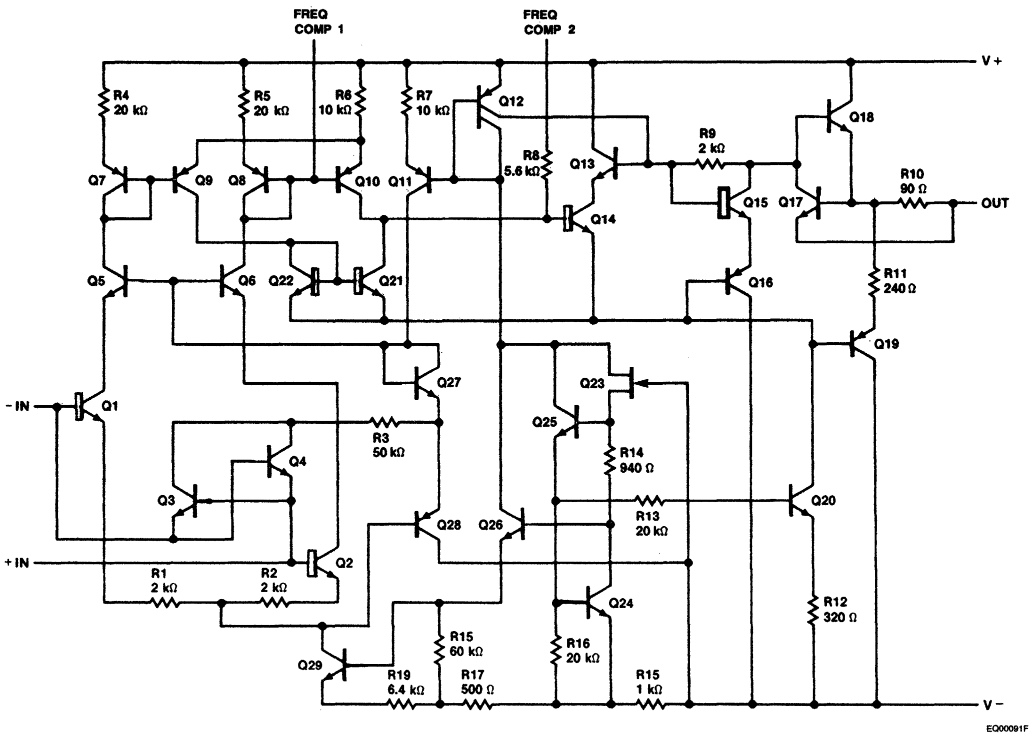
μA2108AQB
Electrical Characteristics $V_{CC} = \pm 5.0$ V and ± 20 V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $-15\ V \leq V_{CM} \leq +15\ V$		0.5	mV	1	1
					1.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		5.0	μV/°C	2	2
			$-55°C \leq T_A \leq +25°C$		5.0	μV/°C	2	3
I_{IO}	Input Offset Current		$-15\ V \leq V_{CM} \leq +15\ V$		0.2	nA	1	1
					0.4	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		2.5	pA/°C	2	2
			$-55°C \leq T_A \leq +25°C$		5.0	pA/°C	2	3
I_{IB}	Input Bias Current		$-15\ V \leq V_{CM} \leq +15\ V$		1.9	nA	1	1,2
					3.0	nA	1	3
Z_I	Input Impedance[7]			30		MΩ	1	1
I_{CC}	Supply Current (Total)		$V_{CC} = \pm 15$ V		1.2	mA	1	1,2
					1.6	mA	1	3
CMR	Common Mode Rejection		$V_{CC} = \pm 20$ V, $V_{CM} = \pm 15$ V, $R_S = 50\ \Omega$	96		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]		$V_{CC} = \pm 20$ V	±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 10 V, V− = −20 V to V+ = 20 V, V− = −10 V, $R_S = 50\ \Omega$		16	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current		$V_{CC} = \pm 15$ V, $t \leq 25$ ms		15	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 20$ V, $V_O = \pm 15$ V, $R_L = 10\ k\Omega$	80		V/mV	1	4
				40		V/mV	1	5,6
			$V_{CC} = \pm 5.0$ V, $V_O = \pm 2.0$ V, $R_L = 10\ k\Omega$	20		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 20$ V, $R_L = 10\ k\Omega$	±16		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0\ k\Omega$, $C_L = 100$ pF, $A_V = 1.0$		1000	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.05		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20$ V	80		dB	1	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10106 may be used as an alternate)



Equivalent Circuit



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A Schlumberger Company

MIL-STD-883

July 1986—Rev 1[5]

μA2108QB Dual Super Beta Operational Amplifier

Aerospace and Defense Data Sheet

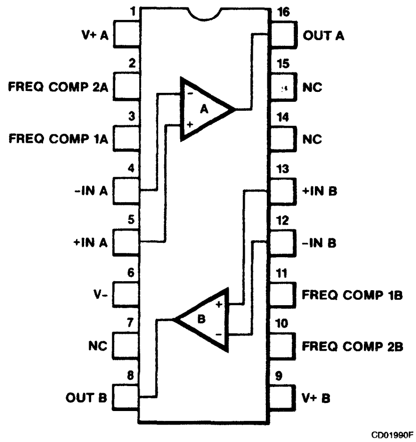
Linear Products

Description

The μA2108QB Dual Super Beta Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low noise, low input offsets, and low temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The μA2108QB is specially selected for low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.[6]

- **Guaranteed Low Input Offset Characteristics**
- **High Input Impedance**
- **Low Offset Current**
- **Low Bias Current**
- **Operation Over Wide Supply Range**

Connection Diagram 16-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA2108DMQB	EC	D-2 16-Lead DIP

JAN Product Available

10106	BEC	D-2 16-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[10]	±20 V
Short Circuit Duration[11]	Indefinite
Differential Input Current[12]	±10 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

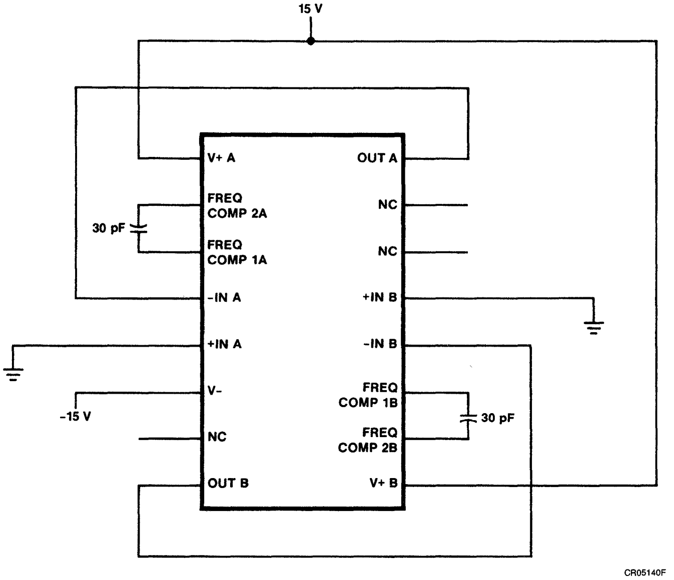
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Input impedance is guaranteed by I_{IB}: $Z_I = 2[(V_T/I_{IB}) + 1001R_E(10^{-6})]$, $V_T = 26$ mV at 25°C, $R_E = 1700\ \Omega$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
10. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.
12. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs unless adequate limiting resistance is used.

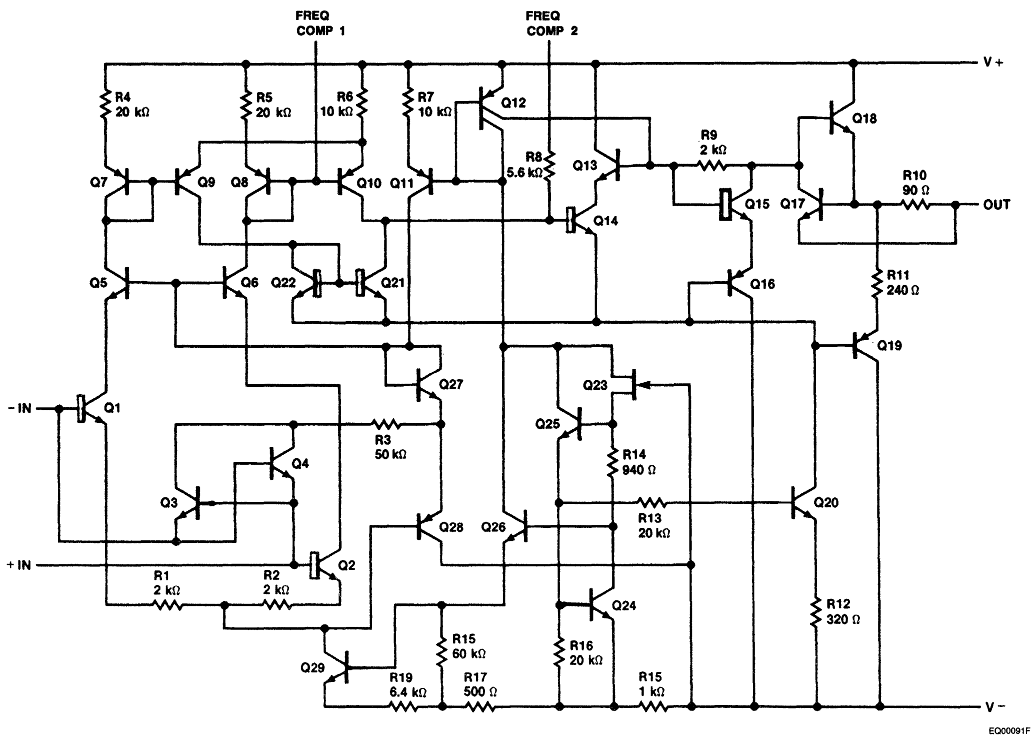
μA2108QB
Electrical Characteristics $\pm 5.0\ V \leq V_{CC} \leq \pm 20\ V$, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = \pm 15\ V$		2.0	mV	1	1
					3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		15	μV/°C	2	2
			$-55°C \leq T_A \leq +25°C$		15	μV/°C	2	3
I_{IO}	Input Offset Current		$V_{CM} = \pm 15\ V$		0.2	nA	1	1
					0.4	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		2.5	pA/°C	2	2
			$-55°C \leq T_A \leq +25°C$		2.5	pA/°C	2	3
I_{IB}	Input Bias Current		$V_{CM} = \pm 15\ V$		2.0	nA	1	1,2
					3.0	nA	1	3
Z_I	Input Impedance[7]			30		MΩ	1	1
I_{CC}	Supply Current (Total)		$V_{CC} = \pm 15\ V$		1.2	mA	1	1,2
					1.6	mA	1	3
CMR	Common Mode Rejection		$V_{CC} = \pm 20\ V$, $V_{CM} = \pm 15\ V$, $R_S = 50\ \Omega$	85		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]		$V_{CC} = \pm 20\ V$	±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$V+ = 10\ V$, $V- = -20\ V$ to $V+ = 20\ V$, $V- = -10\ V$, $R_S = 50\ \Omega$		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current		$V_{CC} = \pm 15\ V$, $t \leq 25\ ms$		20	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 20\ V$, $V_O = \pm 15\ V$, $R_L = 10\ k\Omega$	50		V/mV	1	4
				25		V/mV	1	5,6
			$V_{CC} = \pm 5.0\ V$, $V_O = \pm 2.0\ V$, $R_L = 10\ k\Omega$	12		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 20\ V$, $R_L = 10\ k\Omega$	±16		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20\ V$, $V_I = 50\ mV$, $R_L = 2.0\ k\Omega$, $C_L = 100\ pF$, $A_V = 1.0$		1000	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20\ V$, $R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.05		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20\ V$	70		dB	1	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20\ V$, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20\ V$, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10106 may be used as an alternate)



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA4136QB Quad Operational Amplifier

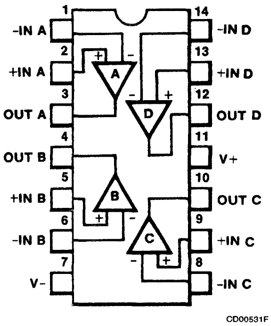
Aerospace and Defense Data Sheet
Linear Products

Description

The μA4136QB Monolithic Quad Operational Amplifier consists of four independent high gain, internal frequency-compensated operational amplifiers. It is constructed using the Fairchild Planar Epitaxial process. The specifically designed low noise input transistors allow the μA4136QB to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.[6]

- **High Unity Gain Bandwidth**
- **Continuous Short Circuit Protection**
- **No Frequency Compensation Required**
- **No Latch-Up**
- **Large Common Mode And Differential Voltage Ranges**
- **μA741QB Operational Amplifier Type Performance**
- **Parameter Tracking Over Temperature Range**
- **Gain And Phase Match Between Amplifiers**

Connection Diagram
14-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA4136DMQB	CA	D-1 14-Lead DIP

JAN Product Available

11004	BCA	D-1 14-Lead DIP
11004	BCB	D-1 14-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage[11]	±30 V
Input Voltage[12]	±20 V
Input Current	10 mA
Short Circuit Duration[13]	Indefinite

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at -55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
11. The differential input voltage shall not exceed the supply voltage.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature. No more than one amplifier should be shorted simultaneously as the maximum junction temperature will be exceeded.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

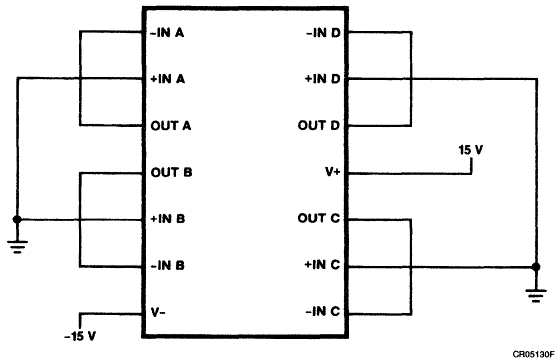
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at -55°C

Group C and D Endpoints: Group A, Subgroup 1

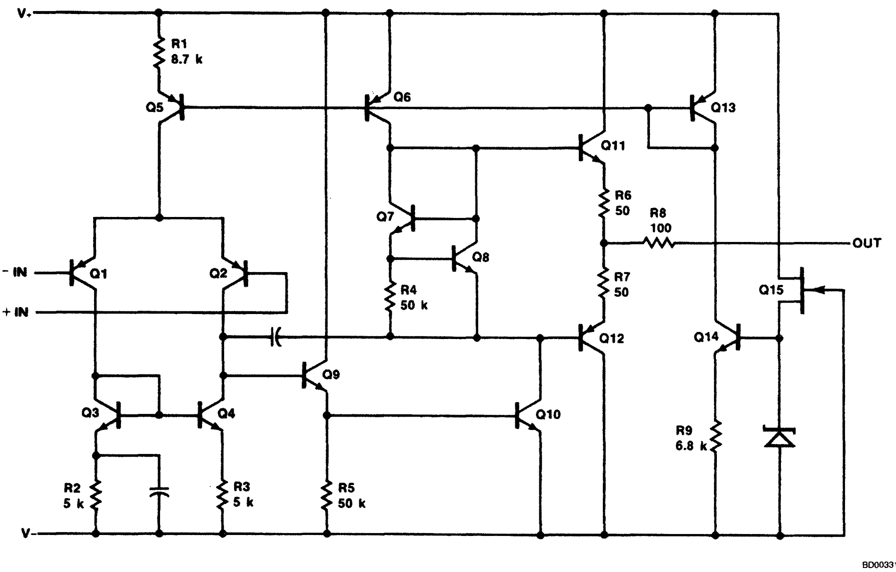
μA4136QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 10$ kΩ, $V_{CM} = 0$ V		5.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		25	μV/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		25	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		200	nA	1	1
					500	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		500	pA/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		1000	pA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		340	nA	1	1
					1500	nA	1	2,3
Z_I	Input Impedance[7]			0.15		MΩ	1	1
I_{CC}	Supply Current (Total)				11.3	mA	1	1
					10	mA	1	2
					13.3	mA	1	3
P_c	Power Consumption (Total)[8]				340	mW	1	1
					300	mW	1	2
					400	mW	1	3
CMR	Common Mode Rejection		$V_{CM} = \pm 12$ V, $R_S = 10$ kΩ	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]			±12		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 22$ V, $R_S = 10$ kΩ		150	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				80	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
			$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		0.3	μs	3	9, 10, 11
$TR(o_s)$		Overshoot			50	%	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$	0.6		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20$ V	80		dB	4	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V		5.0	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V		50	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/11004 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of circuit)



FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 1[5]

μA702QB Wideband DC Amplifier

Aerospace and Defense Data Sheet

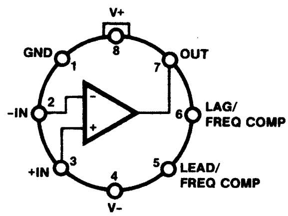
Linear Products

Description

The μA702QB is a monolithic DC amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for use as an operational amplifier in analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.[6]

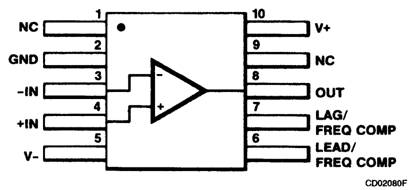
- Low Offset Voltage
- Low Offset Voltage Drift
- Wide Bandwidth
- High Slew Rate

Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA702HMQB	GC	A-1 8-Lead Can
μA702FMQB	HA	F-4 10-Lead Flatpak
μA702DMQB	CA	D-1 14-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	21 V
Differential Input Voltage	±5.0 V
Input Voltage[12]	+1.5 V to -6.0 V
Peak Output Current	50 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at -55°C.
8. P_{c1} is guaranteed by I_{CC1}: $P_{c1} = (12\ V)(I_{CC}) + (6.0\ V)(I_{CC1})$.
9. V_{IR} is guaranteed by the CMR test.
10. P_{c2} is guaranteed by I_{CC2}: $P_{c2} = (6.0\ V)(I_{CC2}) + (3.0\ V)(I_{CC2})$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltage of 21 V.

Transient Response Test Circuits

Figure 1 Unity-Gain Amplifier (Lag Compensation)

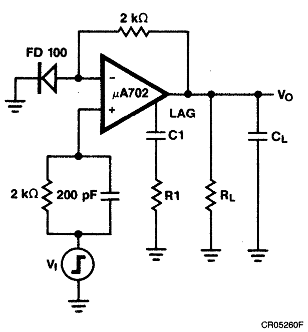
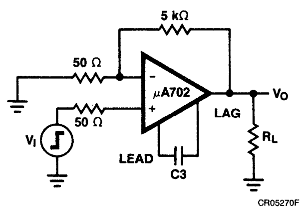


Figure 2 X100 Amplifier (Lead Compensation)



μA702QB
Electrical Characteristics V+ = 12 V, V− = −6.0 V, unless otherwise specified.

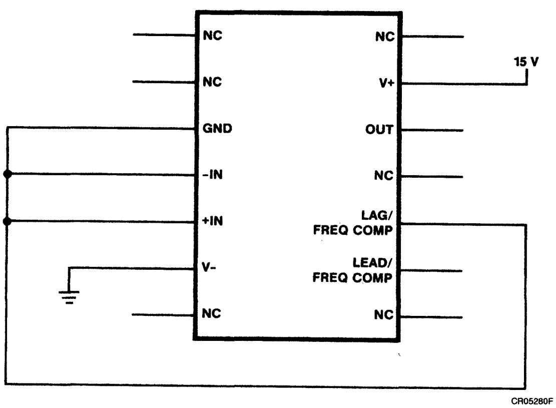
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		2.0	mV	1	1
					3.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		10	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		10	μV/°C	4	3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		500	nA	1	1,2
					1500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		5.0	nA/°C	4	2
			$-55°C \leq T_A \leq +25°C$		16	nA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		3.2	μA	1	1
					10	μA	1	2,3
Z_I	Input Impedance[7]			16		kΩ	1	1
I_{CC1}	Supply Current		$V_O = 0$ V		6.7	mA	1	1,2
					7.5	mA	1	3
P_{c1}	Power Consumption[8]		$V_O = 0$ V		121	mW	1	1,2
					135	mW	1	3
CMR	Common Mode Rejection		$-4.0\ V \leq V_{CM} \leq 0.5$ V, $R_S = 2.0$ kΩ	80		dB	1	1
				70		dB	1	2,3
V_{IR}	Input Voltage Range[9]			−4.0	0.5	V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 12 V, V− = −6.0 V to V+ = 6.0 V, V− = −3.0 V, $R_S = 2.0$ kΩ		200	μV/V	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$R_L = 100$ kΩ, $V_O = \pm 5.0$ V	2.5	6.0	V/mV	1	4
				2.0	7.0	V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 100$ kΩ	±5.0		V	1	4,5,6
			$R_L = 10$ kΩ	±3.5		V	1	4,5,6
$TR(t_r)$	Transient Response *(See Figure 1)*	Rise Time	C1 = 0.01 μF, R1 = 20 Ω, $R_L = 100$ kΩ, $V_I = 10$ mV, $C_L = 100$ pF, $A_V = 1.0$		120	ns	2	9
$TR(o_s)$		Overshoot			50	%	2	9
$TR(t_r)$	Transient Response *(See Figure 2)*	Rise Time	C3 = 50 pF, $R_L = 100$ kΩ, $V_I = 1.0$ mV, $A_V = 100$		30	ns	2	9
$TR(o_s)$		Overshoot			40	%	2	9

14

μA702QB (Cont.)
Electrical Characteristics V+ = +6.0 V, V− = −3.0 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		3.0	mV	1	1
				4.0	mV	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		15	μV/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		15	μV/°C	4	3
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		500	nA	1	1,2
				1500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		4.0	nA/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		13	nA/°C	4	3
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		2.3	μA	1	1
				7.5	μA	1	2,3
Z_I	Input Impedance[7]		22		kΩ	1	1
I_{CC2}	Supply Current	$V_O = 0$ V		3.3	mA	1	1,2
				3.9	mA	1	3
P_{c2}	Power Consumption[10]	$V_O = 0$ V		30	mW	1	1,2
				35	mW	1	3
CMR	Common Mode Rejection	$-1.5\ V \leqslant V_{CM} \leqslant 0.5$ V, $R_S = 2.0$ kΩ	80		dB	1	1
			70		dB	1	2,3
V_{IR}	Input Voltage Range[9]		−1.5	0.5	V	1	1,2,3
A_{VS}	Large Signal Voltage Gain	$R_L = 100$ kΩ, $V_O = \pm 2.5$ V	0.6	1.5	V/mV	1	4
			0.5	1.75	V/mV	1	5,6
V_{OP}	Output Voltage Swing	$R_L = 100$ kΩ	±2.5		V	1	4,5,6
		$R_L = 10$ kΩ	±1.5		V	1	4,5,6

Primary Burn-In Circuit



Equivalent Circuit
Refer to the Fairchild Linear Data Book Commercial Section

μA7092AQB

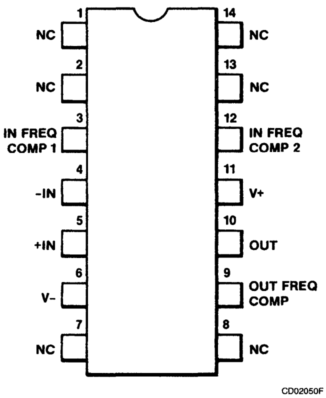
μA709AQB
High Performance Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

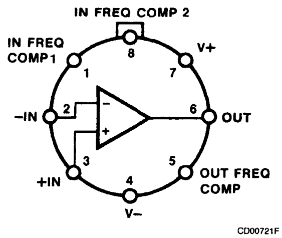
Description

The μA709AQB is a monolithic high gain operational amplifier constructed using the Fairchild Planar Epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in DC servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and non-linear transfer functions.[6]

Connection Diagram 14-Lead DIP (Top View)

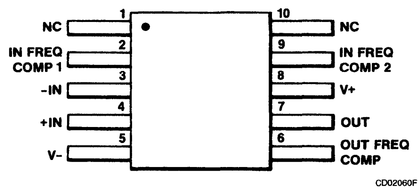


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA709ADMQB	CA	D-1 14-Lead DIP
μA709AHMQB	GC	A-1 8-Lead Can
μA709AFMQB	HA	F-4 10-Lead Flatpak

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±18 V
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Short Circuit Duration	5.0 s

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

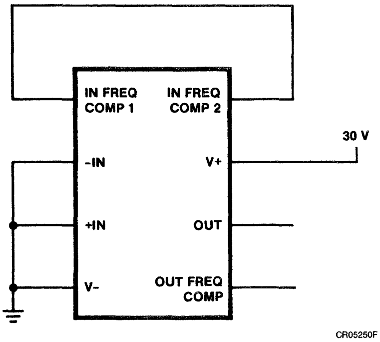
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C.
8. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak, and 120°C/W for the DIP.

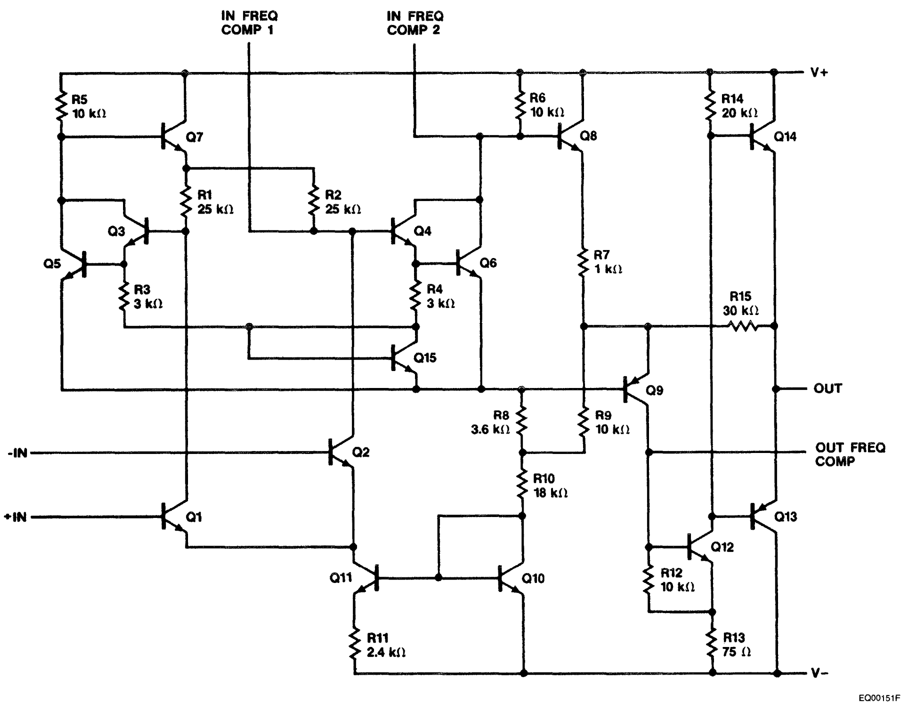
μA709AQB
Electrical Characteristics $\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$.

Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$50\ \Omega \leqslant R_S \leqslant 10\ k\Omega$, $V_{CM} = 0\ V$			2.0	mV	1	1
						3.0	mV	1	2,3
I_{IO}	Input Offset Current		$V_{CM} = 0\ V$			50	nA	1	1,2
						250	nA	1	3
I_{IB}	Input Bias Current		$V_{CC} = \pm 15\ V$, $V_{CM} = 0\ V$			148.5	nA	1	1
						447	nA	1	3
Z_I	Input Impedance[7]				350		kΩ	1	1
					85		kΩ	1	3
I_{CC}	Supply Current		$V_{CC} = \pm 15\ V$			3.6	mA	1	1
						3.0	mA	1	2
						4.5	mA	1	3
P_c	Power Consumption[8]		$V_{CC} = \pm 15\ V$			108	mW	1	1
CMR	Common Mode Rejection		$V_{CM} = \pm 8.0\ V$, $R_S = 10\ k\Omega$		80		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]		$V_{CC} = \pm 15\ V$		±8.0		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 18\ V$, $R_S = 10\ k\Omega$			100	μV/V	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$, $R_L = 2.0\ k\Omega$, $V_O = 10\ k\Omega$		25	70	V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$	$R_L = 10\ k\Omega$	±12		V	1	4,5,6
				$R_L = 2.0\ k\Omega$	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 15\ V$, $V_I = 20\ mV$, $R_L = 2.0\ k\Omega$, $C1 = 5.0\ nF$			1.5	μs	2	9
$TR(o_s)$		Overshoot	$V_{CC} = \pm 15\ V$, $R2 = 50\ \Omega$, $C_L = 100\ pF$, $R1 = 1.5\ k\Omega$, $C2 = 200\ pF$			30	%	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

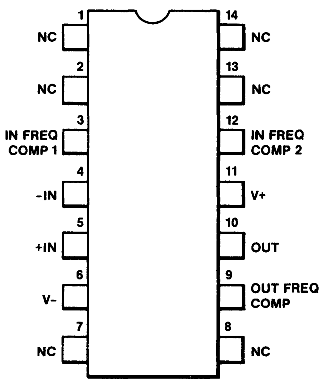
μA709QB High Performance Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

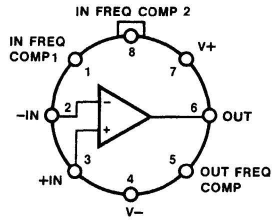
Description

The μA709QB is a monolithic high gain operational amplifier constructed using the Fairchild Planar Epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little performance degradation. The amplifier is intended for use in DC servo systems, high impedance analog computers, low level instrumentation applications and for the generation of special linear and non-linear transfer functions.[6]

Connection Diagram 14-Lead DIP (Top View)

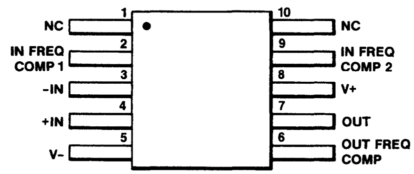


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA709DMQB	CA	D-1 14 Lead DIP
μA709HMQB	GC	A-1 8-Lead Can
μA709FMQB	HA	F-4 10-Lead Flatpak

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±18 V
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Short Circuit Duration	5.0 s

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

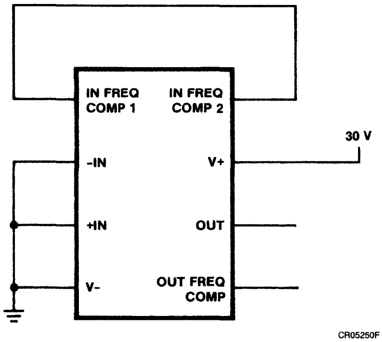
Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 2.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak, and 120°C/W for the DIP.

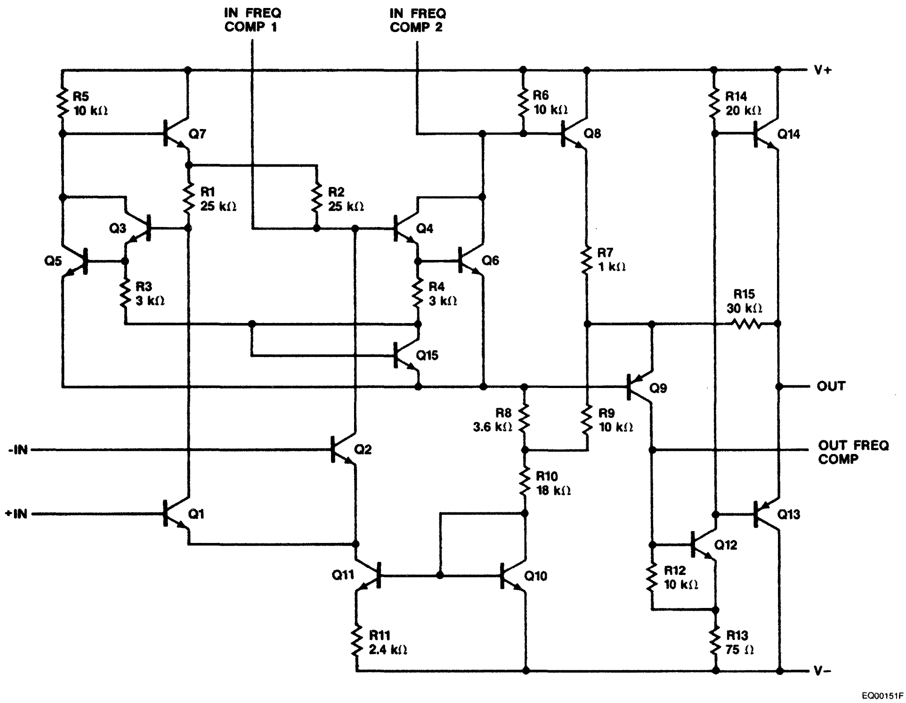
μA709QB
Electrical Characteristics $\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$

Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$50\ \Omega \leqslant R_S \leqslant 10\ k\Omega$, $V_{CM} = 0\ V$			5.0	mV	1	1
						6.0	mV	1	2,3
I_{IO}	Input Offset Current		$V_{CM} = 0\ V$			200	nA	1	1,2
						500	nA	1	3
I_{IB}	Input Bias Current		$V_{CC} = \pm 15\ V$, $V_{CM} = 0\ V$			340	nA	1	1
						950	nA	1	3
Z_I	Input Impedance[7]				150		kΩ	1	1
					40		kΩ	1	3
I_{CC}	Supply Current		$V_{CC} = \pm 15\ V$			5.5	mA	1	1
P_c	Power Consumption[8]		$V_{CC} = \pm 15\ V$			165	mW	1	1
CMR	Common Mode Rejection		$V_{CM} = \pm 8.0\ V$, $R_S = 10\ k\Omega$		70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]		$V_{CC} = \pm 15\ V$		±8.0		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 9.0\ V \leqslant V_{CC} \leqslant \pm 18\ V$, $R_S = 10\ k\Omega$			150	μV/V	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 15\ V$, $R_L = 2.0\ k\Omega$, $V_O = 10\ k\Omega$		25	70	V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 15\ V$	$R_L = 10\ k\Omega$	±12		V	1	4,5,6
				$R_L = 2.0\ k\Omega$	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 15\ V$, $V_I = 20\ mV$, $R_L = 2.0\ k\Omega$, $C1 = 5.0\ nF$			1.0	μs	2	9
$TR(o_s)$		Overshoot	$V_{CC} = \pm 15\ V$, $R_2 = 50\ \Omega$, $C_L = 100\ pF$, $R1 = 1.5\ k\Omega$, $C2 = 200\ pF$			30	%	2	9

Primary Burn-In Circuit



Equivalent Circuit



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MIL-STD-883

July 1986—Rev 1[5]

μA714QB Precision Operational Amplifier

Aerospace and Defense Data Sheet

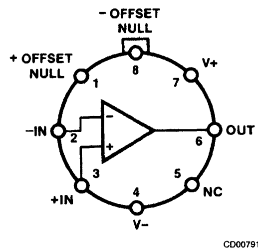
Linear Products

Description

The μA714QB is a monolithic instrumentation operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications.[6]

- **Low Offset Voltage**
- **Low Offset Voltage Drift**
- **Low Bias Current**
- **Low Input Noise Current**
- **High Open Loop Gain**
- **Low Input Offset Current**
- **High Common Mode Rejection**
- **Wide Power Supply Range**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA714HMQB	GC	A-1 8-Lead Can

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[11]	±22 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_{c1} is guaranteed by I_{CC1}; $P_{c1} = 30\ I_{CC1}$.
8. P_{c2} is guaranteed by I_{CC2}; $P_{c2} = 6\ I_{CC2}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.
11. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C

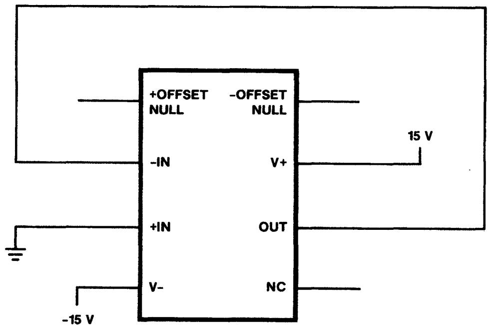
Group C and D Endpoints: Group A, Subgroup 1

μA714QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

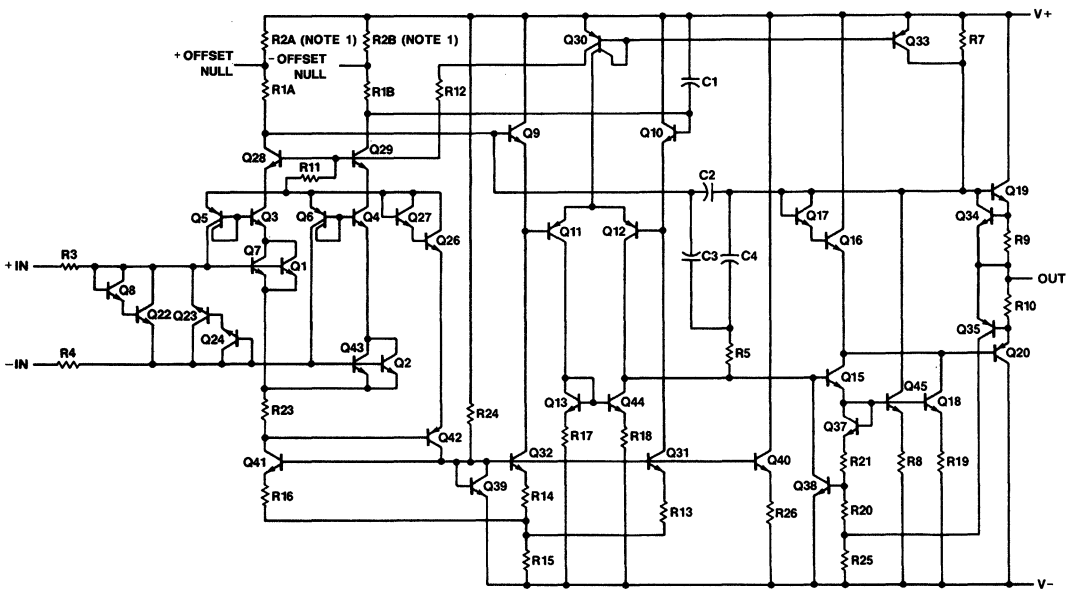
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		75	μV	1	1
				200	μV	1	2,3
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		2.8	nA	1	1
				5.6	nA	1	2,3
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		3.0	nA	1	1
				6.0	nA	1	2,3
I_{CC1}	Supply Current	$V_O = 0$ V		4.0	mA	1	1
I_{CC2}	Supply Current	$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		1.0	mA	1	1
P_{c1}	Power Consumption[7]	$V_O = 0$ V		120	mW	1	1
P_{c2}	Power Consumption[8]	$V_{CC} = \pm 3.0$ V, $V_O = 0$ V		6.0	mW	1	1
CMR	Common Mode Rejection	$V_{CM} = \pm 13$ V, $R_S = 50\ \Omega$	110		dB	1	1
			106		dB	1	2,3
V_{IR}	Input Voltage Range[9]		±13.0		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 3.0\ V \leqslant V_{CC} \leqslant \pm 18$ V, $R_S = 50\ \Omega$		10	μV/V	1	1
				20	μV/V	1	2,3
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	200		V/mV	1	4
			150		V/mV	1	5,6
		$V_{CC} = \pm 3.0$ V, $V_O = \pm 0.5$ V, $R_L = 500\ \Omega$	150		V/mV	1	4
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.5		V	1	4
		$R_L = 2.0$ kΩ	±12.0		V	1	4,5,6
		$R_L = 1.0$ kΩ	±10.5		V	1	4

14

Primary Burn-In Circuit



Equivalent Circuit



Note

1. R2A and R2B are electronically adjusted on a chip at the factory for minimum offset voltage.

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MIL-STD-883
July 1986—Rev 1[5]

μA715QB High Speed Operational Amplifier

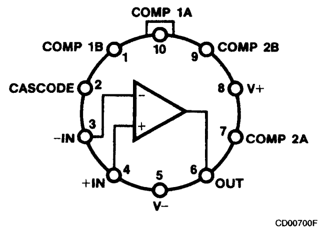
Aerospace and Defense Data Sheet
Linear Products

Description

The μA715QB is a high speed, high gain, monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715QB features fast settling time, high slew rate, low offsets and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715QB is ideally suited for use in A/D and D/A converters, active filters, deflection amplifiers, video amplifiers, phase-locked loops, multiplexed analog gates, precision comparators, sample-and-holds, and general feedback applications requiring DC wide bandwidth operation.[6]

- **High Slew Rate**
- **Fast Settling Time**
- **Wide Bandwidth**
- **Wide Operating Supply Range**
- **Wide Input Voltage Ranges**

Connection Diagram
10-Lead Can
(Top View)



Lead 5 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA715HMQB	IC	A-2 10-Lead Can

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can	350 mW
Supply Voltage	±18 V
Differential Input Voltage	±15 V
Input Voltage[10]	±15 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

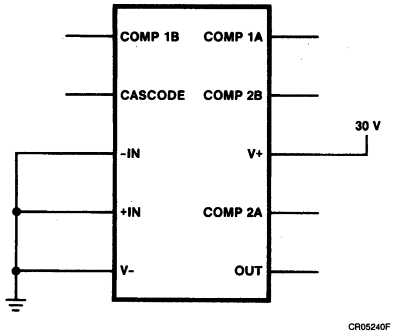
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W.
10. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

μA715QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

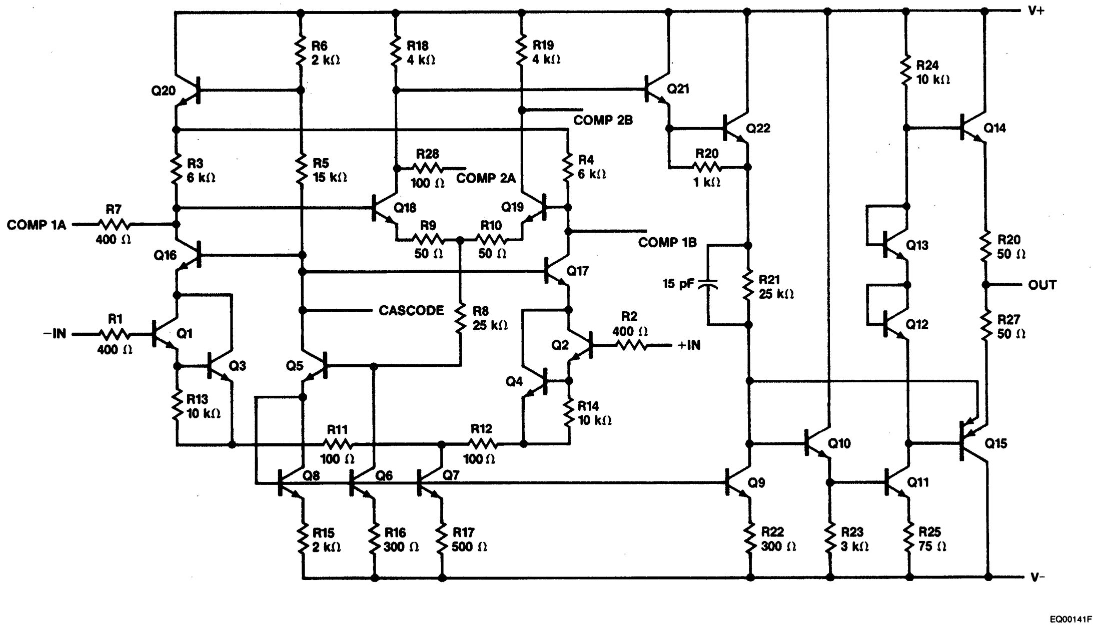
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
					7.5	mV	1	2,3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		250	nA	1	1,2
					800	nA	1	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		750	nA	1	1,2
					4.0	μA	1	3
I_{CC}	Supply Current				7.0	mA	1	1
P_c	Power Consumption[7]				210	mW	1	1
CMR	Common Mode Rejection		$V_{CM} = \pm 10$ V, $R_S = 10$ kΩ	74		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]			±10		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 7.0\ V \leqslant V_{CC} \leqslant \pm 18$ V, $R_S = 10$ kΩ		300	μV/V	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	15		V/mV	1	4
				10		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_I = 400$ mV, $A_V = 1.0$		60	ns	2	9
$TR(o_s)$		Overshoot			40	%	2	9
SR	Slew Rate		$A_V = 1.0$	15		V/μs	2	9

14

Primary Burn-In Circuit



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA725AQB Instrumentation Operational Amplifier

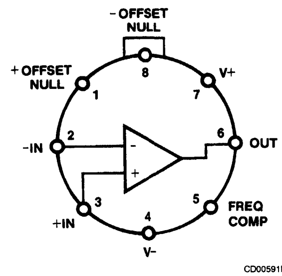
Aerospace and Defense Data Sheet
Linear Products

Description

The μA725AQB is a monolithic instrumentation operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725AQB is lead compatible with the popular μA741AQB operational amplifier.[6]

- **Low Input Noise Current**
- **High Open Loop Gain**
- **Low Input Offset Current**
- **Low Input Voltage Drift**
- **High Common Mode Rejection**
- **High Input Voltage Range**
- **Wide Power Supply Range**
- **Offset Null Capability**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA725AHMQB	GC	A-1 8-Lead Can

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[11]	±22 V
Voltage Between Offset Null and V+	±0.5 V
Short Circuit Duration[12]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

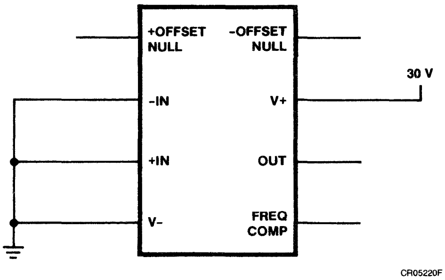
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_{c1} is guaranteed by I_{CC1}: $P_{c1} = 30\ I_{CC1}$.
8. P_{c2} is guaranteed by I_{CC2}: $P_{c2} = 6.0\ I_{CC2}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.
11. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA725AQB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

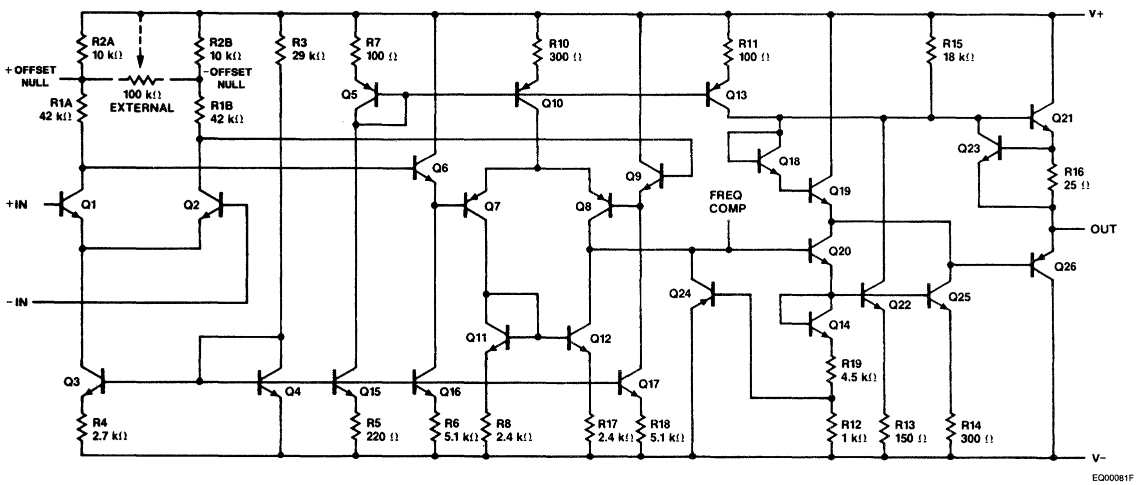
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage (Without External Trim)	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		0.5	mV	1	1
				0.75	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (Without External Trim)	$25°C \leq T_A \leq 125°C$		2.0	μV/°C	4	2
		$-55°C \leq T_A \leq +25°C$		5.0	μV/°C	4	3
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		5.0	nA	1	1
				4.0	nA	1	2
				18	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leq T_A \leq 125°C$		90	pA/°C	4	2
		$-55°C \leq T_A \leq +25°C$		90	pA/°C	4	3
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		75	nA	1	1
				70	nA	1	2
				180	nA	1	3
I_{CC1}	Supply Current			4.0	mA	1	1
I_{CC2}	Supply Current	$V_{CC} = \pm 3.0$ V		1.0	mA	1	1
P_{c1}	Power Consumption[7]			120	mW	1	1
P_{c2}	Power Consumption[8]	$V_{CC} = \pm 3.0$ V		6.0	mW	1	1
CMR	Common Mode Rejection	$V_{CM} = \pm 13.5$ V, $R_S = 50\ \Omega$	120		dB	1	1
			110		dB	1	2,3
V_{IR}	Input Voltage Range[9]		±13.5		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 5.0\ V \leq V_{CC} \leq \pm 22$ V, $R_S = 50\ \Omega$		5.0	μV/V	1	1
				8.0	μV/V	1	2,3
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	1000		V/mV	1	4,5
			500		V/mV	1	6
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12.5		V	1	4
		$R_L = 2.0$ kΩ	±10		V	1	5,6
N_O	Noise Voltage	f = 10 Hz		15	$nV/\sqrt{Hz}$	4	9
		100 Hz ≤ f ≤ 1.0 kHz		12	$nV/\sqrt{Hz}$	4	9
N_I	Noise Current	f = 10 Hz		1.2	$pA/\sqrt{Hz}$	4	9
		f = 100 Hz		0.6	$pA/\sqrt{Hz}$	4	9
		f = 1.0 kHz		0.25	$pA/\sqrt{Hz}$	4	9

14

Primary Burn-In Circuit



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA725QB Instrumentation Operational Amplifier

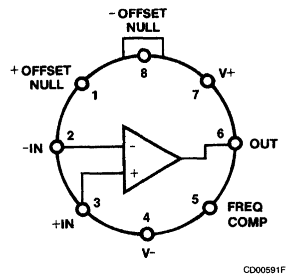
Aerospace and Defense Data Sheet
Linear Products

Description

The μA725QB is a monolithic instrumentation operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725QB is lead compatible with the popular μA741QB operational amplifier.[6]

- **Low Input Noise Current**
- **High Open Loop Gain**
- **Low Input Offset Current**
- **Low Input Voltage Drift**
- **High Common Mode Rejection**
- **High Input Voltage Range**
- **Wide Power Supply Range**
- **Offset Null Capability**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA725HMQB	QC	A-1 8-Lead Can

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can	330 mW
Supply Voltage	±22 V
Differential Input Voltage	±5.0 V
Input Voltage[10]	±22 V
Voltage Between Offset Null and V+	±0.5 V
Short Circuit Duration[11]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

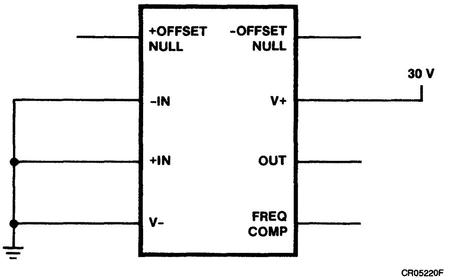
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.
10. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
11. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

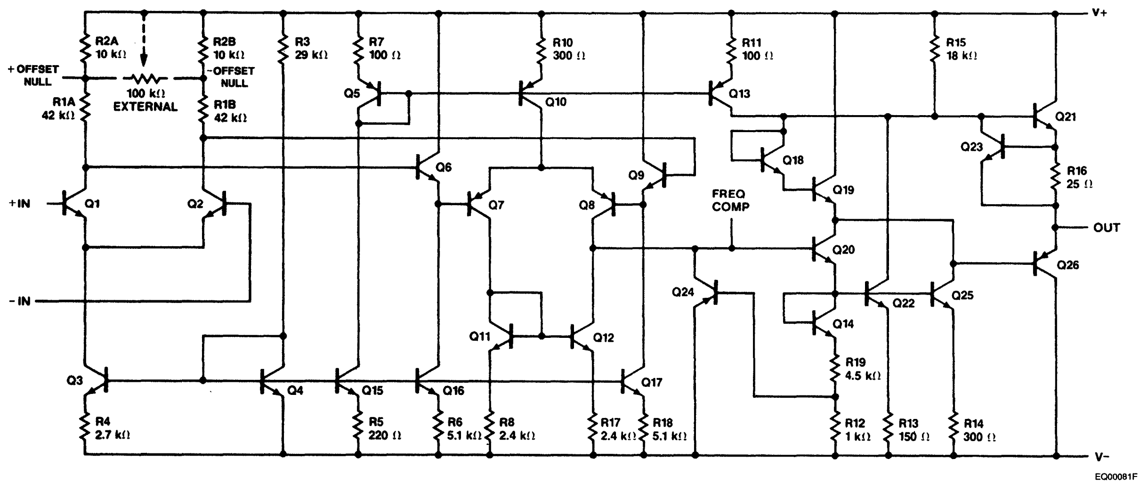
μA725QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage (Without External Trim)	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		1.0	mV	1	1
				1.5	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity (Without External Trim)	$25°C \leqslant T_A \leqslant 125°C$		5.0	μV/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		7.0	μV/°C	4	3
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		20	nA	1	1,2
				40	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		150	pA/°C	4	2
		$-55°C \leqslant T_A \leqslant +25°C$		150	pA/°C	4	3
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		100	nA	1	1,2
				200	nA	1	3
I_{CC}	Supply Current			4.0	mA	1	1
P_c	Power Consumption[7]			120	mW	1	1
CMR	Common Mode Rejection	$V_{CM} = \pm 13.5$ V, $R_S = 50\ \Omega$	110		dB	1	1
			100		dB	1	2,3
V_{IR}	Input Voltage Range[8]		±13.5		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 22$ V, $R_S = 50\ \Omega$		10	μV/V	1	1
				20	μV/V	1	2,3
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	1000		V/mV	1	4,5
			250		V/mV	1	6
V_{OP}	Output Voltage Swing	$R_L = 10$ kΩ	±12		V	1	4
		$R_L = 2.0$ kΩ	±10		V	1	4,5,6

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD
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MIL-STD-883
July 1986—Rev 2[5]

μA741AQB Operational Amplifier

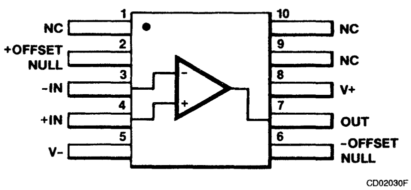
Aerospace and Defense Data Sheet
Linear Products

Description

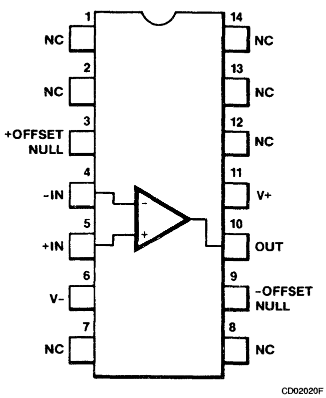
The μA741AQB is a high performance monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741AQB ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.[6]

- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

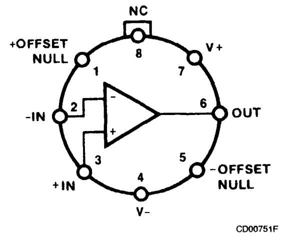
Connection Diagram 10-Lead Flatpak (Top View)



Connection Diagram 14-Lead DIP (Top View)

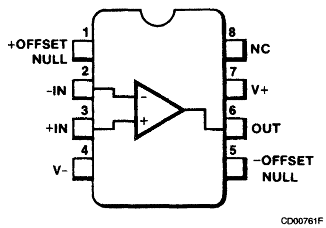


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 8-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA741ADMQB	CA	D-1 14-Lead DIP
μA741AHMQB	GC	A-1 8-Lead Can
μA741AFMQB	HA	F-4 10-Lead Flatpak
μA741ARMQB	PA	D-4 8-Lead DIP

JAN Product Available

10101	BCA	D-1 14-Lead DIP
10101	BCB	D-1 14-Lead DIP
10101	BGA	A-1 8-Lead Can
10101	BGC	A-1 8-Lead Can
10101	BHA	F-4 10-Lead Flatpak
10101	BHB	F-4 10-Lead Flatpak
10101	BPA	D-4 8-Lead DIP
10101	BPB	D-4 8-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[12]	±20 V
Short Circuit Duration[13]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C and 19 mV at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 40\ I_{CC}$.
9. V_{IR} is guaranteed by the CMR test.
10. BW is guaranteed by t_r: $BW = 0.35/t_r$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA741AQB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V			3.0	mV	1	1
						4.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$			15	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$			15	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		$V_{CC} = \pm 20$ V		5.0		mV	1	1,2,3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V			30	nA	1	1
						70	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$			0.5	nA/°C	4	2
			$-55°C \leq T_A \leq +25°C$			0.5	nA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V			80	nA	1	1
						210	nA	1	2,3
Z_I	Input Impedance[7]				1.0		MΩ	1	1
					0.5		MΩ	1	2
I_{CC}	Supply Current		$V_{CC} = \pm 20$ V			3.750	mA	1	1
						3.375	mA	1	2
						4.125	mA	1	3
P_c	Power Consumption[8]		$V_{CC} = \pm 20$ V			150	mW	1	1
						135	mW	1	2
						165	mW	1	3
CMR	Common Mode Rejection		$V_{CC} = \pm 20$ V, $V_{CM} = \pm 15$ V, $R_S = 50\ \Omega$		80		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]		$V_{CC} = \pm 20$ V		±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 10 V, V− = −20 V to V+ = 20 V, V− = −10 V, $R_S = 50\ \Omega$			50	μV/V	1	1
						100	μV/V	1	2,3
I_{OS}	Output Short Circuit Current					60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_{CC} = \pm 20$ V, $V_O = \pm 15$ V, $R_L = 2.0$ kΩ		50		V/mV	1	4
					32		V/mV	1	5,6
			$V_{CC} = \pm 5.0$ V, $V_O = \pm 2.0$ V, $R_L = 2.0$ kΩ		10		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		$V_{CC} = \pm 20$ V	$R_L = 10$ kΩ	±16		V	1	4,5,6
				$R_L = 2.0$ kΩ	±15		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$			800	ns	3	9, 10, 11
$TR(o_s)$		Overshoot				25	%	3	9, 10, 11
BW	Bandwidth[10]				0.437		MHz	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$		0.3		V/μs	3	9, 10, 11
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz			15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz			40	μV_{pk}	4	9

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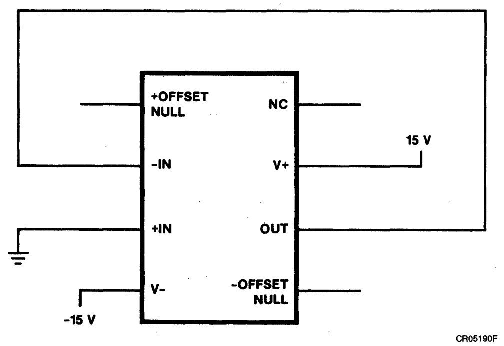
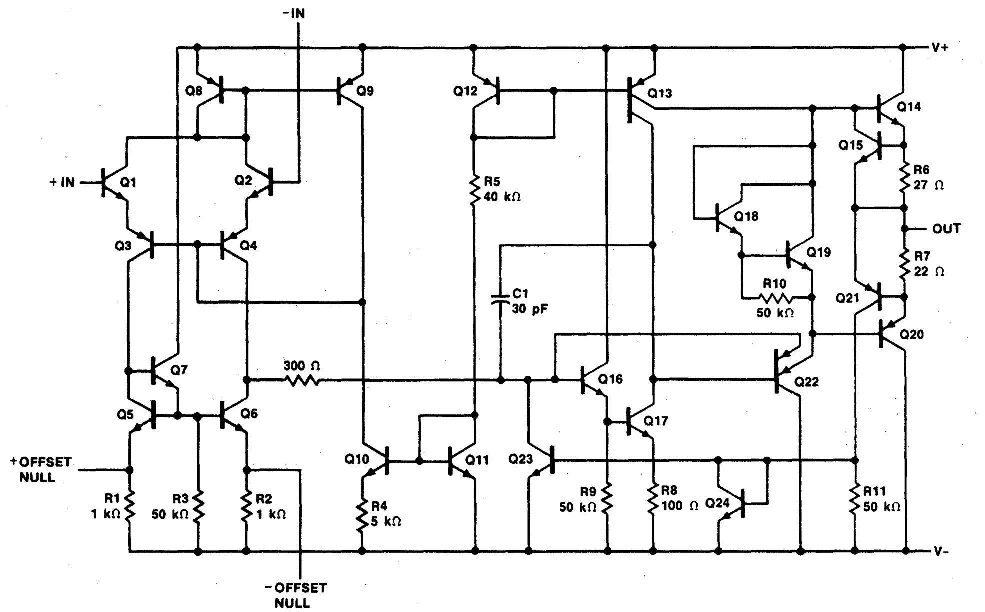
Primary Burn-In Circuit
(38510/10101 may be used by FSC as an alternate)



Equivalent Circuit



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μA741QB
Operational Amplifier

MIL-STD-883
July 1986—Rev 2[5]

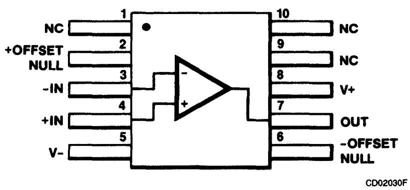
Aerospace and Defense Data Sheet
Linear Products

Description

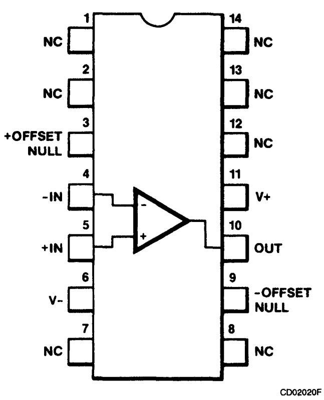
The μA741QB is a high performance monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of latch-up tendencies make the μA741QB ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.[6]

- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

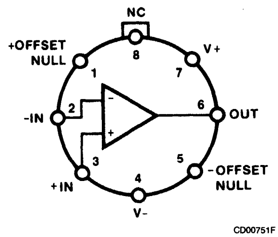
Connection Diagram
10-Lead Flatpak
(Top View)



Connection Diagram
14-Lead DIP
(Top View)

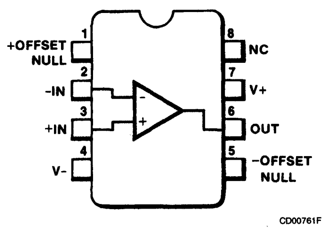


Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA741DMQB	CA	D-1 14-Lead DIP
μA741HMQB	GC	A-1 8-Lead Can
μA741FMQB	HA	F-4 10-Lead Flatpak
μA741RMQB	PA	D-4 8-Lead DIP

JAN Product Available

10101	BCA	D-1 14-Lead DIP
10101	BCB	D-1 14-Lead DIP
10101	BGA	A-1 8-Lead Can
10101	BGC	A-1 8-Lead Can
10101	BHA	F-4 10-Lead Flatpak
10101	BHB	F-4 10-Lead Flatpak
10101	BPA	D-4 8-Lead DIP
10101	BPB	D-4 8-Lead DIP

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[11]	
Can and Flatpak	330 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[12]	±20 V
Short Circuit Duration[13]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

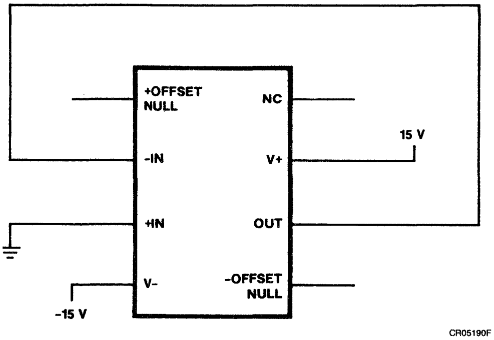
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C and 19 mW at −55°C.
8. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$
9. V_{IR} is guaranteed by the CMR test.
10. BW is guaranteed by t_r: $BW = 0.35/t_r$.
11. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
12. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
13. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA741QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

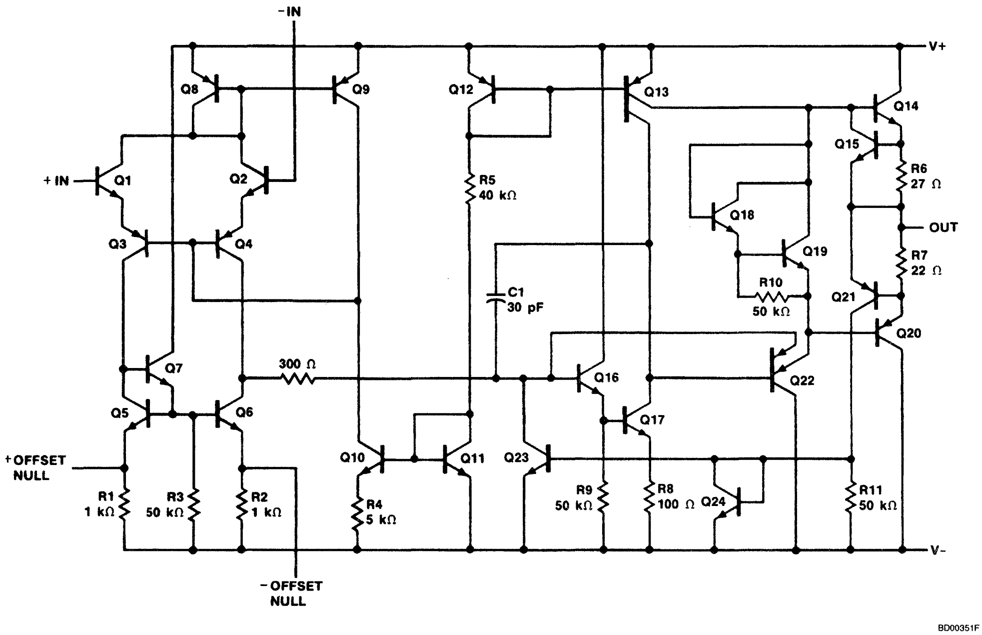
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgr
V_{IO}	Input Offset Voltage		$50\ \Omega \leq R_S \leq 10\ k\Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		15	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		15	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		$V_{CC} = \pm 20$ V	5.0		mV	1	1,2,3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		200	nA	1	1,2
					500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		1.0	nA/°C	4	2
			$-55°C \leq T_A \leq +25°C$		1.0	nA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		340	nA	1	1
					500	nA	1	2
					1500	nA	1	3
Z_I	Input Impedance[7]			0.3		MΩ	1	1
				0.2		MΩ	1	2
I_{CC}	Supply Current				2.8	mA	1	1
					2.5	mA	1	2
					3.3	mA	1	3
P_c	Power Consumption[8]				85	mW	1	1
					75	mW	1	2
					100	mW	1	3
CMR	Common Mode Rejection		$V_{CM} = \pm 12$ V, $R_S = 50\ \Omega$	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]			±12		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 5.0\ V \leq V_{CC} \leq \pm 22$ V, $R_S = 50\ \Omega$		150	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0\ k\Omega$	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10\ k\Omega$	±12		V	1	4,5,6
			$R_L = 2.0\ k\Omega$	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0\ k\Omega$, $C_L = 100$ pF, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[10]			0.437		MHz	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0\ k\Omega$, $A_V = 1.0$	0.3		V/μs	3	9, 10, 11
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		40	μV_{pk}	4	9

14

Primary Burn-In Circuit
(38510/10101 may be used by FSC as an alternate)



Equivalent Circuit



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MIL-STD-883
July 1986—Rev 2[5]

μA747AQB Dual Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

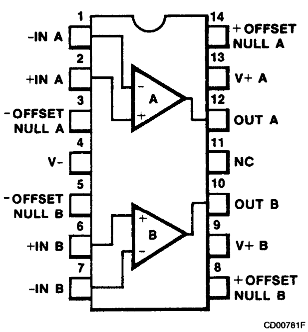
Description

The μA747AQB is a pair of high performance monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA747AQB ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.

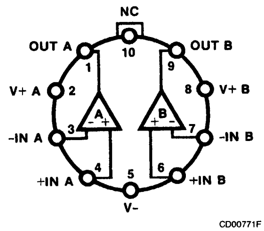
The μA747AQB is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications.[6]

- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

Connection Diagram 14-Lead DIP (Top View)

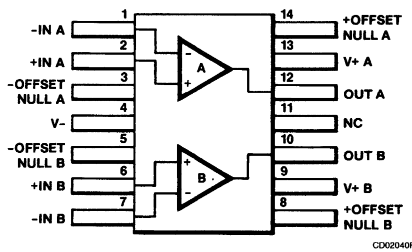


Connection Diagram 10-Lead Can (Top View)



Lead 5 connected to case.

Connection Diagram 14-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA747AFMQB	AA	F-1 14-Lead Flatpak
μA747ADMQB	CA	D-1 14-Lead DIP
μA747AHMQB	IC	A-2 10-Lead Can

JAN Product Available

10102	BAA	F-1 14-Lead Flatpak
10102	BAB	F-1 14-Lead Flatpak
10102	BCA	D-1 14-Lead DIP
10102	BCB	D-1 14-Lead DIP
10102	BIA	A-2 10-Lead Can
10102	BIC	A-2 10-Lead Can

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[12]	
Can and Flatpak	350 mW
DIP	400 mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[13]	±20 V
Short Circuit Duration[14]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at -55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Not available on μA747AHMQB.
8. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at -55°C.
9. P_c is guaranteed by I_{CC}: $P_c = 40\ I_{CC}$.
10. V_{IR} is guaranteed the CMR test.
11. BW is guaranteed by t_r: $BW = 0.35/t_r$.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Can and Flatpak and 120°C/W for the DIP.
13. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
14. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA747AQB
Electrical Characteristics ±5.0 V ≤ V_{CC} ≤ ±20 V, unless otherwise specified.

Symbol	Characteristic		Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		R_S = 50 kΩ, V_{CM} = 0 V			3.0	mV	1	1
						4.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			15	μV/°C	4	2
			−55°C ≤ T_A ≤ +25°C			15	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range[7]		V_{CC} = ±20 V		5.0		mV	1	1,2,3
I_{IO}	Input Offset Current		V_{CM} = 0 V			30	nA	1	1
						70	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		25°C ≤ T_A ≤ 125°C			0.2	nA/°C	4	2
			−55°C ≤ T_A ≤ +25°C			0.5	nA/°C	4	3
I_{IB}	Input Bias Current		V_{CM} = 0 V			80	nA	1	1
						210	nA	1	2,3
Z_I	Input Impedance[8]		V_{CC} = ±20 V		1.0		MΩ	1	1
					0.5		MΩ	1	2
I_{CC}	Supply Current (Total)		V_{CC} = ±20 V			7.50	mA	1	1
						6.75	mA	1	2
						8.25	mA	1	3
P_c	Power Consumption (Total)[9]		V_{CC} = ±20 V			300	mW	1	1
						270	mW	1	2
						330	mW	1	3
CMR	Common Mode Rejection		V_{CC} = ±20 V, V_{CM} = ±15 V, R_S = 50 Ω		80		dB	1	1,2,3
V_{IR}	Input Voltage Range[10]				±15		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 10 V, V− = −20 V to V+ = 20 V, V− = −10 V, R_S = 50 Ω			50	μV/V	1	1
						100	μV/V	1	2,3
I_{OS}	Output Short Circuit Current					60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		V_{CC} = ±20 V, V_O = ±15 V, R_L = 2.0 kΩ		50		V/mV	1	4
					32		V/mV	1	5,6
			V_{CC} = ±5 V, V_O = ±2 V, R_L = 2.0 kΩ		10		V/mV	1	4,5,6
V_{OP}	Output Voltage Swing		V_{CC} = ±20 V	R_L = 10 kΩ	±16		V	1	4,5,6
				R_L = 2.0 kΩ	±15		V	1	4,5,6
TR(t_r)	Transient Response	Rise Time	V_{CC} = ±20 V, V_I = 50 mV, R_L = 2.0 kΩ, C_L = 100 pF, A_V = 1.0			800	ns	3	9, 10, 11
TR(o_s)		Overshoot				25	%	3	9, 10, 11
BW	Bandwidth[11]				0.437		MHz	3	9, 10, 11

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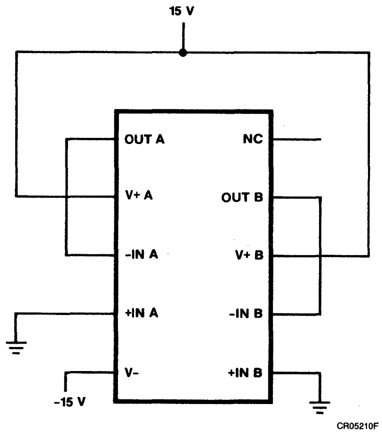
μA747AQB (Cont.)

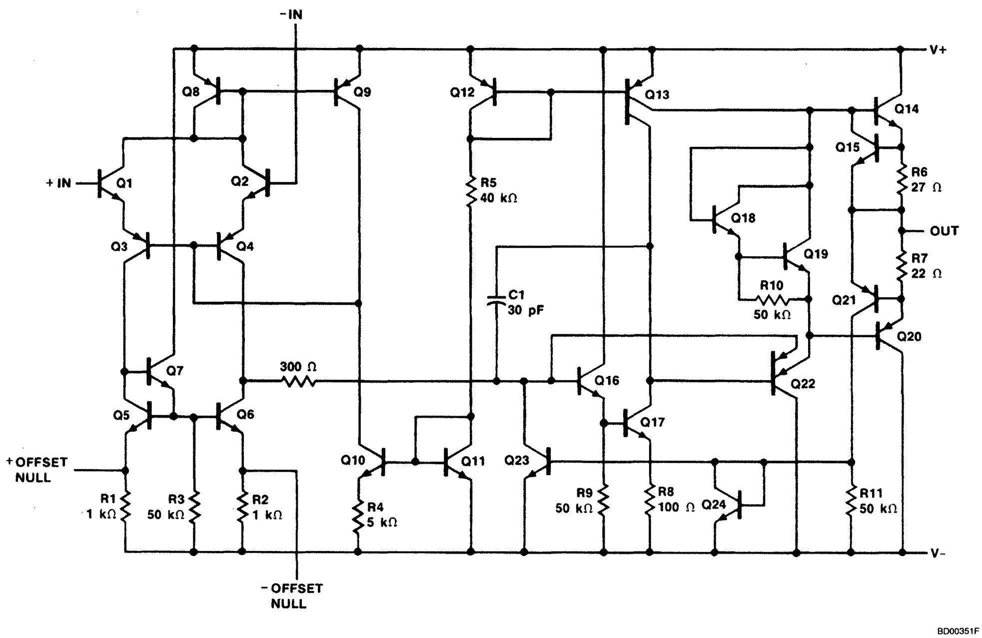
Electrical Characteristics ±5.0 V ≤ V_{CC} ≤ ±20 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
SR	Slew Rate	V_{CC} = ±20 V, R_L = 2.0 kΩ, A_V = 1.0	0.3		V/μs	3	9, 10, 11
CS	Channel Separation	V_{CC} = ±20 V	100		dB	1	9, 10, 11
N_I (BB)	Noise Broadband	V_{CC} = ±20 V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn	V_{CC} = ±20 V, BW = 5.0 kHz		40	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/10102 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA747QB Dual Operational Amplifier

Aerospace and Defense Data Sheet
Linear Products

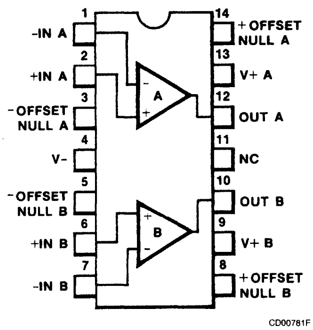
Description

The μA747QB is a pair of high performance monolithic operational amplifiers constructed using the Fairchild Planar Epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of latch-up make the μA747QB ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.

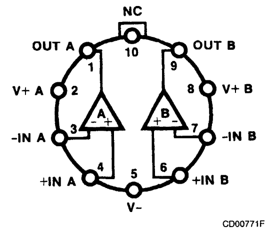
The μA747QB is short circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications.[6]

- **No Frequency Compensation Required**
- **Short Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common Mode And Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

Connection Diagram 14-Lead DIP (Top View)

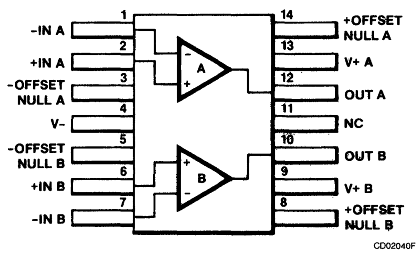


Connection Diagram 10-Lead Can Package (Top View)



Lead 5 connected to case.

Connection Diagram 14-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA747FMQB	AA	F-1 14-Lead Flatpak
μA747DMQB	CA	D-1 14-Lead DIP
μA747HMQB	IC	A-2 10-Lead Can

JAN Product Available

10102	BAA	F-1 14-Lead Flatpak
10102	BAB	F-1 14-Lead Flatpak
10102	BCA	D-1 14-Lead DIP
10102	BCB	D-1 14-Lead DIP
10102	BIA	A-2 10-Lead Can
10102	BIC	A-2 10-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[12]	
Can and Flatpak	350 mW
DIP	400mW
Supply Voltage	±22 V
Differential Input Voltage	±30 V
Input Voltage[13]	±20 V
Short Circuit Duration[14]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Not available on μA747HMQB.
8. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at −55°C.
9. P_c is guaranteed by I_{CC}: $P_c = 30\ I_{CC}$.
10. V_{IR} is guaranteed by the CMR test.
11. BW is guaranteed by t_r: $BW = 0.35/t_r$.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Can and Flatpak and 120°C/W for the DIP.
13. For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
14. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

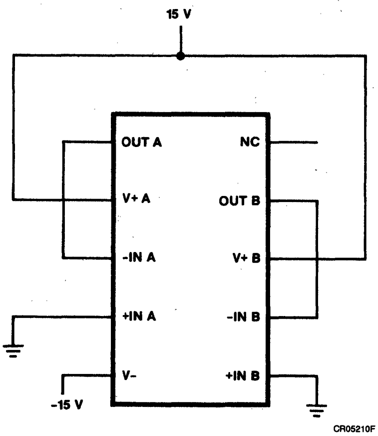
μA747QB

Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

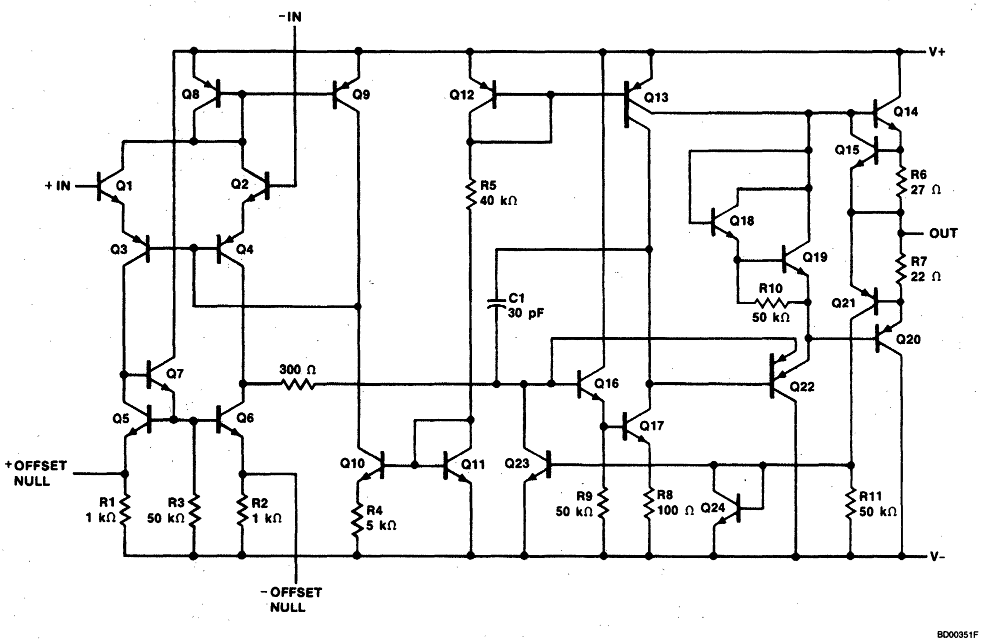
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 10$ kΩ, $V_{CM} = 0$ V		5.0	mV	1	1
					6.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		25°C ≤ T_A ≤ 125°C		15	μV/°C	4	2
			−55°C ≤ T_A ≤ +25°C		15	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range[7]			5.0		mV	4	1,2,3
I_{IO}	Input Offset Current		$V_{CM} = 0$ V		200	nA	1	1,2
					500	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity		25°C ≤ T_A ≤ 125°C		1.0	nA/°C	4	2
			−55°C ≤ T_A ≤ +25°C		1.0	nA/°C	4	3
I_{IB}	Input Bias Current		$V_{CM} = 0$ V		340	nA	1	1
					500	nA	1	2
					1500	nA	1	3
Z_I	Input Impedance[8]			0.3		MΩ	1	1
				0.2		MΩ	1	2
I_{CC}	Supply Current (Total)				5.6	mA	1	1
					5.0	mA	1	2
					6.6	mA	1	3
P_c	Power Consumption (Total)[9]				170	mW	1	1
					150	mW	1	2
					200	mW	1	3
CMR	Common Mode Rejection		$V_{CM} = \pm 12$ V, $R_S = 50$ Ω	70		dB	1	1,2,3
V_{IR}	Input Voltage Range[10]			±12		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		V+ = 10 V, V− = −20 V to V+ = 20 V, V− = −10 V, $R_S = 50$ Ω		150	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				60	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
			$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_{CC} = \pm 20$ V, $V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		800	ns	3	9, 10, 11
$TR(o_s)$		Overshoot			25	%	3	9, 10, 11
BW	Bandwidth[11]			0.437		MHz	3	9, 10, 11
SR	Slew Rate		$V_{CC} = \pm 20$ V, $R_L = 2.0$ kΩ, $A_V = 1.0$	0.3		V/μs	3	9, 10, 11
CS	Channel Separation		$V_{CC} = \pm 20$ V	80		dB	1	9
N_I (BB)	Noise Broadband		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		$V_{CC} = \pm 20$ V, BW = 5.0 kHz		40	μV_{pk}	4	9

14

Primary Burn-In Circuit
(38510/10102 may be used by FSC as an alternate)



Equivalent Circuit (1/2 of circuit)



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MIL-STD-883
July 1986—Rev 1[5]

μA759QB Power Operational Amplifier

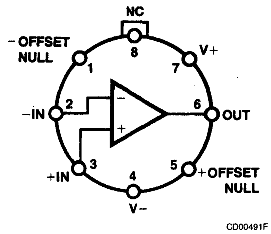
Aerospace and Defense Data Sheet
Linear Products

Description

The μA759QB is a high performance monolithic operational amplifier constructed using the Fairchild Planar Epitaxial process. The amplifier provides high output current and features small signal characteristics better than the μA741QB. The amplifier is designed to operate from a single or dual power supply and the input common mode range includes the negative supply. The high gain and high output power provide superior performance whenever an operational amplifier is needed. The μA759QB employs internal current-limiting, thermal shutdown and safe-area compensation making it essentially indestructible. It is intended for a wide range of applications including voltage regulators, audio amplifiers, servo amplifiers, and power drivers.[6]

- **High Output Current**
- **Internal Short Circuit Current-Limiting**
- **Internal Thermal Overload Protection**
- **Internal Output Transistors Safe-Area Protection**
- **Input Common Mode Voltage Range Includes Ground Or Negative Supply**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA759HMQB	GB	A-1 8-Lead Can

14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
Supply Voltage	±18 V
Differential Input Voltage	±15 V
Input Voltage[11]	(V− − 0.3 V) to V+

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C

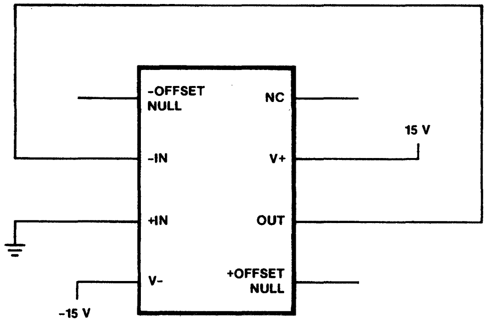
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Z_I is guaranteed by I_{IB}: $Z_I = 4.0\ V_T/I_{IB}$, $V_T = 26$ mV at 25°C, 34 mV at 125°C, and 19 mV at −55°C.
8. V_{IR} is guaranteed by the CMR test.
9. $V_O = \pm 12$ V is guaranteed by worse case $V_O = \pm 5$ V.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.
11. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

μA759QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

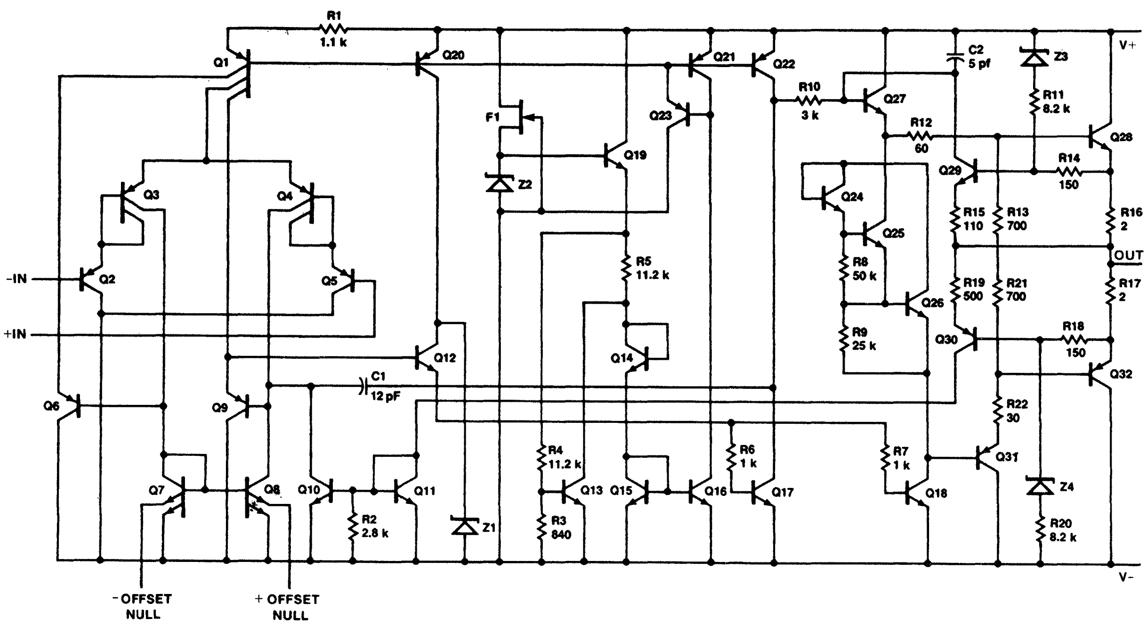
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		3.0	mV	1	1
				4.5	mV	1	2,3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		6.0		mV	1	1
I_{IO}	Input Offset Current	$V_{CM} = 0$ V		30	nA	1	1
				60	nA	1	2,3
I_{IB}	Input Bias Current	$V_{CM} = 0$ V		150	nA	1	1
				300	nA	1	2,3
Z_I	Input Impedance[7]		0.25		MΩ	1	1
I_{CC}	Supply Current			18	mA	1	1
CMR	Common Mode Rejection	$-15\ V \leqslant V_{CM} \leqslant 13$ V, $R_S = 10$ kΩ	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]		−15	13	V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 18$ V, $R_S = 10$ kΩ		100	μV/V	1	1,2,3
I_{pk}	Peak Output Current[9]	$5.0\ V \leqslant V_O \leqslant 12$ V, $-12\ V \leqslant V_O \leqslant -5.0$ V	±325		mA	1	1
A_{VS}	Large Signal Voltage Gain	$R_L = 50\ \Omega$, $V_O = \pm 10$ V	50		V/mV	1	4
			25		V/mV	1	5,6
V_{OP}	Output Voltage Swing	$R_L = 50\ \Omega$	±10		V	1	4,5,6

Primary Burn-In Circuit



CR05200F

Equivalent Circuit



EQ00021F

FAIRCHILD
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μA771BQB Operational Amplifier

MIL-STD-883
July 1986—Rev 1[5]

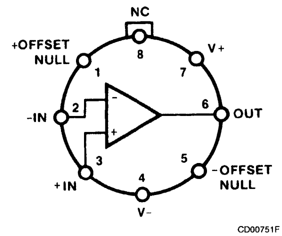
Aerospace and Defense Data Sheet
Linear Products

Description

This monolithic JFET input operational amplifier incorporates well matched ion-implanted JFETs on the same chip with standard bipolar transistors. The key feature of this op amp is low input bias currents in the sub nanoamp range plus high slew rate and wide bandwidth.[6]

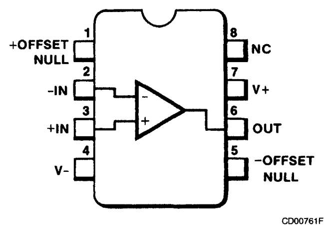
- **Low Input Bias Current**
- **Low Input Offset Current**
- **High Slew Rate**
- **Wide Bandwidth**

Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 8-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA771BHMQB	GC	A-1 8-Lead Can
μA771BRMQB	PA	D-4 8-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
DIP	400 mW
Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage[11]	±16 V
Short Circuit Duration[12]	Indefinite

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

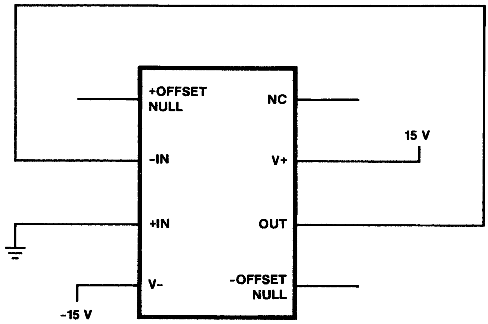
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal dissipation, P_D. $T_J = T_A + \theta jA\ P_D$ where θjA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
8. V_{IR} is guaranteed by the CMR test.
9. V_{OP} is guaranteed by the A_{VS} test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and 120°C/W for the DIP.
11. For negative supply voltages less than −16 V, the negative input voltage is equal to the negative supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

μA771BQB

Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specifies.

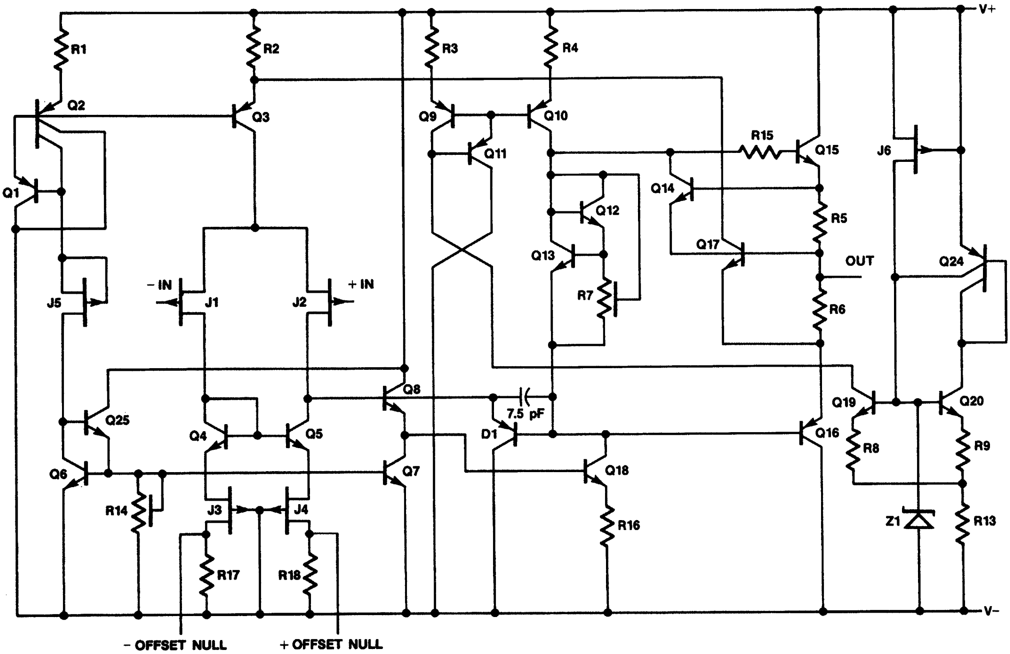
Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
					8.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		30	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		30	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		$V_{CM} = 0$ V	8.0		mV	4	1,2,3
I_{IO}	Input Offset Current[7]		$V_{CM} = 0$ V		50	pA	1	1
					20	nA	1	2,3
I_{IB}	Input Bias Current[7]		$V_{CM} = 0$ V		100	pA	1	1
					50	nA	1	2,3
I_{CC}	Supply Current				2.8	mA	1	1
					3.4	mA	1	2,3
CMR	Common Mode Rejection		$V_{CM} = \pm 11$ V, $R_S = 50$ kΩ	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]			±11		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 10\ V \leq V_{CC} \leq \pm 18$ V, $R_S = 50$ kΩ		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				80	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
	Output Voltage Swing[9]		$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		200	ns	4	9,10,11
$TR(o_s)$		Overshoot			40	%	4	9,10,11
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$	7.0		V/μs	4	9,10,11
t_S	Settling Time		$A_V = 1.0$		1500	ns	4	9
N_I (BB)	Noise Broadband		BW = 10 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		BW = 10 kHz		80	μV_{pk}	4	9

Primary Burn-In Circuit
(38510/11904 may be used by FSC as an alternate)



CR05190F

Equivalent Circuit



EQ00051F

FAIRCHILD

A Schlumberger Company

μA772BQB Operational Amplifier

MIL-STD-883
July 1986—Rev 1[5]

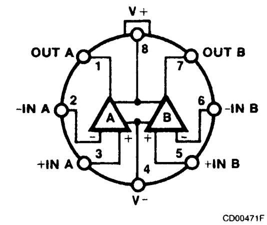
Aerospace and Defense Data Sheet
Linear Products

Description

This monolithic JFET input operational amplifier incorporates well matched ion-implanted JFETS on the same chip with standard bipolar transistors. The key feature of this op amp is low input bias currents in the sub nanoamp range plus high slew rate and wide bandwidth.[6]

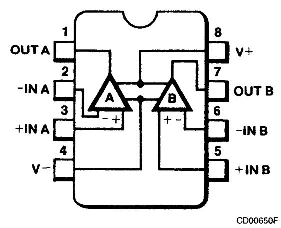
- **Low Input Bias Current**
- **Low Input Offset Current**
- **High Slew Rate**
- **Wide Bandwidth**

Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 8-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA772BHMQB	GC	A-1 8-Lead Can
μA772BRMQB	PA	D-4 8-Lead DIP

JAN Product Available

11905	BPB	D-4 8-Lead DIP

14

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
DIP	400 mW
Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage[11]	±16 V
Short Circuit Duration[12]	Indefinite

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal dissipation, P_D. $T_J = T_A + \theta jA\ P_D$ where θjA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
8. V_{IR} is guaranteed by the CMR test.
9. V_{OP} is guaranteed by the A_{VS} test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and 120°C/W for the DIP.
11. For negative supply voltages less than −16 V, the negative input voltage is equal to the negative supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

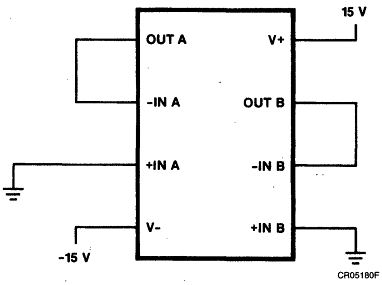
μA772BQB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
					8.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leq T_A \leq 125°C$		30	μV/°C	4	2
			$-55°C \leq T_A \leq +25°C$		30	μV/°C	4	3
I_{IO}	Input Offset Current[7]		$V_{CM} = 0$ V		50	pA	1	1
					20	nA	1	2,3
I_{IB}	Input Bias Current[7]		$V_{CM} = 0$ V		100	pA	1	1
					50	nA	1	2,3
I_{CC}	Supply Current (Total)				5.6	mA	1	1
					6.8	mA	1	2,3
CMR	Common Mode Rejection		$V_{CM} = \pm 11$ V, $R_S = 50$ kΩ	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]			±11		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 10\ V \leq V_{CC} \leq \pm 18$ V, $R_S = 50$ kΩ		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				80	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
	Output Voltage Swing[9]		$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_I = 50$ mV, $R_L = 2.0$ kΩ $C_L = 100$ pF, $A_V = 1.0$		200	ns	4	9,10,11
$TR(o_s)$		Overshoot			40	%	4	9,10,11
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$	7.0		V/μs	4	9,10,11
t_S	Settling Time		$A_V = 1.0$		1500	ns	4	9
N_I (BB)	Noise Broadband		BW = 10 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		BW = 10 kHz		80	μV_{pk}	4	9
CS	Channel Separation			80		dB	1	9

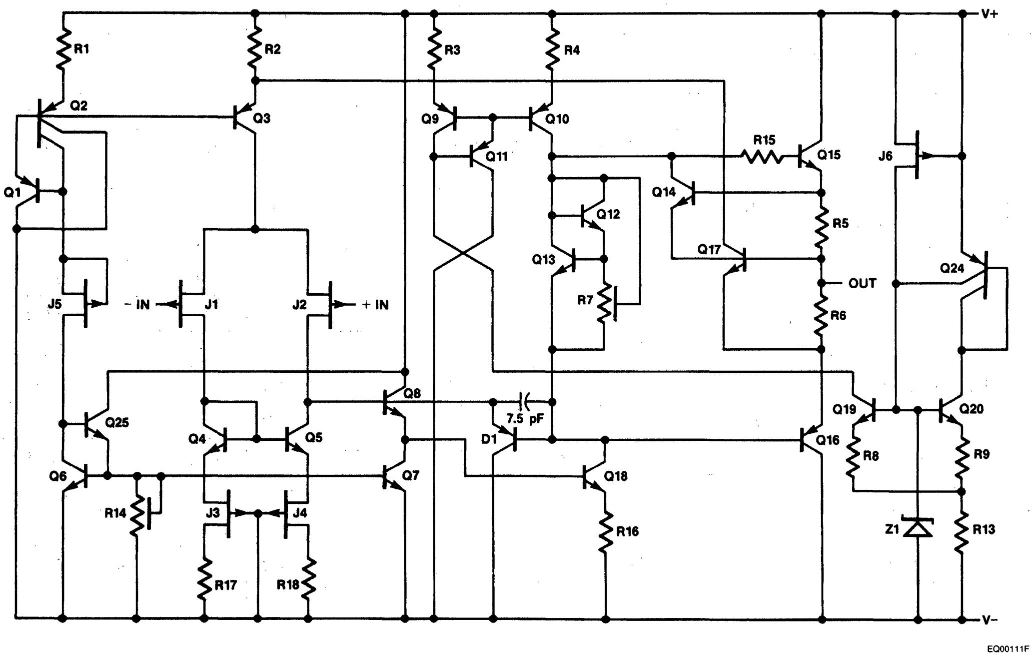
14

Primary Burn-In Circuit

(38510/11905 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD
A Schlumberger Company

μA774BQB Operational Amplifier

MIL-STD-883
July 1986—Rev 1[5]

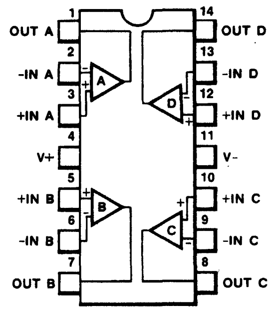
Aerospace and Defense Data Sheet
Linear Products

Description

This monolithic JFET input operational amplifier incorporates well matched ion-implanted JFETS on the same chip with standard bipolar transistors. The key feature of this op amp is low input bias currents in the sub nanoamp range plus high slew rate and wide bandwidth.[6]

- **Low Input Bias Current**
- **Low Input Offset Current**
- **High Slew Rate**
- **Wide Bandwidth**

Connection Diagram 14-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA774BDMQB	PA	D-1 14-Lead DIP

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
DIP	400 mW
Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage[11]	±16 V
Short Circuit Duration[12]	Indefinite

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal dissipation, P_D. $T_J = T_A + \theta jA\ P_D$ where θjA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
8. V_{IR} is guaranteed by the CMR test.
9. V_{OP} is guaranteed by the A_{VS} test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
11. For negative supply voltages less than −16 V, the negative input voltage is equal to the negative supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

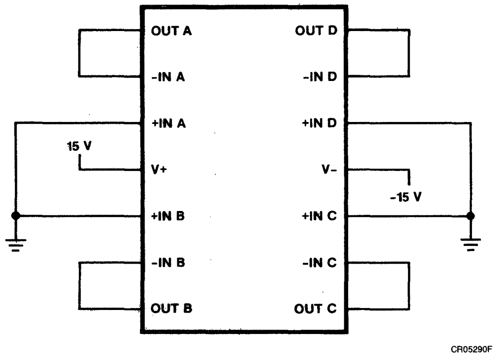
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

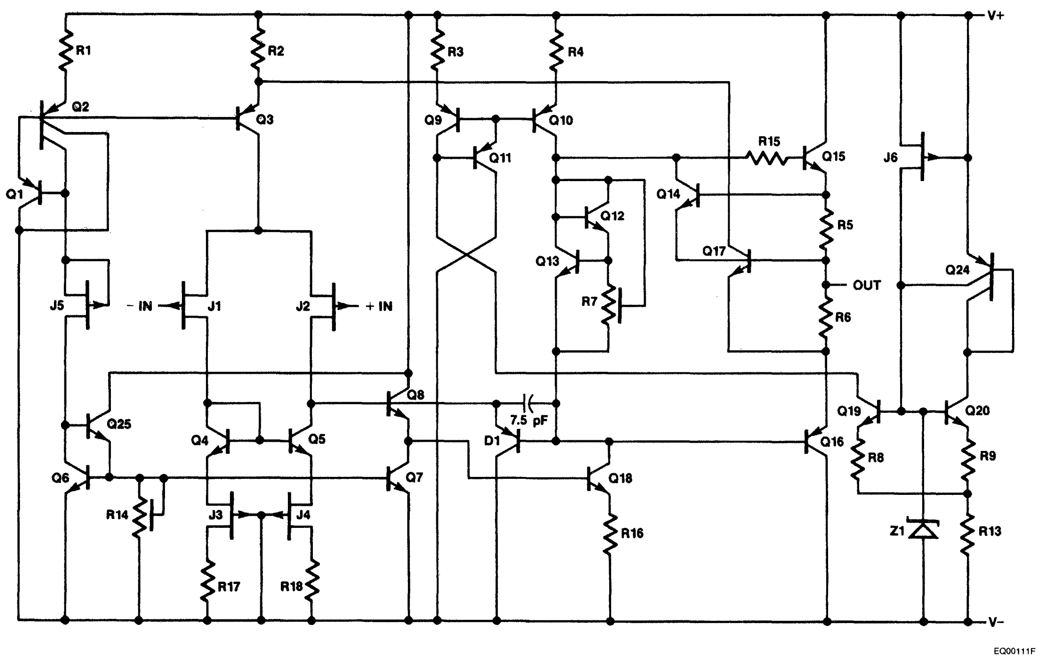
μA774BQB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage		$R_S = 50\ \Omega$, $V_{CM} = 0$ V		5.0	mV	1	1
					8.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity		$25°C \leqslant T_A \leqslant 125°C$		30	μV/°C	4	2
			$-55°C \leqslant T_A \leqslant +25°C$		30	μV/°C	4	3
I_{IO}	Input Offset Current[7]		$V_{CM} = 0$ V		50	pA	1	1
					20	nA	1	2,3
I_{IB}	Input Bias Current[7]		$V_{CM} = 0$ V		100	pA	1	1
					50	nA	1	2,3
I_{CC}	Supply Current (Total)				11.2	mA	1	1
					13.6	mA	1	2,3
CMR	Common Mode Rejection		$V_{CM} = \pm 11$ V, $R_S = 50$ kΩ	80		dB	1	1,2,3
V_{IR}	Input Voltage Range[8]			±11		V	1	1,2,3
PSRR	Power Supply Rejection Ratio		$\pm 10\ V \leqslant V_{CC} \leqslant \pm 18$ V, $R_S = 50\ \Omega$		100	μV/V	1	1,2,3
I_{OS}	Output Short Circuit Current				80	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain		$V_O = \pm 10$ V, $R_L = 2.0$ kΩ	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing		$R_L = 10$ kΩ	±12		V	1	4,5,6
	Output Voltage Swing[9]		$R_L = 2.0$ kΩ	±10		V	1	4,5,6
$TR(t_r)$	Transient Response	Rise Time	$V_I = 50$ mV, $R_L = 2.0$ kΩ, $C_L = 100$ pF, $A_V = 1.0$		200	ns	4	9,10,11
$TR(o_s)$		Overshoot			40	%	4	9,10,11
SR	Slew Rate		$R_L = 2.0$ kΩ, $A_V = 1.0$	7.0		V/μs	4	9,10,11
t_S	Settling Time		$A_V = 1.0$		1500	ns	4	9
N_I (BB)	Noise Broadband		BW = 10 kHz		15	μV_{rms}	4	9
N_I (PC)	Noise Popcorn		BW = 10 kHz		80	μV_{pk}	4	9
CS	Channel Separation			80		dB	1	9

Primary Burn-In Circuit
(38510/11906 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of Circuit)



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA776QB
Multi-Purpose Programmable Operational Amplifier

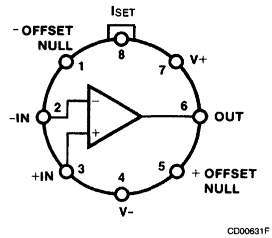
Aerospace and Defense Data Sheet
Linear Products

Description

The μA776QB Programmable Operational Amplifier is constructed using the Fairchild Planar Epitaxial process. High input impedance, low supply currents, and low input noise (over a wide range of operating supply voltages) coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption, analog applications. Input noise voltage, noise current, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nanowatt power consumption or for characteristics similar to the μA741QB. Internal frequency compensation, absence of latch-up, high slew rate, and short circuit current protection assure ease of use in long time integrators, active filters, and sample-and-hold circuits.[6]

- **Micropower Consumption**
- **± 1.2 V to ± 18 V Operation**
- **No Frequency Compensation Required**
- **Low Input Bias Currents**
- **Wide Programming Range**
- **High Slew Rate**
- **Low Noise**
- **Short Circuit Protection**
- **Offset Null Capability**
- **No Latch-Up**

Connection Diagram
8-Lead Can
(Top View)



Lead 4 connected to case.

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA776HMQB	GB	A-1 8-Lead Can

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
Can	330 mW
Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage[11]	±15 V
Short Circuit Duration[12]	Indefinite
Voltage Between Offset Null and V−	±0.5 V
I_{SET} (Max Current at I_{SET})	500 μA
V_{SET} (Max Voltage to GND at I_{SET})	$(V+ - 2\ V) \leq V_{SET} \leq V+$

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_{c1} is guaranteed by I_{CC1}: $P_{c1} = 30\ I_{CC1}$.
8. P_{c2} is guaranteed by I_{CC2}: $P_{c2} = 6\ I_{CC2}$.
9. V_{IR} is guaranteed by the CMR test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W.
11. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
12. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature for $I_{SET} \leq 30$ μA.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

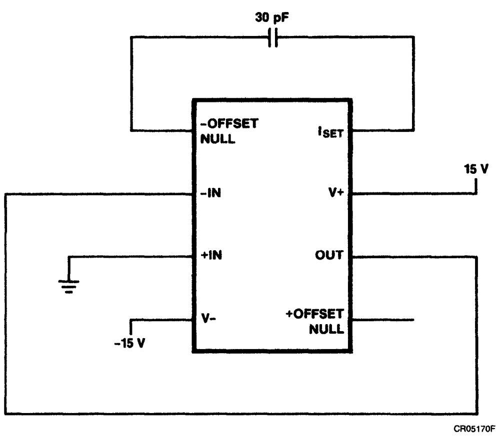
μA776QB
Electrical Characteristics $\pm 3.0\ V \leq V_{CC} \leq \pm 15\ V$, $1.5\ \mu A \leq I_{SET} \leq 15\ \mu A$, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $V_{CM} = 0\ V$			5.0	mV	1	1
					6.0	mV	1	2,3
I_{IO}	Input Offset Current	$V_{CM} = 0\ V$	$I_{SET} = 1.5\ \mu A$		3.0	nA	1	1
					5.0	nA	1	2
					10	nA	1	3
			$I_{SET} = 15\ \mu A$		15	nA	1	1,2
					40	nA	1	3
I_{IB}	Input Bias Current	$V_{CM} = 0\ V$	$I_{SET} = 1.5\ \mu A$		7.5	nA	1	1,2
					20	nA	1	3
			$I_{SET} = 15\ \mu A$		50	nA	1	1,2
					120	nA	1	3
I_{CC1}	Supply Current	$V_{CC} = \pm 15\ V$	$I_{SET} = 1.5\ \mu A$		25	μA	1	1
					30	μA	1	2,3
			$I_{SET} = 15\ \mu A$		180	μA	1	1
					200	μA	1	2,3
I_{CC2}	Supply Current	$V_{CC} = \pm 3.0\ V$	$I_{SET} = 1.5\ \mu A$		20	μA	1	1
					25	μA	1	2,3
			$I_{SET} = 15\ \mu A$		160	μA	1	1
					180	μA	1	2,3
P_{c1}	Power Consumption[7]	$V_{CC} = \pm 15\ V$	$I_{SET} = 1.5\ \mu A$		0.75	mW	1	1
					0.9	mW	1	2,3
			$I_{SET} = 15\ \mu A$		5.4	mW	1	1
					6.0	mW	1	2,3
P_{c2}	Power Consumption[8]	$V_{CC} = \pm 3.0\ V$	$I_{SET} = 1.5\ \mu A$		120	μW	1	1
					150	μW	1	2,3
			$I_{SET} = 15\ \mu A$		960	μW	1	1
					1080	μW	1	2,3
CMR	Common Mode Rejection	$V_{CC} = \pm 15\ V$, $V_{CM} = \pm 10\ V$, $R_S = 50\ \Omega$		70		dB	1	1,2,3
		$V_{CC} = \pm 3.0\ V$, $V_{CM} = \pm 1.0\ V$, $R_S = 50\ \Omega$		70		dB	1	1,2,3
V_{IR}	Input Voltage Range[9]	$V_{CC} = \pm 15\ V$		±10		V	1	1,2,3
		$V_{CC} = \pm 3.0\ V$		±1.0		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	$\pm 3.0\ V \leq V_{CC} \leq \pm 18\ V$, $R_S = 50\ \Omega$			150	μV/V	1	1,2,3

μA776QB (Cont.)
Electrical Characteristics $\pm 3.0\ V \leqslant V_{CC} \leqslant \pm 15\ V$, $1.5\ \mu A \leqslant I_{SET} \leqslant 15\ \mu A$, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
A_{VS}	Large Signal Voltage Gain	$V_{CC} = \pm 15\ V$, $V_O = \pm 10\ V$	$I_{SET} = 1.5\ \mu A$, $R_L = 75\ k\Omega$	200		V/mV	1	4
				100		V/mV	1	5,6
			$I_{SET} = 15\ \mu A$, $R_L = 75\ k\Omega$	100		V/mV	1	4
				75		V/mV	1	5,6
		$V_{CC} = \pm 3.0\ V$, $V_O = \pm 1.0\ V$	$I_{SET} = 1.5 \mu A$, $R_L = 75\ k\Omega$	50		V/mV	1	4
				25		V/mV	1	5,6
			$I_{SET} = 15\ \mu A$, $R_L = 5.0\ k\Omega$	50		V/mV	1	4
				25		V/mV	1	5,6
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 15\ V$, $R_L = 75\ k\Omega$		± 12		V	1	4
				± 10		V	1	5,6
		$V_{CC} = \pm 3.0\ V$	$I_{SET} = 1.5\ \mu A$, $R_L = 75\ k\Omega$	± 2.0		V	1	4,5,6
			$I_{SET} = 15\ \mu A$, $R_L = 5.0\ k\Omega$	± 1.9		V	1	4,5,6

Primary Burn-In Circuit



Equivalent Circuit

Refer to the Fairchild Linear Data Book Commercial Section

FAIRCHILD

A Schlumberger Company

μA111QB Voltage Comparator

MIL-STD-883
July 1986—Rev 2[5]

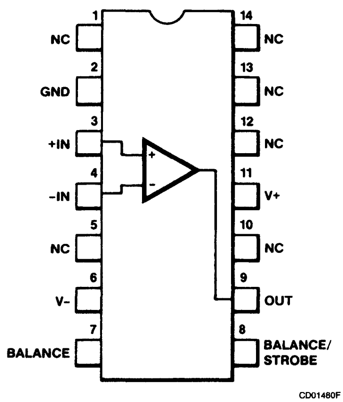
Aerospace and Defense Data Sheet
Linear Products

Description

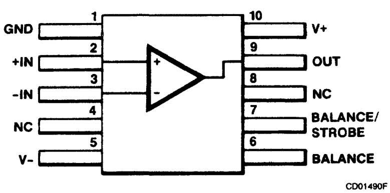
The μA111QB is a monolithic, low input current voltage comparator, constructed using the Fairchild Planar Epitaxial process. The μA111QB operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA111QB is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.[6]

- **Low Input Bias Current**
- **Low Input Offset Current**
- **Wide Differential Input Voltage**
- **Power Supply Voltage, Single 5 V To ±15 V**
- **Offset Voltage Null Capability**
- **Strobe Capability**

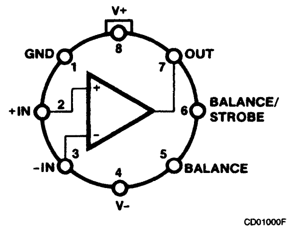
Connection Diagram 14-Lead DIP (Top View)



Connection Diagram 10-Lead Flatpak (Top View)

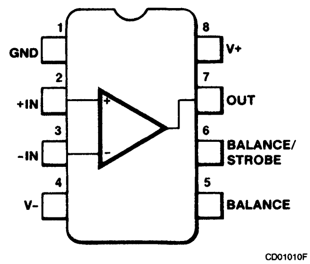


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 8-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA111DMQB	CA	D-1 (14-Lead DIP)
μA111HMQB	GC	A-1 (8-Lead Can)
μA111FMQB	HA	F-4 (10-Lead Flatpak)
μA111RMQB	PA	D-4 (8-Lead DIP)

JAN Product Available

10304	BCA	D-1 (14-Lead DIP)
10304	BCB	D-1 (14-Lead DIP)
10304	BGA	A-1 (8-Lead Can)
10304	BGC	A-1 (8-Lead Can)
10304	BHA	F-4 (10-Lead Flatpak)
10304	BHB	F-4 (10-Lead Flatpak)
10304	BPA	D-4 (8-Lead DIP)
10304	BPB	D-4 (8-Lead DIP)

Absolute Maximum Ratings

Storage Temperature Range	-65°C to 175°C
Operating Temperature Range	-55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can and Flatpak	330 mW
DIP	400 mW
Total Supply Voltage	36 V
Negative Supply Voltage	−30 V
Output to Negative Supply Voltage	50 V
Differential Input Voltage	±30 V
Input Voltage[10]	±15 V
Sink Current	50 mA
Strobe Current	10 mA
Short Circuit Duration	10 s

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. The limit is the maximum value required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effect of voltage gain and input impedance.
8. Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to V+.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.
10. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less negative.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at -55°C

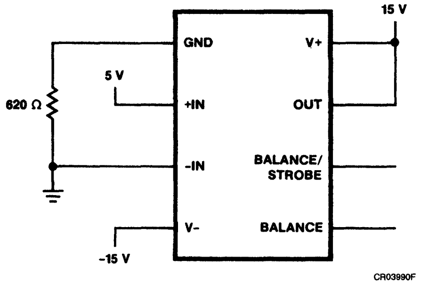
Group C and D Endpoints: Group A, Subgroup 1

μA111QB

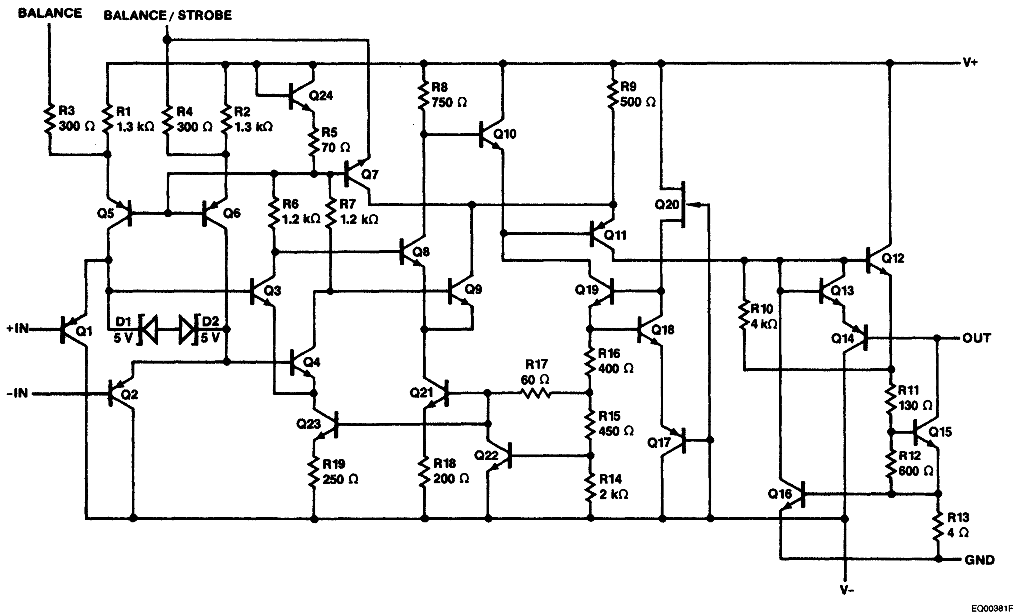
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage[7]	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 15$ V, $50\ \Omega \leqslant R_S \leqslant 50\ k\Omega$, $V_{CM} = 0$ V		3.0	mV	1	1
				4.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		25	μV/°C	4	2
		$-55°C \leqslant T_A \leqslant 25°C$		25	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		5.0		mV	1	1
$V_{IO\ (R)}$	Raised Input Offset Voltage[8]	$R_S = 50\ \Omega$, $-14.5\ V \leqslant V_{CM} \leqslant 13$ V, $V_{BAL} = V_{BAL}/STB = V+$		3.0	mV	1	1
				4.5	mV	1	2,3
I_{IO}	Input Offset Current[7]	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 15$ V, $V_{CM} = 0$ V		10	nA	1	1
				20	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	$25°C \leqslant T_A \leqslant 125°C$		100	PA/°C	4	2
		$-55°C \leqslant T_A \leqslant 25°C$		200	PA/°C	4	3
$I_{IO\ (R)}$	Raised Input Offset Current[8]	$R_S = 100\ k\Omega$, $V_{CM} = 0$ V, $V_{BAL} = V_{BAL}/STB = V+$		25	nA	4	1,2
				50	nA	4	3
I_{IB}	Input Bias Current	$\pm 5.0\ V \leqslant V_{CC} \leqslant \pm 15$ V, $V_{CM} = 0$ V		100	nA	1	1
				150	nA	1	2,3
I+	Positive Supply Current	V_O = Open, $V_I- = 10$ mV		6.0	mA	1	1,2
				7.0	mA	1	3
I−	Negative Supply Current	V_O = Open, $V_I- = 10$ mV	−5.0		mA	1	1,2
			−6.0		mA	1	3
V_{OL1}	Saturation Voltage 1	$V+ = 4.5$ V, $V- = 0$ V, $V_I- = 6.0$ mV, $I_{OL} = 8.0$ mA		0.4	V	1	1,2,3
V_{OL2}	Saturation Voltage 2	$V_I- = 50$ mV, $I_{OL} = 50$ mA		1.5	V	1	1,2,3
I_{CEX}	Output Leakage Current	$V_I+ = 5.0$ mV, $V_O = 35$ V		10	nA	1	1
				0.5	μA	1	2,3
I_{I1}	Input Leakage Current 1	$V_{CC} = \pm 18$ V, $V_I- = 29$ V	0	500	nA	1	1,2,3
I_{I2}	Input Leakage Current 2	$V_{CC} = \pm 18$ V, $V_I+ = 29$ V	0	500	nA	1	1,2,3
V_O	Collector Output Voltage	$R_S = 50\ \Omega$, $I_{ST} = -3.0$ mA	14		V	1	1,2,3
CMR	Common Mode Rejection	$R_S = 50\ \Omega$, $-14.5\ V \leqslant V_{CM} \leqslant 13$ V	80		dB	1	1,2,3
I_{OS}	Output Short Circuit Current	10 ms max test duration	0	200	mA	1	1
				150	mA	1	2
				250	mA	1	3
A_{VE}	Large Signal Voltage Gain (Emitter Follower Output)	$R_L = 600\ \Omega$		10	V/mV	1	4
				8.0	V/mV	1	5,6
t_{PLH}	Propagation Delay to High Level	$V_{OD} = 5.0$ mV, $C_L = 50$ pF, $V_I = 100$ mV	0	300	ns	4	9, 11
			0	600	ns	4	10
t_{PHL}	Propagation Delay to Low Level		0	300	ns	4	9, 11
			0	500	ns	4	10

Primary Burn-In Circuit
(38510/10304 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

μA139QB Quad Comparator

MIL-STD-883
July 1986—Rev 2[5]

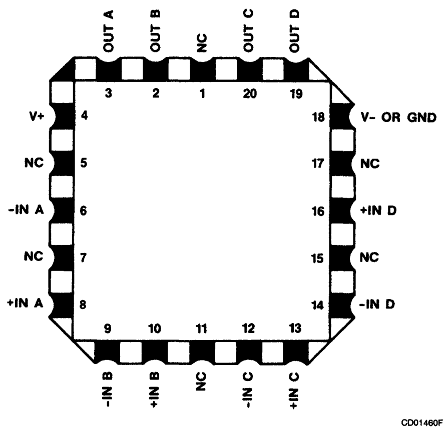
Aerospace and Defense Data Sheet
Linear Products

Description

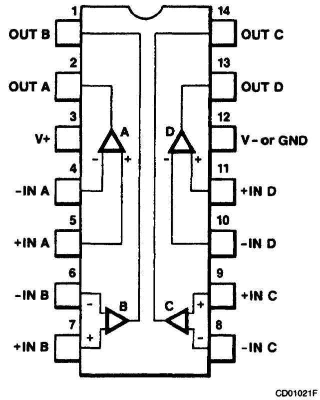
The μA139QB consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stages allow the input common mode voltage to include ground.[6]

- **Single Supply Operation**
- **Dual Supply Operation**
- **Allow Comparison Of Voltages Near Ground Potential**
- **Low Current Drain**
- **Compatible With All Forms Of Logic**
- **Low Input Bias Current**
- **Low Input Offset Current**
- **Low Offset Voltage**

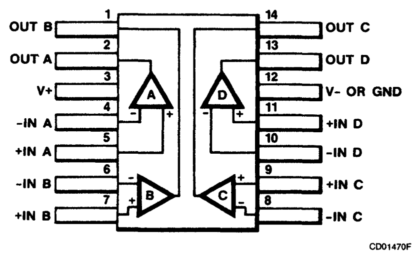
Connection Diagram 20-Terminal CCP (Top View)



Connection Diagram 14-Lead DIP (Top View)



Connection Diagram 14-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA139FMQB	AA	F-1 (14-Lead Flatpak)
μA139DMQB	CA	D-1 (14-Lead DIP)
μA139LMQB	2C	C-2 (20-Terminal CCP)

JAN Product Available

11201	BCA	D-1 (14-Lead DIP)
11201	BCB	D-1 (14-Lead DIP)

15

Absolute Maximum Ratings

Storage Temperature Range	-65°C to 175°C
Operating Temperature Range	-55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
Flatpak	350 mW
DIP and CCP	400 mW
Supply Voltage	±18 V or 36 V
Differential Input Voltage[9]	36 V
Input Voltage[10]	-0.3 V to 36 V
Input Current	10 mA
Short Circuit Duration[11]	Indefinite

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IR} is guaranteed by the V_{IO} test.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Flatpak and 120°C/W for the DIP and CCP.
9. The differential input voltage shall not exceed the supply voltage.
10. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage. The input common mode voltage or either signal input voltage should not be allowed to go negative more than 0.3 V.
11. Short circuit may be to ground or negative supply. Rating applies to 125°C case temperature or 75°C ambient temperature. Short circuit from output to V+ can cause extensive heating and eventual destruction. No more than one amplifier should be shorted at the same time as the maximum junction temperature will be exceeded.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at -55°C

Group C and D Endpoints: Group A, Subgroup 1

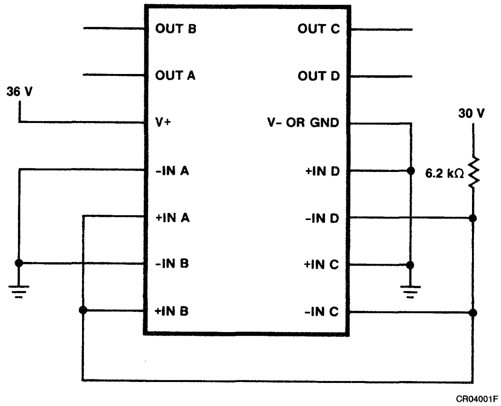
μA139QB

Electrical Characteristics V+ = 5 V, V− = 0 V, unless otherwise specified.

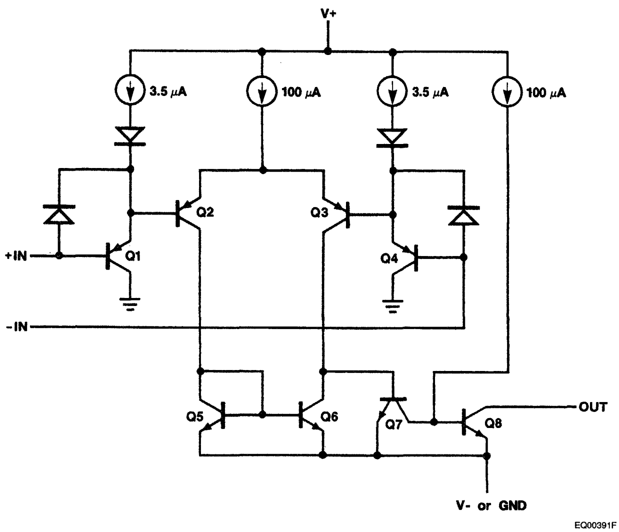
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	5.0 V ≤ V+ ≤ 36 V, V_O = 1.4 V; 0 V ≤ V_{CM} ≤ (V+) − 1.5 V		5.0	mV	1	1
		0 V ≤ V_{CM} ≤ (V+) − 2.0 V		9.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	25°C ≤ T_A ≤ 125°C		25	μV/°C	4	2
		−55°C ≤ T_A ≤ 25°C		25	μV/°C	4	3
I_{IO}	Input Offset Current	V_{CM} = 0 V		25	nA	1	1
				100	nA	1	2,3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	25°C ≤ T_A ≤ 125°C		300	pA/°C	4	2
		−55°C ≤ T_A ≤ 25°C		400	pA/°C	4	3
I_{IB}	Input Bias Current	V_{CM} = 0 V	−100		nA	1	1
			−300		nA	1	2,3
I_{CC}	Supply Current (Total)	V_{CC} = 5.0 V		2.0	mA	1	1,2
				3.0	mA	1	3
		V_{CC} = 30 V		3.0	mA	1	1,2
				4.0	mA	1	3
CMR	Common Mode Rejection	V+ = 30 V, R_S = 50 Ω, V_{CM} = 28 V	76		dB	4	1,2,3
V_{IR}	Input Voltage Range	5.0 V ≤ V+ ≤ 36 V, V_O = 1.4 V	0	V+ −1.5	V	7	1
			0	V+ −2	V	7	2,3
I_{CEX}	Output Leakage Current	V_I+ = 1.0 V, V_I− = 0 V, V_O = 30 V		200	nA	1	1
				1.0	μA	1	2,3
I_{IL} (±)	Input Leakage Current	V_{CC}+ = 36 V, V_I+ = 34 V, 0V V_I− = 0V, 34 V	−500	500	ns	4	1,2,3
I_{OL}	Output Sink Current	V_I+ = 0 V, V_I− = 1.0 V, V_O = 1.5 V	6.0		mA	1	1
V_{LAT}	Voltage Latch (High Level Input)	V_I+ = 0 V, V_I− = 10 V, I_{OL} = 4 mA		400	mV	3	1
V_{OL}	Low Level Output Voltage	V_I+ = 0 V, V_I− = 1.0 V, I_{OL} = 4.0 mA		400	mV	1	1
				700	mV	1	2,3
A_{VS}	Large Signal Voltage Gain	V+ = 15 V, R_L = 15 kΩ	25		V/mV	4	4,5,6
CS	Channel Separation	V+ = 30 V	80		dB	4	9
t_{PLH}	Propagation Delay to High Level	V_I = 100 mV, R_L = 5.1 kΩ; V_{OD} = 5.0 mV		7.0	μs	3	10
				5.0	μs	3	9,11
		V_{OD} = 50 mV		1.2	μs	3	10
				0.8	μs	3	9,11
t_{PHL}	Propagation Delay to Low Level	V_I = 100 mV, R_L = 5.1 kΩ; V_{OD} = 5.0 mV		3.0	μs	3	10
				2.5	μs	3	9,11
		V_{OD} = 50 mV		1.0	μs	3	10
				0.8	μs	3	9,11

15

Primary Burn-In Circuit
(38510/11201 may be used by FSC as an alternate)



Equivalent Circuit (1/4 of circuit)



FAIRCHILD

A Schlumberger Company

μA2111QB Dual Voltage Comparator

MIL-STD-883
July 1986—Rev 1[5]

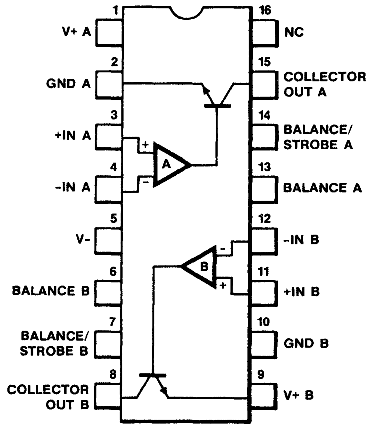
Aerospace and Defense Data Sheet
Linear Products

Description

The μA2111QB is a multi-chip, low input current dual voltage comparator, constructed using the Fairchild Planar Epitaxial process. The μA2111QB operates from the single 5 V integrated circuit logic supply to the standard ±15 V operational amplifier supplies. The μA2111QB is intended for a wide range of applications including driving lamps or relays and switching voltages up to 50 V at currents as high as 50 mA. The output stage is compatible with RTL, DTL, TTL and MOS logic. The input stage current can be raised to increase input slew rate.[6]

- **Low Input Bias Current**
- **Low Input Offset Current**
- **Wide Differential Input Voltage**
- **Power Supply Voltage, Single 5 V To ±15 V**
- **Offset Voltage Null Capability**
- **Strobe Capability**

Connection Diagram
16-Lead DIP
(Top View)



CD01440F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA2111DMQB	EA	D-2 (16-Lead DIP)

JAN Product Available

10305	BEA	D-2 (16-Lead DIP)
10305	BEB	D-2 (16-Lead DIP)

15

Absolute Maximum Ratings

Storage Temperature Range	−65°C to 175°C
Operating Temperature Range	−55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Total Supply Voltage	36 V
Negative Supply Voltage	−30 V
Output to Negative Supply Voltage	50 V
Differential Input Voltage	±30 V
Input Voltage[9]	±15 V
Sink Current	50 mA
Strobe Current	10 mA
Short Circuit Duration	10 s

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to V+.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
9. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less negative.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

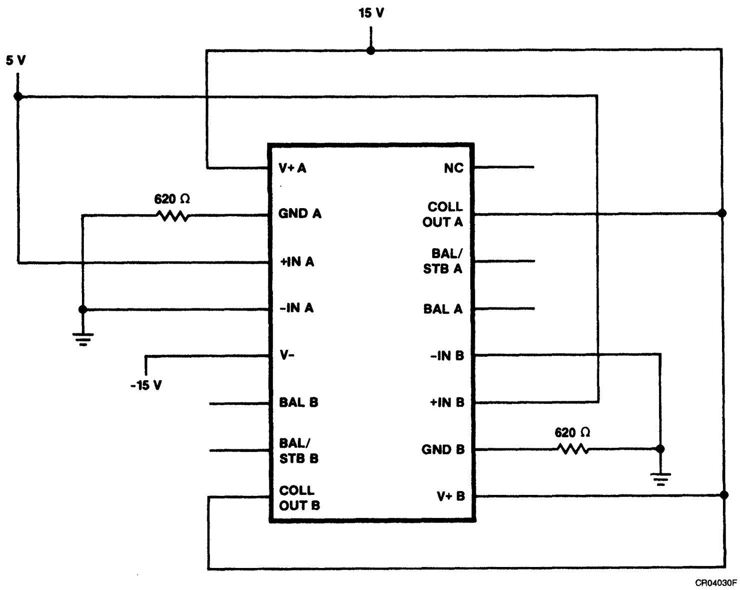
μA2111QB
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$, $-14\ V \leqslant V_{CM} \leqslant 13\ V$		3.0	mV	1	1
				4.0	mV	1	2,3
		$V_{CC} = \pm 2.5$ V, $R_S = 50\ \Omega$, $V_{CM} = 0$ V		3.0	mV	1	1
				4.0	mV	1	2,3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	25°C $\leqslant T_A \leqslant$ 125°C		25	μV/°C	4	2
		−55°C $\leqslant T_A \leqslant$ 25°C		25	μV/°C	4	3
$V_{IO\ adj}$	Input Offset Voltage Adjustment Range		5.0		mV	1	1
$V_{IO\ (R)}$	Raised Input Offset Voltage[7]	$R_S = 50\ \Omega$, $-14.5\ V \leqslant V_{CM} \leqslant 13\ V$ $V_{BAL} = V_{BAL}/STB = V+$		3.0	mV	1	1
				4.5	mV	1	2,3
I_{IO}	Input Offset Current	$R_S = 100\ k\Omega$, $-14.5\ V \leqslant V_{CM} \leqslant 13\ V$		10	nA	1	1,2
				20	nA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity	25°C $\leqslant T_A \leqslant$ 125°C		100	PA/°C	4	2
		−55°C $\leqslant T_A \leqslant$ 25°C		200	PA/°C	4	3
$I_{IO\ (R)}$	Raised Input Offset Current[7]	$R_S = 100\ k\Omega$, $V_{CM} = 0$ V, $V_{BAL} = V_{BAL}/STB = V+$		25	nA	1	1,2
				50	nA	1	3
I_{IB}	Input Bias Current	$R_S = 50\ \Omega$, $V_{CM} = 0$ V		100	nA	1	1,2
				150	nA	1	3
		$R_S = 50\ \Omega$, $-14.5\ V \leqslant V_{CM} \leqslant 13\ V$		150	nA	1	1,2
				200	nA	1	3
I+	Positive Supply Current (per Channel)			6.0	mA	1	1,2
				7.0	mA	1	3
I−	Negative Supply Current (Total)		−10		mA	1	1,2
			−12		mA	1	3
V_{OL1}	Low Level Output Voltage 1	V+ = 4.5 V, V− = 0 V, $V_I+ = -6$ V, $I_{OL} = 8.0$ mA		0.4	V	1	1,2,3
V_{OL2}	Low Level Output Voltage 2	$V_{CC} = \pm 15$ V, $V_I+ = -5.0$ mV, $I_{OL} = 50$ mA		1.5	V	1	1,2,3
I_{CEX}	Output Leakage Current	$V_{CC} = \pm 18$ V, $V_O = 32$ V		10	nA	1	1
				500	nA	1	2
I_{I1}	Input Leakage Current 1	$V_{CC} = \pm 18$ V, $V_I+ = -29$ V		500	nA	1	1,2,3
I_{I2}	Input Leakage Current 2	$V_{CC} = \pm 18$ V, $V_I+ = 29$ V		500	nA	1	1,2,3
V_O	Collector Output Voltage	$R_S = 50\ \Omega$, $I_{ST} = -3.0$ mA	14		V	1	1,2,3

μA2111QB (Cont.)
Electrical Characteristics $V_{CC} = \pm 15$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
CMR	Common Mode Rejection	$R_S = 50\ \Omega$, $-14.5\ V \leq V_{CM} \leq 13\ V$	80		dB	1	1,2,3
I_{OS}	Output Short Circuit Current	10 ms maximum test duration		200	mA	1	1
				150	mA	1	2
				250	mA	1	3
A_{VE}	Large Signal Voltage Gain (Emitter Follower Output)	$R_L = 600\ \Omega$	10		V/mV	1	4
			8		V/mV	1	5,6
t_{PLH}	Propagation Delay to High Level (Collector Output)	$V_{OD} = 5.0$ mV, $C_L = 50$ pF, $V_I = 100$ mV		300	ns	4	9, 11
				600	ns	4	10
t_{PHL}	Propagation Delay to Low Level (Collector Output)			300	ns	4	9, 11
				500	ns	4	10

Primary Burn-In Circuit
(38510/10305 may be used by FSC as an alternate)



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA710QB High Speed Differential Comparator

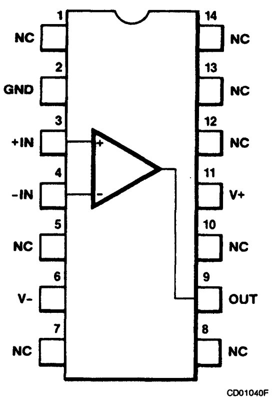
Aerospace and Defense Data Sheet
Linear Products

Description

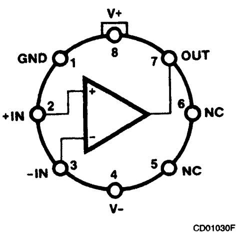
The μA710QB is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar Epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse-height discriminator, a voltage comparator in high speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.[6]

- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Low Offset Voltage Drift**

Connection Diagram 14-Lead DIP (Top View)

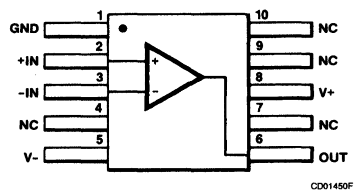


Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 10-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA710DMQB	CA	D-1 (14-Lead DIP)
μA710HMQB	GC	A-1 (8-Lead Can)
μA710FMQB	HA	F-4 (10-Lead Flatpak)

JAN Product Available

10301	BCA	D-1 (14-Lead DIP)
10301	BCB	D-1 (14-Lead DIP)
10301	BGA	A-1 (8-Lead Can)
10301	BGC	A-1 (8-Lead Can)
10301	BHA	F-4 (10-Lead Flatpak)
10301	BHB	F-4 (10-Lead Flatpak)

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to 175°C
Operating Temperature Range	-55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can and Flatpak	330 mW
DIP	400 mW
Positive Supply Voltage	14 V
Negative Supply Voltage	-7 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	±7 V
Short Circuit Duration	10 s

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

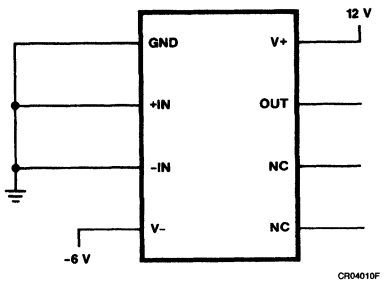
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_C is guaranteed by I+, I−: P_C=(12) (I+) + (6) (I−).
8. V_{IR} is guaranteed by the CMR test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.

μA710QB

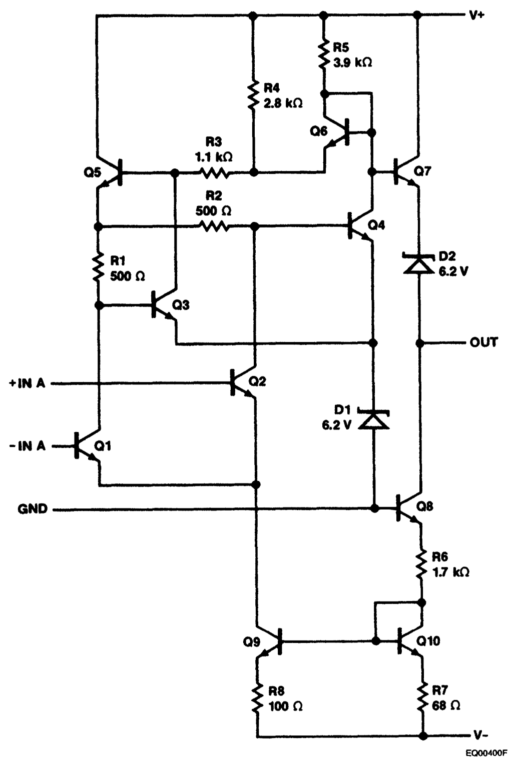
Electrical Characteristics V+ = 12 V, V− = −6 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	50 Ω ≤ R_S ≤ 200 Ω, V_{CM} = 0 V	V_O = 1.4 V		2.0	mV	1	1
			V_O = 1.0 V		3.0	mV	1	2
			V_O = 1.8 V		3.0	mV	1	3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient	25°C ≤ T_A ≤ 125°C			10	μV/°C	4	2
		−55°C ≤ T_A ≤ 25°C			10	μV/°C	4	3
I_{IO}	Input Offset Current	V_{CM} = 0 V	V_O = 1.4 V		3.0	μA	1	1
			V_O = 1.0 V		3.0	μA	1	2
			V_O = 1.8 V		7.0	μA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Coefficient	25°C ≤ T_A ≤ 125°C			25	nA/°C	4	2
		−55°C ≤ T_A ≤ 25°C			75	nA/°C	4	3
I_{IB}	Input Bias Current	V_{CM} = 0 V			20	μA	1	1
					45	μA	1	2,3
I+	Positive Supply Current	V_O = 0 V, V_I− = 10 mV			9.0	mA	1	1,2,3
I−	Negative Supply Current	V_O = 0 V, V_I− = 10 mV		−7.0		mA	1	1,2,3
P_C	Power Consumption	V_O = 0 V, V_I− = 10 mV			150	mW	7	1,2,3
CMR	Common Mode Rejection	V− = −7.0 V, V_{CM} = ±5.0 V, R_S = 200 Ω		80		dB	1	1,2,3
V_{IR}	Input Voltage Range	V− = −7.0 V		±5.0		V	8	1,2,3
V_{OH}	Output Voltage HIGH	V_I+ = 5.0 mV, 0 mA ≤ I_{OH} ≤ 5.0 mA		2.5	4.0	V	1	1,2,3
V_{OL}	Output Voltage LOW	V_I− = 5.0 mV, I_{OL} = 0 mA		−1.0	0	V	1	1,2,3
I_{OL}	Output Sink Current	V_I− = 5.0 mV, V_O = 0 V		2.0		mA	1	1
				0.5		mA	1	2
				1.0		mA	1	3
A_{VS}	Large Signal Voltage Gain			1250		V/V	1	4
				1000		V/V	1	5,6
t_{PLH}	Propagation Delay to High Level	C_L = 5.0 pF, 100 mV step, V_{OD} = 5.0 mV			60	ns	4	9
t_{PHL}	Propagation Delay to Low Level				60	ns	4	9

Primary Burn-In Circuit
(38510/10301 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA711QB
Dual High Speed Differential Comparator

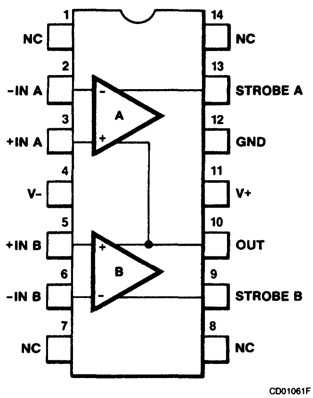
Aerospace and Defense Data Sheet
Linear Products

Description

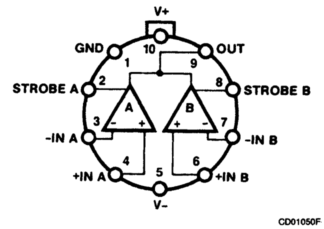
The μA711QB is a dual differential voltage comparator featuring high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double ended limit detector for automatic Go/No-Go test equipment. The μA711QB, which is similar to the μA710QB differential comparator, is constructed using the Fairchild Planar Epitaxial process.[6]

- **Fast Response Time**
- **Low Offset Voltage**
- **Low Offset Current**
- **Independent Comparator Strobing**

Connection Diagram
14-Lead DIP
(Top View)

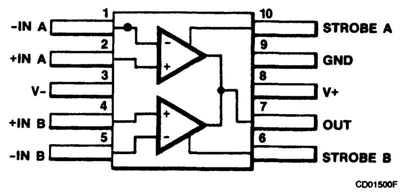


Connection Diagram
10-Lead Can
(Top View)



Lead 5 connected to case.

Connection Diagram
10-Lead Flatpak
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA711DMQB	CA	D-1 (14-Lead DIP)
μA711FMQB	HA	F-4 (10-Lead Flatpak)
μA711HMQB	IC	A-2 (10-Lead Can)

JAN Product Available

10302	BIC	A-2 (10-Lead Can)

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to 175°C
Operating Temperature Range	−55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can	350 mW
DIP	400 mW
Flatpak	330 mW
Positive Supply Voltage	14 V
Negative Supply Voltage	−7 V
Peak Output Current	50 mA
Differential Input Voltage	±5 V
Input Voltage	±7 V
Strobe Voltage	0 V to 6 V
Short Circuit Duration	10 s

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. P_C is guaranteed by I+, I−: $P_C = (12\ V)\ (I+) + (6\ V)\ (I-)$.
8. V_{IR} is guaranteed by the V_{IO} test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and Flatpak and 120°C/W for the DIP.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C

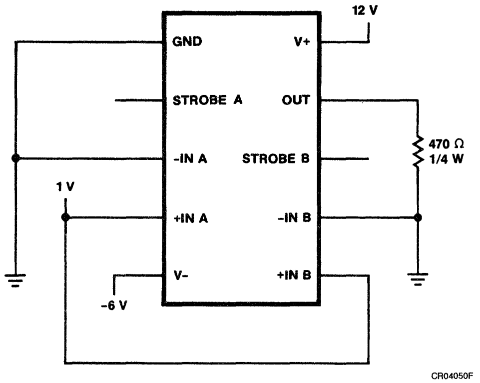
Group C and D Endpoints: Group A, Subgroup 1

μA711QB

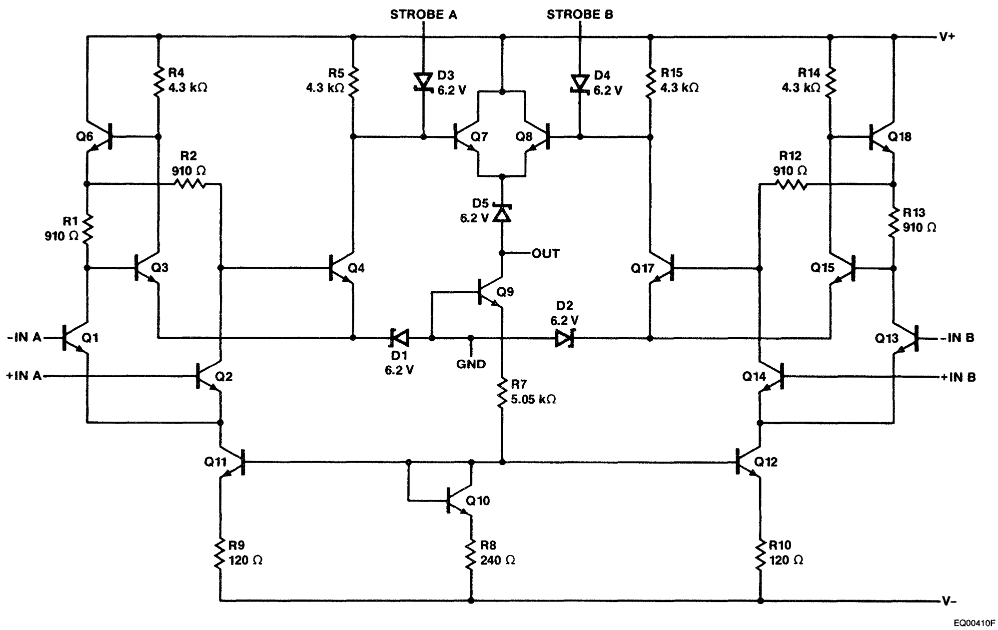
Electrical Characteristics V+ = 12 V, V– = –6 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	50 Ω ≤ R_S ≤ 200 Ω, V_{CM} = 0 V	V_O = 1.4 V		3.5	mV	1	1
			V_O = 1.0 V		4.5	mV	1	2
			V_O = 1.8 V		4.5	mV	1	3
		V– = –7.0 V, R_S = 200 Ω, V_{CM} = ±5.0 V	V_O = 1.4 V		5.0	mV	1	1
			V_O = 1.0 V		6.0	mV	1	2
			V_O = 1.8 V		6.0	mV	1	3
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient	25°C ≤ T_A ≤ 125°C			10	μV/°C	4	2
		–55°C ≤ T_A ≤ 25°C			10	μV/°C	4	3
I_{IO}	Input Offset Current	V_{CM} = 0 V	V_O = 1.4 V		10	μA	1	1
			V_O = 1.0 V		20	μA	1	2
			V_O = 1.8 V		20	μA	1	3
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Coefficient	25°C ≤ T_A ≤ 125°C			25	nA/°C	4	2
		–55°C ≤ T_A ≤ 25°C			75	nA/°C	4	3
I_{IB}	Input Bias Current	V_{CM} = 0 V			75	μA	1	1
					150	μA	1	2,3
I+	Positive Supply Current	V_O = 0 V, V_I– = 5.0 mV			13.3	mA	1	1,2,3
I–	Negative Supply Current	V_O = 0 V, V_I– = 5.0 mV		–6.1		mA	1	1,2,3
P_C	Power Consumption	V_O = 0 V, V_I– = 5.0 mV			200	mW	7	1,2,3
CMR	Common Mode Rejection	V– = –7.0 V, V_{CM} = ±5.0 V, R_S = 200 Ω		80		dB	1	1,2,3
V_{IR}	Input Voltage Range	V– = –7.0 V		±5.0		V	8	1,2,3
V_{OH}	Output High Voltage	V_I+ = 10 mV, 0 mA ≤ I_{OH} ≤ 5.0 mA		2.5	5.0	V	1	1,2,3
V_{OL}	Output Low Voltage	V_I– = 10 mV, I_{OL} = 0 mA		–1.0	0	V	1	1,2,3
V_O (ST)	Strobed Output Level	V_{ST} = 0.3 V		–1.0	0	V	1	1,2,3
I_{OL}	Output Sink Current	V_I– = 10 mV, V_O = 0 V		0.5		mA	1	1,2,3
I_O (ST)	Strobe Current	V_{ST} = 100 mV, V_I+ = 10 mV			2.5	mA	1	1,2,3
A_{VS}	Large Signal Voltage Gain			750		V/V	1	4
				500		V/V	1	5,6
t_{STRL}	Strobe Release Time	C_L = 5.0 pF, V_I+ = 10 mV			15	ns	4	9
t_{PLH}	Propagation Delay to High Level	C_L = 5.0 pF, 100 mV step, V_{OD} = 5.0 mV			90	ns	4	9
t_{PHL}	Propagation Delay to Low Level				60	ns	4	9

Primary Burn-In Circuit
(38510/10302 may be used by FSC as an alternate)



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA760QB High Speed Differential Comparator

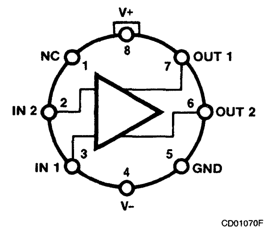
Aerospace and Defense Data Sheet
Linear Products

Description

The μA760QB is a differential voltage comparator offering considerable speed improvement over the μA710QB and operates from symmetric supplies of ±4.5 V to ±6.5 V. The μA760QB can be used in high speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The μA760QB output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.[6]

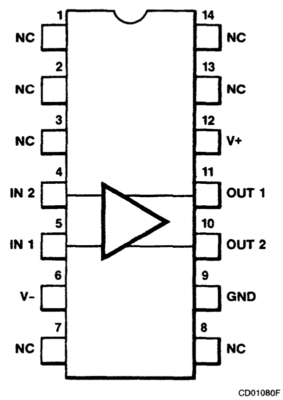
- **Guaranteed High Speed**
- **Guaranteed Delay Matching On Both Outputs**
- **Complementary TTL Compatible Outputs**
- **High Sensitivity**
- **Standard Supply Voltages**

Connection Diagram 8-Lead Can (Top View)



Lead 4 connected to case.

Connection Diagram 14-Lead DIP (Top View)



15

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA760DMQB	CA	D-1 (14-Lead DIP)
μA760HMQB	GC	A-1 (8-Lead Can)

Absolute Maximum Ratings

Storage Temperature Range	−65°C to 175°C
Operating Temperature Range	−55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can	330 mW
DIP	400 mW
Supply Voltage	±8 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage[10]	±8 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

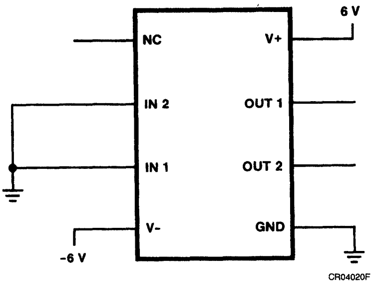
Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Response time measured from the 50% point of a 30 mV_{p-p} 10 MHz sinusoidal input to the 50% point of the output.
8. Response time measured from the 50% point of a 2 V_{p-p} 10 MHz sinusoidal input to the 50% point of the output.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and 120°C/W for the DIP.
10. For supply voltages less than ±8 V, the absolute maximum input voltage is equal to the supply voltage.

μA760QB

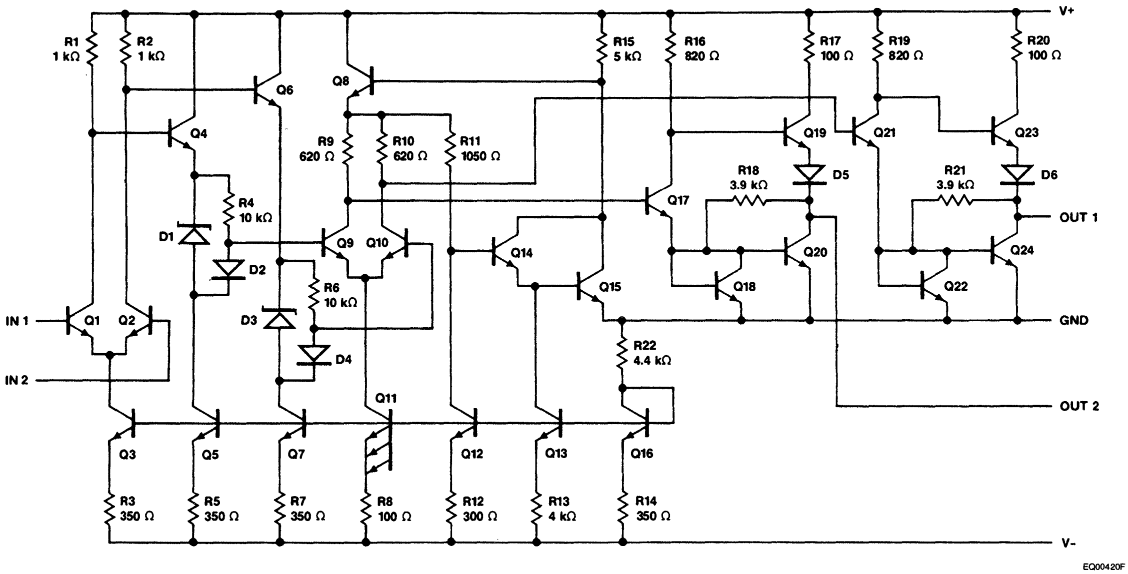
Electrical Characteristics $\pm 4.5\ V \leqslant V_{CC} \leqslant \pm 6.5\ V$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IO}	Input Offset Voltage	$R_S = 50\ \Omega$		6.0	mV	1	1,2,3
I_{IO}	Input Offset Current			7.5	μA	1	1,2,3
I_{IB}	Input Bias Current			60	μA	1	1,2,3
V_{IR}	Input Voltage Range	$V_{CC} = \pm 6.5\ V$	±4.0		V	1	1,2,3
V_{OH}	Output Voltage HIGH (either output)	$V_{CC} = \pm 5.0\ V$, $0\ mA \leqslant I_{OH} \leqslant 5.0\ mA$	2.4		V	1	1,2,3
		$V_{CC} = \pm 4.5\ V$, $I_{OH} = 80\ \mu A$	2.4		V	1	1,2,3
V_{OL}	Output Voltage LOW (either output)	$I_{OL} = 3.2\ mA$		0.4	V	1	1,2,3
I+	Positive Supply Current	$V_{CC} = \pm 6.5\ V$		32	mA	1	1,2,3
I–	Negative Supply Current	$V_{CC} = \pm 6.5\ V$		16	mA	1	1,2,3
t_{PD}	Response Time[7]			30	ns	2	9
t_{PD}	Response Time[8]			25	ns	2	9
	Response Time Difference Between Outputs[7]						
Δt_{PD}	$(t_{PD}$ of $+V_{I1}) - (t_{PD}$ of $-V_{I2})$			5.0	ns	2	9
Δt_{PD}	$(t_{PD}$ of $+V_{I2}) - (t_{PD}$ of $-V_{I1})$			5.0	ns	2	9
Δt_{PD}	$(t_{PD}$ of $+V_{I1}) - (t_{PD}$ of $+V_{I2})$			7.5	ns	2	9
Δt_{PD}	$(t_{PD}$ of $-V_{I1}) - (t_{PD}$ of $-V_{I2})$			7.5	ns	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA55107AQB Dual Line Receiver

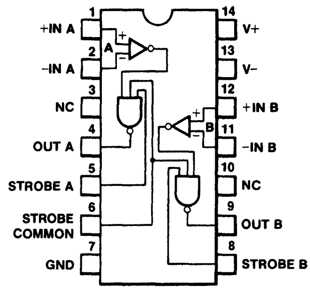
Aerospace and Defense Data Sheet
Linear Products

Description

The μA55107AQB is a high speed, two channel line receiver with common voltage supply and ground terminals. It is designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. It features high input impedance and low input current which induce very little loading on the transmission line systems. The receiver input common mode voltage range is ±3 V but can be increased to ±15 V by the use of input attenuators. The μA55107AQB features an active pull-up (totem-pole output). The receiver is designed to be used with the μA55110AQB line driver. The receiver is useful in high speed balanced, unbalanced and party-line transmission systems and as a data comparator.[6]

- **High Speed**
- **Standard Supply Voltages**
- **Dual Channels**
- **High Common Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Input Common Mode Voltage Range Of ±3 V**
- **Separate Or Common Strobes**
- **Wired-OR Output Capability**
- **High DC Noise Margins**
- **Strobe Input Clamp Diodes**

Connection Diagram 14-Lead DIP (Top View)



CD00930F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA55107ADMQB	CA	D-1 14-Lead DIP

JAN Product Available

10401	BAA	D-1 14-Lead DIP
10401	BAB	D-1 14-Lead DIP
10401	BCA	F-1 14-Lead Flatpak
10401	BCB	F-1 14-Lead Flatpak

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[7]	
DIP	400 mW
Supply Voltage to GND	±7.0 V
Differential Input Voltage[8]	±6.0 V
Input Voltage to GND	±5.0 V
Strobe Input Voltage to GND	5.5 V
Short Circuit Duration[9]	Indefinite

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
8. These votage values are at +IN with respect to −IN.
9. Short circuit to ground. Rating applies to 125°C case temperature or 75°C ambient temperature. No more than one amplifier should be shorted at the same time as the maximum junction temperature will be exceeded.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

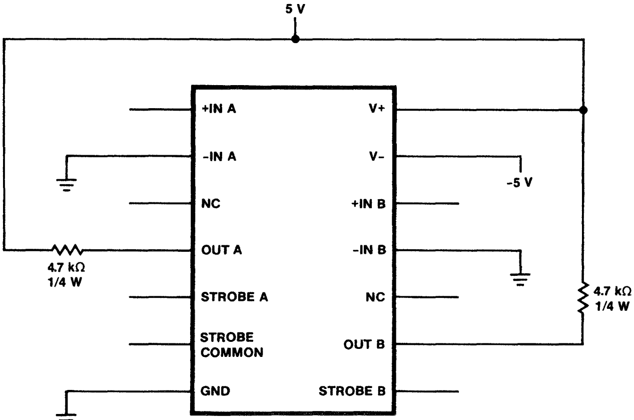
Group C and D Endpoints: Group A, Subgroup 1

μA55107AQB

Electrical Characteristics $V_{CC} = \pm 5.5$ V, unless otherwise specified.

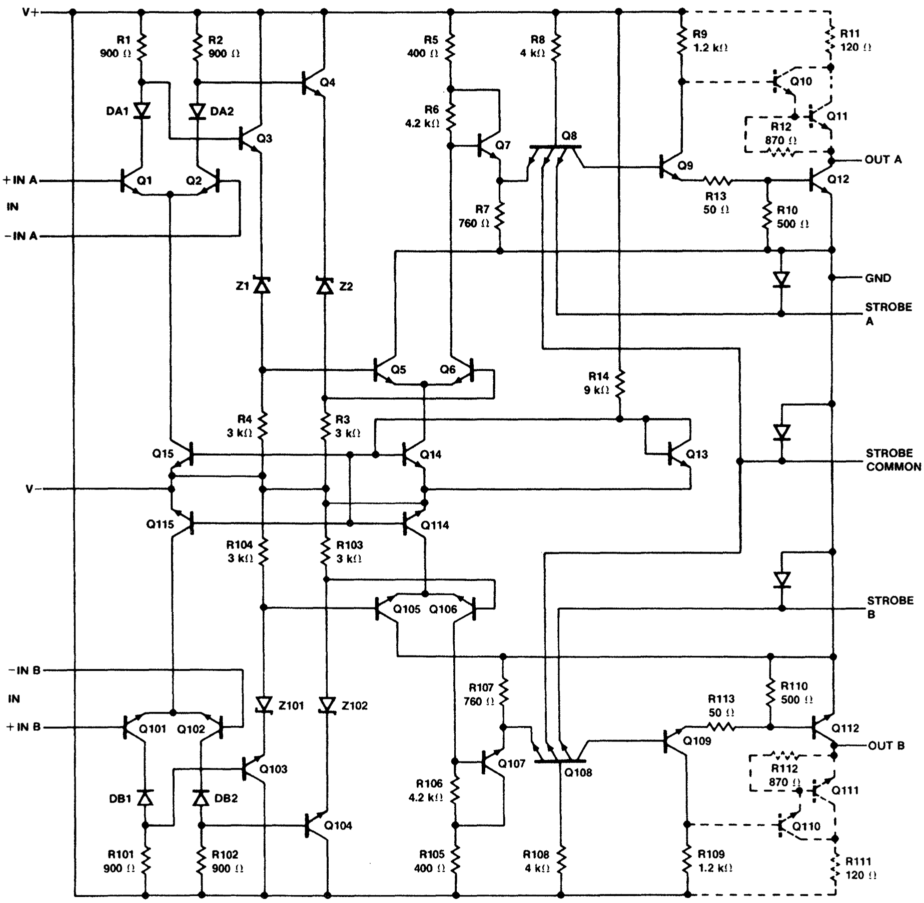
Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
I_{IH1}	Input Current HIGH into 1A or 2A	$V_{DIFF} = 0.5$ V, $V_{CM} = \pm 3.0$ V			75	μA	1	1,2,3
I_{IL1}	Input Current LOW into 1A or 2A	$V_{DIFF} = -2.0$ V, $V_{CM} = \pm 3.0$ V		−10		μA	1	1,2,3
I_{IH4}	Input Current HIGH into 1G or 2G	$V_G = 2.4$ V			40	μA	1	1,2,3
I_{IH5}		$V_G = 5.5$ V			1.0	mA	1	1,2,3
I_{IL2}	Input Current LOW into 1G or 2G	$V_G = 0.4$ V		−1.6		mA	1	1,2,3
I_{IH2}	Input Current HIGH into S	$V_{ST} = 2.4$ V			80	μA	1	1,2,3
I_{IH3}		$V_{ST} = 5.5$ V			2.0	mA	1	1,2,3
I_{IL3}	Input Current LOW into S	$V_{ST} = 0.4$ V		−3.2		mA	1	1,2,3
V_{OH}	Output Voltage HIGH	$I_{OH} = -400$ μA	V+ = 4.5 V	2.4		V	1	1,2,3
		$V_{CM} = \pm 3.0$ V	V− = −4.5 V	2.4		V	1	1,2,3
V_{OL}	Output Voltage LOW	$I_{OL} = 16$ mA	V+ = 4.5 V		0.4	V	1	1,2,3
		$V_{CM} = \pm 3.0$ V	V− = −4.5 V		0.4	V	1	1,2,3
I_{OS}	Output Short Circuit Current	$V_O = 0$ V		−70	−18	mA	1	1,2,3
I+	Positive Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ mA			30	mA	1	1,2,3
I−	Negative Supply Current	$V_O = V_{OH}$, $I_{OH} = 0$ mA		−15		mA	1	1,2,3
t_{PLH1}	Propagation Delay to High Level (Inputs A&B to Output)	$V_{CC} = \pm 5.0$ V, $R_L = 390$ Ω, $C_L = 50$ pF (*See Fig. 1*)			25	ns	1	9
					40	ns	3	10,11
t_{PHL1}	Propagation Delay to Low Level (Inputs A&B to Output)				25	ns	1	9
					35	ns	3	10,11
t_{PLH2}	Propagation Delay to High Level (Strobe Inputs G or S to Output)				15	ns	1	9
					30	ns	3	10,11
t_{PHL2}	Propagation Delay to Low Level (Strobe Inputs G or S to Output)				15	ns	1	9
					25	ns	3	10,11

Primary Burn-In Circuit
(38510/10401 may be used by FSC as an alternate)



CR04910F

Equivalent Circuit



EQ00310F

μA55110AQB Dual Line Driver

MIL-STD-883
July 1986—Rev 1[5]

Aerospace and Defense Data Sheet
Linear Products

Description

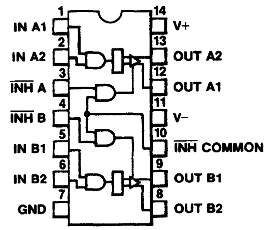
The μA55110AQB has improved output current regulation with supply voltage and temperature variations. The higher current outputs allow data to be transmitted over longer lines. It offers optimum performance when used with the μA55107AQB Line Receiver.

It features independent channels with common voltage supply and ground terminals. The driver features a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by LOW logic levels on the inhibit inputs.

The inhibit feature is provided so the circuit can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, I_O(OFF), is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high; the output impedance of output transistor is biased to cutoff.[6]

- **No Output Transients On Power-Up Or Down**
- **Improved Stability Over Supply Voltage And Temperature Ranges**
- **Constant Current, High Impedance Outputs**
- **High Speed**
- **Standard Supply Voltages**
- **Inhibitor Available For Driver Selection**
- **High Common Mode Output Voltage Range**
- **TTL Input Compatibility**

Connection Diagram
14-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA55110ADMQB	CA	D-1 14-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Supply Voltage to GND	±7.0 V
Input Voltage to GND	5.5 V
Output Voltage	−5.0 V to +12 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

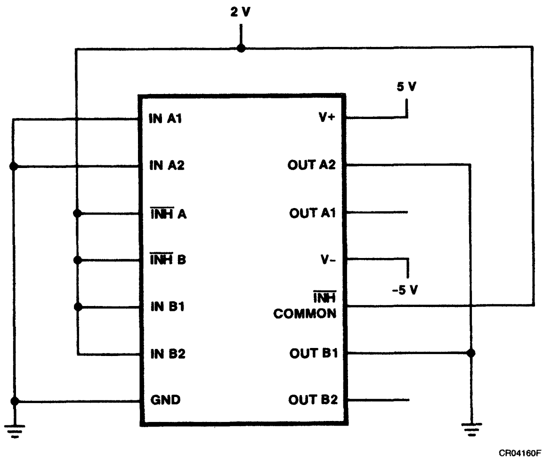
Group C and D Endpoints: Group A, Subgroup 1

μA55110AQB
Electrical Characteristics

Symbol	Characteristic		Condition	Min	Max	Unit	Note	Subgrp
V_{IH}	Input Voltage HIGH		$\pm 4.5\ V \leqslant V_{CC} \leqslant \pm 5.5\ V$	2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW		$\pm 4.5\ V \leqslant V_{CC} \leqslant \pm 5.5\ V$		0.8	V	1	1,2,3
V_{IC}	Input Clamp Voltage		$V_{CC} = \pm 4.5\ V,\ I_I = -12\ mA$	-1.5		V	4	1
$I_O(ON)$	On-State Output Current		$V_{CC} = \pm 5.5\ V,\ V_O = 10\ V$		15	mA	1	1,2,3
			$V_{CC} = \pm 4.5\ V,\ V_O = -3.0\ V$	6.5		mA	1	1,2,3
$I_O(OFF)$	Off-State Output Current		$V_{CC} = \pm 4.5\ V,\ V_O = 10\ V$		100	μA	1	1,2,3
$I_{I\ Max}$	Input Current at Maximum Input Voltage	A, B, or C Inputs	$V_{CC} = \pm 5.5\ V,\ V_I = 5.5\ V$		1.0	mA	1	1,2,3
		D Input	$V_{CC} = \pm 5.5\ V,\ V_I = 5.5\ V$		2.0	mA	1	1,2,3
I_{IH}	Input Current HIGH	A, B, or C Inputs	$V_{CC} = \pm 5.5\ V,\ V_I = 2.4\ V$		40	μA	1	1,2,3
		D Input	$V_{CC} = \pm 5.5\ V,\ V_I = 2.4\ V$		80	μA	1	1,2,3
I_{IL}	Input Current LOW	A, B, or C Inputs	$V_{CC} = \pm 5.5\ V,\ V_I = 0.4\ V$	-3.0		mA	1	1,2,3
		D Input	$V_{CC} = \pm 5.5\ V,\ V_I = 0.4\ V$	-6.0		mA	1	1,2,3
I+(ON)	Positive Supply Current from V+ with driver enabled		$V_{CC} = \pm 5.5\ V$, A & B inputs at 0.4 V, C & D inputs at 2.0 V		35	mA	1	1,2,3
I−(ON)	Negative Supply Current from V− with driver enabled			-50		mA	1	1,2,3
t_{PLH1}	Propagation Delay to High Level	Inputs A or B to Y or Z	$V_{CC} = \pm 5.0\ V,\ R_L = 50\ \Omega$, $C_L = 40\ pF$ (*See Fig. 1*)		15	ns	1	9
t_{PHL1}	Propagation Delay to Low Level				15	ns	1	9
t_{PLH2}	Propagation Delay to High Level	Inputs C or D to Y or Z			25	ns	1	9
t_{PHL2}	Propagation Delay to Low Level				25	ns	1	9

16

Primary Burn-In Circuit



Equivalent Circuit

Refer to the Fairchild Linear Data Book Commercial Section

FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA55452BQB Dual NAND Peripheral Driver

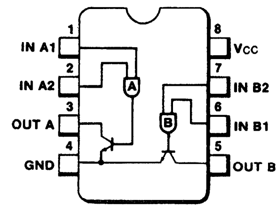
Aerospace and Defense Data Sheet
Linear Products

Description

The μA55452BQB is a dual high speed general purpose interface driver that converts TTL and DTL logic levels to high current drive capability. The μA55452BQB features two standard series 74 TTL gates in AND configurations driving the base of two high voltage, high current, uncommitted collector output transistors. The μA55452BQB can be used in designing high speed logic buffers, power drivers, lamp drivers, line drivers, MOS drivers, clock drivers and memory drivers.[6]

- **No Latch-Up Up to 20 V**
- **High Output Current Capability**
- **TTL or DTL Input Compatible**
- **Input Clamp Diodes**
- **+5 V Supply Voltage**

Connection Diagram
8-Lead DIP
(Top View)



CD00241F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA55452BRMQB	PA	D-4 8-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[7]	
DIP	400 mW
Supply Voltage Range[8]	7.0 V
Input Voltage[8]	5.5 V
Inter-Emitter Voltage[9]	5.5 V
Output Voltage[8,10]	30 V
Continuous Output Current[11]	300 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

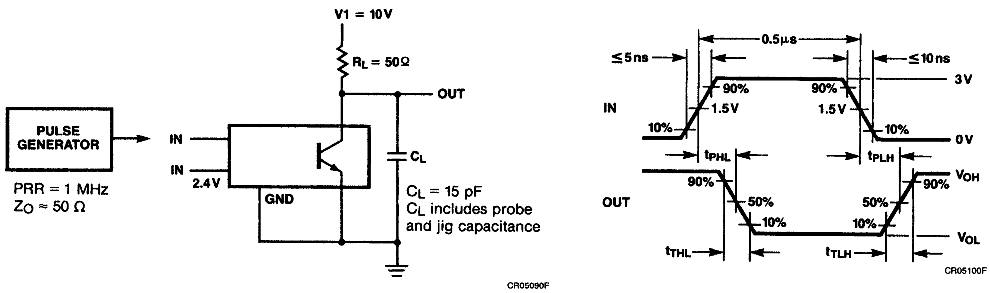
Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
8. Voltage with respect to network ground.
9. Voltage between two emitters of a multiple emitter input transistor.
10. Voltage which should be applied to any output when it is in the off state.
11. Both channels may conduct simultaneously.

Figure 1 Switching Time Test Circuit and Waveforms

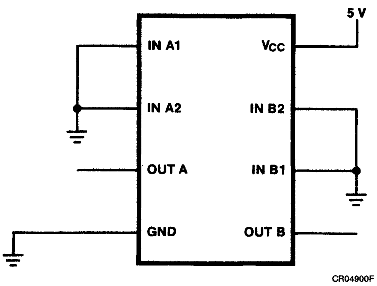


μA55452BQB
Electrical Characteristics

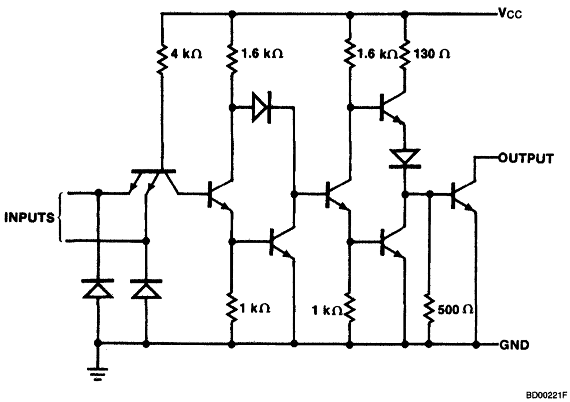
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{IH}	Input Voltage HIGH		2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW			0.8	V	1	1,2,3
V_{IC}	Input Clamp Diode Voltage	V_{CC} = 4.5 V, I_I = −12 mA	−1.5		V	1	1,2,3
I_{OH}	Output Current HIGH	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{OH} = 30 V		100	μA	1	1
				300	μA	1	2,3
V_{OL}	Output Voltage LOW	V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 100 mA		0.4	V	1	1
				0.5	V	1	2,3
		V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 300 mA		0.7	V	1	1
				0.8	V	1	2,3
$I_{I\ Max}$	Input Current at Maximum Input Voltage	V_{CC} = 5.25 V, V_I = 5.5 V		1.0	mA	1	1,2,3
I_{IH}	Input Current HIGH	V_{CC} = 5.5 V, V_I = 2.4 V		40	μA	1	1,2,3
I_{IL}	Input Current LOW	V_{CC} = 5.5 V, V_I = 0.4 V	−1.6		mA	1	1,2,3
I_{CCH}	Supply Current, Output HIGH	V_{CC} = 5.5 V, V_I = 0 V		14	mA	1	1,2,3
I_{CCL}	Supply Current, Output LOW	V_{CC} = 5.5 V, V_I = 5.0 V		71	mA	1	1,2,3
t_{PLH}	Propagation Delay to High Level	V_{CC} = 5.0 V, I_O = 200 mA, C_L = 15 pF, R_L = 50 Ω (*See Fig. 1*)		35	ns	2	9
t_{PHL}	Propagation Delay to Low Level			35	ns	2	9
t_{TLH}	Transition Time, LOW to HIGH			8.0	ns	2	9
t_{THL}	Transition Time, HIGH to LOW			12	ns	2	9

16

Primary Burn-In Circuit



Equivalent Circuit (1/2 of circuit)



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA9614QB Dual Differential Line Driver

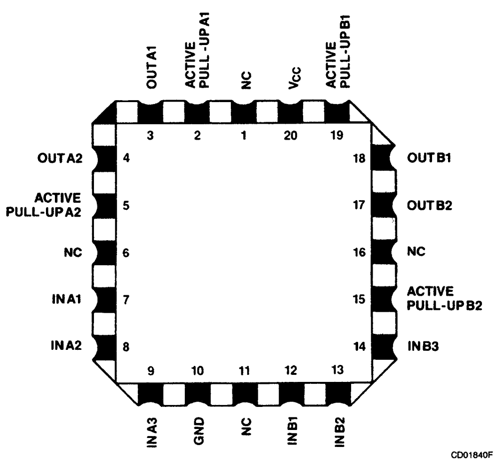
Aerospace and Defense Data Sheet
Linear Products

Description

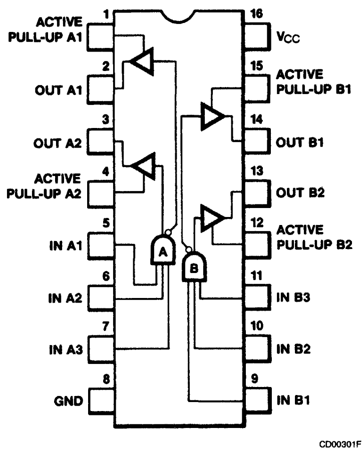
The μA9614QB is a TTL compatible dual differential line driver. It is designed to drive transmission lines either differentially or single ended, back matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent leads. This allows multiplex operation (wired-OR) at the driving site in either the single ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other. The active pull-up is short circuit protected and offers a low output impedance to allow back matching. The two pairs of outputs are complementary, providing NAND and AND functions of the inputs and adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.[6]

- **Single 5 V Supply**
- **TTL Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Output Clamp Diodes For Termination Of Line Transients**
- **Complementary Outputs For NAND/AND Operation**
- **Uncommitted Collector Outputs For Wired-OR Application**

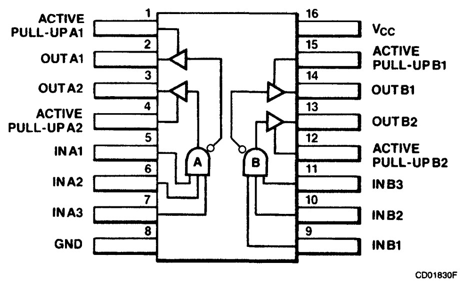
Connection Diagram 20-Terminal CCP (Top View)



Connection Diagram 16-Lead DIP (Top View)



Connection Diagram 16-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9614DMQB	EA	D-2 16-Lead DIP
μA9614FMQB	FA	F-5 16-Lead Flatpak
μA9614LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10403	BEA	D-2 16-Lead DIP
10403	BEB	D-2 16-Lead DIP
10403	BFA	F-5 16-Lead Flatpak
10403	BFB	F-5 16-Lead Flatpak

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP, Flatpak, and CCP	400 mW
Supply Voltage Range	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IH} and V_{IL} are guaranteed by the V_{OL}, V_{OH1}, and V_{OH2} tests.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition B, PDA calculated using Method 5005, Subgroup 1

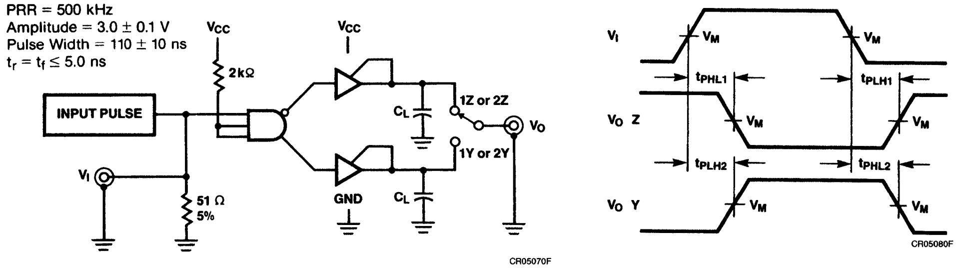
Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Figure 1 Switching Time Test Circuit and Waveforms

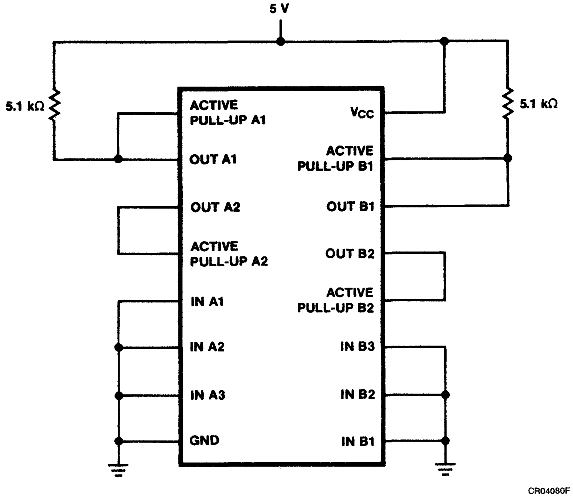
Input Pulse
PRR = 500 kHz
Amplitude = 3.0 ± 0.1 V
Pulse Width = 110 ± 10 ns
$t_r = t_f \leq 5.0$ ns



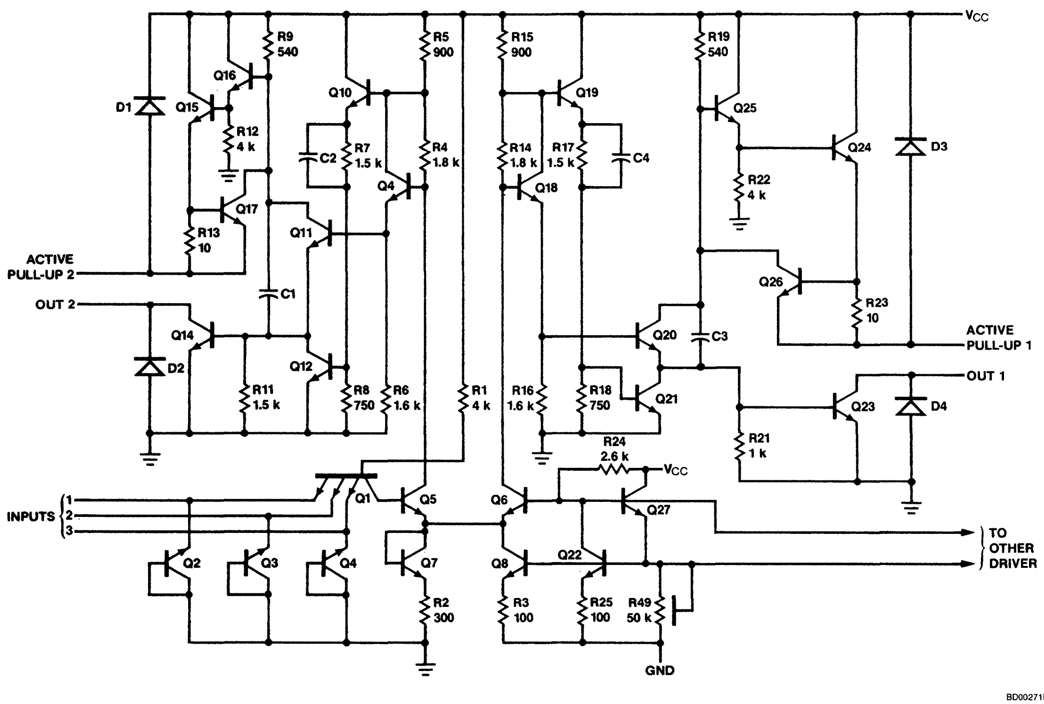
μA9614QB
Electrical Characteristics 4.5 V $\leqslant V_{CC} \leqslant$ 5.5 V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{OL}	Output Voltage LOW	I_{OL} = 40 mA		400	mV	1	1,2,3
V_{OH1}	Output Voltage 1 HIGH	I_{OH} = −10 mA	2.4		V	1	1,2,3
V_{OH2}	Output Voltage 2 HIGH	I_{OH} = −20 mA	2.0		V	1	1,2,3
I_{OS}	Output Short Circuit Current	V_{CC} = 5.5 V, V_O = 0 V	−120	−40	mA	1	1,2,3
I_{CEX}	Output Leakage Current	V_{CC} = 5.5 V, V_{CEX} = 12 V		100	μA	1	1
				200	μA	1	2,3
I_{IL}	Low Level Input Current	V_{CC} = 5.5 V, V_I = 0.4 V	−1.6		mA	1	1,2,3
I_R	Input Reverse Current	V_{CC} = 5.5 V, V_I = 4.5 V		60	μA	1	1
				100	μA	1	2
V_{IH}	Input Voltage HIGH[7]		2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW[7]			0.8	V	1	1,2,3
V_{OC}	Clamped Output Voltage LOW	V_{CC} = 5.5 V, I_{OC} = −40 mA	−1.5		V	1	1
I_{CC}	Supply Current	V_{CC} = 5.5 V, Inputs = 0 V		50	mA	1	1,2,3
I_{Max}	Supply Current Maximum	V_{CC} = 7.0 V, Inputs = 0 V		65	mA	1	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IC} = −12 mA	−1.5		V	1	1
I_{IH1}	High Level Input Current (Inputs 1, 2, & 3)	V_{CC} = 5.5 V, V_I = 2.4 V		40	μA	3	1
				100	μA	4	2,3
I_{IH2}	High Level Input Current (Inputs 1, 2, & 3)	V_{CC} = 5.5 V, V_I = 5.5 V		100	μA	4	1,2,3
B_{VI}	High Level Input Breakdown Voltage	V_{CC} = 5.5 V, I_I = 1.0 mA	5.5		V	1	1
t_{PLH1}	Propagation Delay to High Level (Input to 1Z or 2Z)	V_{CC} = 5.0 V, C_L = 30 pF, VM = 1.5 V (*See Fig. 1*)		20	ns	2	9
				32	ns	3	10, 11
t_{PHL1}	Propagation Delay to Low Level (Input to 1Z or 2Z)			20	ns	2	9
				30	ns	3	10, 11
t_{PLH2}	Propagation Delay to High Level (Input to 1Y or 2Y)			20	ns	2	9
				30	ns	3	10, 11
t_{PHL2}	Propagation Delay to Low Level (Input to 1Y or 2Y)			20	ns	2	9
				32	ns	3	10, 11

Primary Burn-In Circuit
(38510/10403 may be used by FSC as an alternate)



Equivalent Circuit (1/2 of circuit)



Note
All resistor values in ohms.

MIL-STD-883
July 1986—Rev 2[5]

μA9615QB Dual Differential Line Receiver

Aerospace and Defense Data Sheet
Linear Products

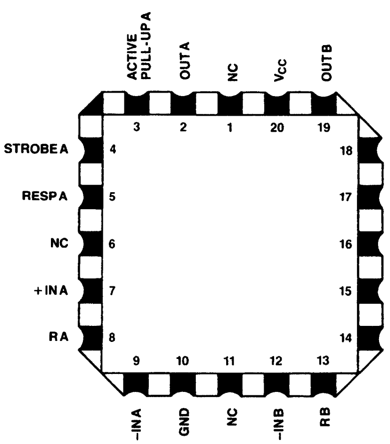
Description

The μA9615QB is a dual differential line receiver designed to receive differential digital data from transmission lines and operate using a single 5 V supply. It can receive differential data in the presence of high level (± 15 V) common mode voltages and deliver undisturbed TTL logic to the output.

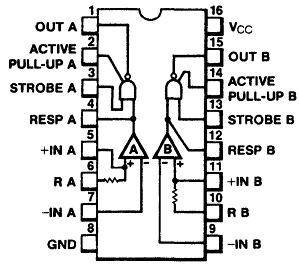
The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent lead to allow either wired-OR or active pull-up TTL output configuration.[6]

- **TTL Compatible Output**
- **High Common Mode Voltage Range**
- **Choice Of An Uncommitted Collector Or Active Pull-Up**
- **Strobe**
- **Single 5 V Supply**
- **Frequency Response Control**
- **130 Ω Terminating Resistor**

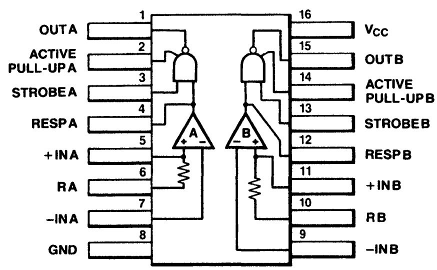
Connection Diagram 20-Terminal CCP (Top View)



Connection Diagram 16-Lead DIP (Top View)



Connection Diagram 16-Lead Flatpak (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9615DMQB	EA	D-2 16-Lead DIP
μA9615FMQB	FA	F-5 16-Lead Flatpak
μA9615LMQB	2C	C-2 20-Terminal CCP

JAN Product Available

10404	BEA	D-2 16-Lead DIP
10404	BEB	D-2 16-Lead DIP
10404	BFA	F-5 16-Lead Flatpak
10404	BFB	F-5 16-Lead Flatpak

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
DIP, Flatpak, and CCP	400 mW
Supply Voltage Range	-0.5 V to +7.0 V
Input Voltage	
Data Inputs	±20 V
Strobe Inputs	-0.5 V to +5.5 V
Voltage Applied to Outputs for High output state without Active Pull-up	-0.5 V to +13.2 V

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Connect Output A to Active Pull-up A and connect Output B to Active Pull-up B.
8. V_{DIFF} is a differential input voltage referred from +IN A to −IN A and from +IN B to −IN B.
9. V_{IR} is guaranteed by the V_{OL} and V_{OH} tests.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

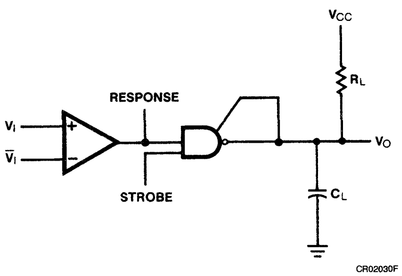
Burn-In: Method 1015, Condition B, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

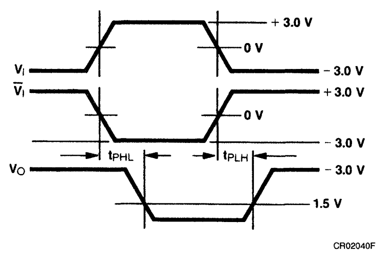
Group A Electrical Tests Subgroups:
1. Static test at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Figure 1 Switching Time Test Circuit and Waveforms



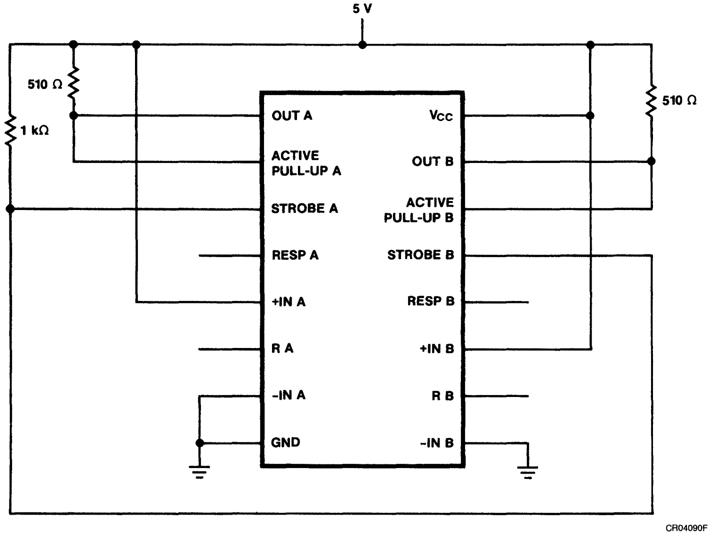
Use V_I or $\overline{V}_I$, ground other input.



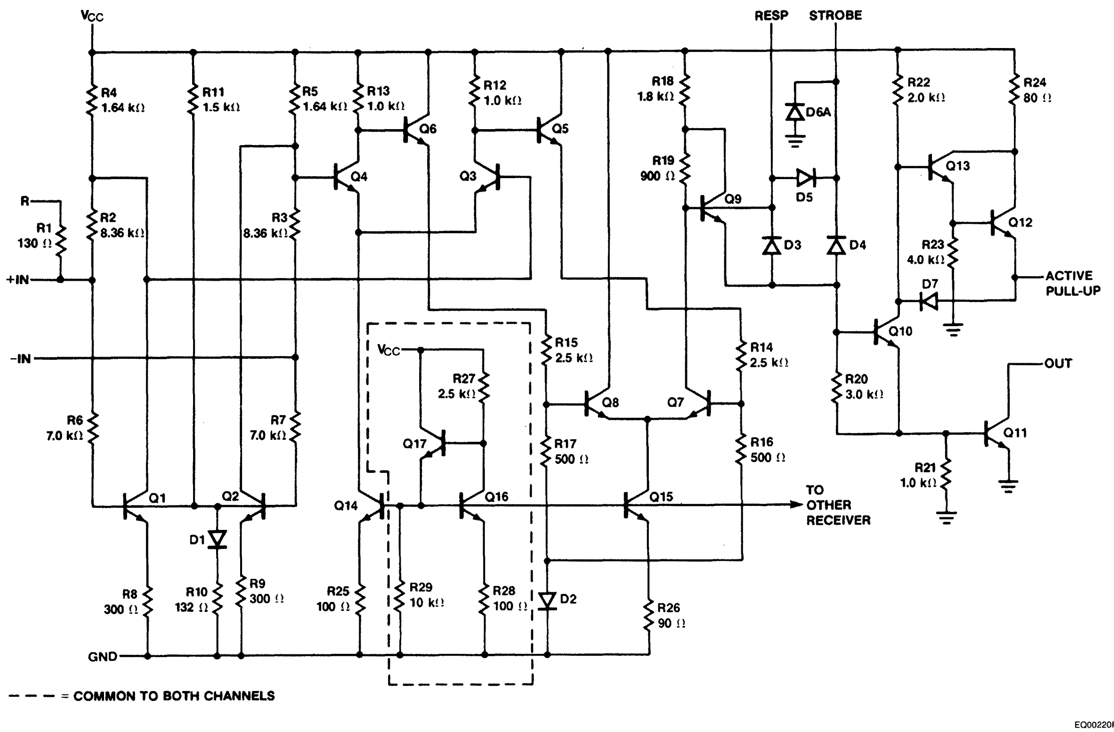
μA9615QB
Electrical Characteristics

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{OL}	Output Voltage LOW[7,8]	$V_{CC} = 4.5$ V, $I_{OL} = 15$ mA, $V_{DIFF} = 0.5$ V		0.40	V	1	1,2,3
V_{OH}	Output Voltage HIGH[7,8]	$V_{CC} = 4.5$ V, $I_{OH} = -5.0$ mA, $V_{DIFF} = -0.5$ V	2.4		V	1	1,2
			2.2		V	1	3
I_{CEX}	Output Leakage Current[8]	$V_{CC} = 4.5$ V, $V_{CEX} = 12$ V, $V_{DIFF} = 4.5$ V		100	μA	1	1
				200	μA	1	2,3
I_{OS}	Output Short Circuit Current[7,8]	$V_{CC} = 5.5$ V, $V_O = 0$ V, $V_{DIFF} = -0.5$ V	−80	−15	mA	1	1,2,3
I_{IL1}	Low Level Input Current (Data Input)	$V_{CC} = 5.5$ V, $V_I = 0.4$ V, Other Input = 5.5 V	−0.7		mA	1	1,2
			−0.9		mA	1	3
I_{IL2}	Low Level Input Current[8] (Strobe)	$V_{CC} = 5.5$ V, $V_I = 0.4$ V, $V_{DIFF} = 0.5$ V	−2.4		mA	1	1
			−2.4		mA	4	2,3
I_{IL3}	Low Level Input Current[8] (Response Control)	$V_{CC} = 5.5$ V, $V_{DIFF} = 0.5$ V		−1.2	mA	1	1
				−1.2	mA	4	2,3
V_{IR}	Input Voltage Range[9]	$V_{CC} = 5.0$ V, $V_{DIFF} = 1.0$ V	−15	15	V	1	1,2,3
I_{IH}	High Level Input Current[8] (Strobe)	$V_{CC} = 4.5$ V, $V_{DIFF} = -0.5$ V, $V_R = 4.5$ V		2.0	μA	1	1
				5.0	μA	1	2,3
R_I	Input Resistor	$V_{CC} = 5.0$ V, $V_I(R) = 1.0$ V, +Input = GND	77	167	Ω	1	1
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = 4.5$ V, $V_{CM} = 0$ V	−500	500	mV	1	1,2,3
		$V_{CC} = 5.0$ V, $V_{CM} = \pm 15$ V	−1.0	1.0	V	1	1,2,3
I_{CC}	Supply Current	$V_{CC} = 5.5$ V, −Inputs = 0 V, +Inputs = 0.5 V		50	mA	1	1,2,3
V_{IC}	Input Clamp Voltage (Strobe)	$V_{CC} = 4.5$ V, $I_{IC} = -12$ mA	−1.5		V	3	1
B_{VI}	High Level Input Breakdown Voltage (Strobe)	$V_{CC} = 5.5$ V, $I_I = 1.0$ mA	5.5		V	4	1,2,3
t_{PLH1}	Propagation Delay to High Level (Inputs A and B to Output)	$V_{CC} = 5.0$ V, $C_L = 30$ pF, $R_L = 3.9$ kΩ *(See Fig. 1)*		50	ns	2	9
				75	ns	3	10, 11
t_{PHL1}	Propagation Delay to Low Level (Inputs A and B to Output)	$V_{CC} = 5.0$ V, $C_L = 30$ pF, $R_L = 390$ Ω *(See Fig. 1)*		50	ns	2	9
				75	ns	3	10, 11
t_{PHL2}	Propagation Delay to Low Level (Strobe to Output)	$V_{CC} = 5.0$ V, $C_L = 30$ pF, $R_L = 390$ Ω		15	ns	4	9
				22	ns	3	10, 11
t_{PLH2}	Propagation Delay to High Level (Strobe to Output)	$V_{CC} = 5.0$ V, $C_L = 30$ pF, $R_L = 3.9$ kΩ		15	ns	4	9
				25	ns	3	10, 11

Primary Burn-In Circuit
(38510/10404 may be used by FSC as an alternate)



Equivalent Circuit (1/2 of circuit)



FAIRCHILD

A Schlumberger Company

μA9616HQB Triple Line Driver

MIL-STD-883
July 1986—Rev 2[5]

Aerospace and Defense Data Sheet
Linear Products

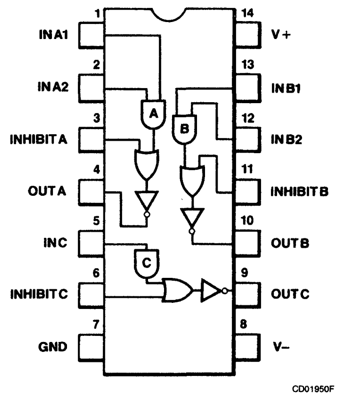
Description

The μA9616HQB is a triple line driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C. Each driver converts TTL/DTL logic levels to EIA/CCITT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

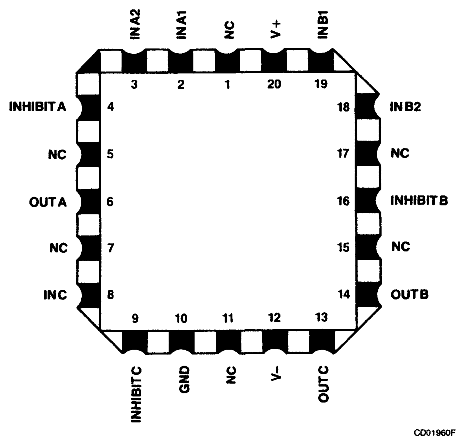
For the complementary function, see the μA9627QB Dual EIA RS-232-C and MIL-STD-188C Line Receiver.[6]

- **Internal Slew Rate Limiting**
- **Meets EIA RS-232-C And CCITT V.24 And/Or MIL-STD-188C**
- **Logic True Inhibit Function**
- **Output Short Circuit Current-Limiting**
- **Output Voltage Levels Independent Of Supply Voltages**

Connection Diagram 14-Lead DIP (Top View)



Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9616HDMQB	CA	D-1 14-Lead DIP
μA9616HLMQB	2C	C-2 20-Terminal CCP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
DIP and CCP	400 mW
Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 V to +6.0 V
Output Signal Voltage	±15 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

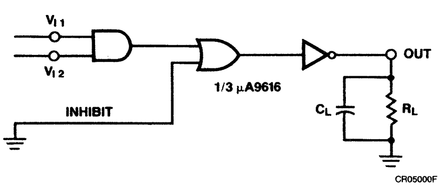
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

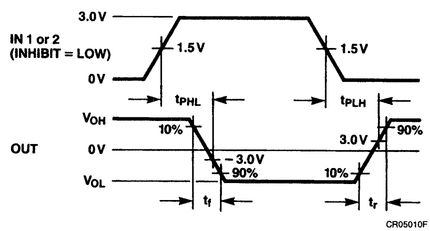
Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IH} and V_{IL} are guaranteed by the V_{OH} and V_{OL} tests.
8. All input and supply leads are grounded.
9. An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Figure 1 Switching Time Test Circuit and Waveforms



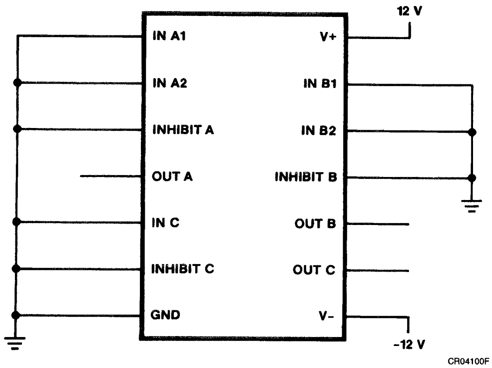


Omit $V_{I\,2}$ for channel 'C'.
Input: PRR = 50 kHz
Pulse Width = 20 μs
$t_r = t_f = 10 \pm 5.0$ ns

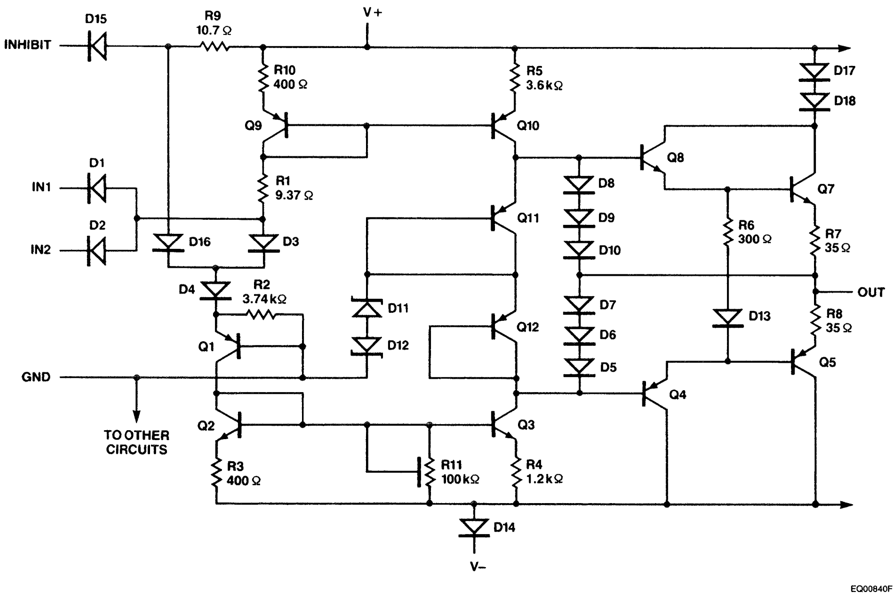
μA9616HQB
Electrical Characteristics $\pm 10.8\ V \leq V_{CC} \leq \pm 13.2\ V$, $R_L = 3.0\ k\Omega$, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{OH}	Output Voltage HIGH	V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8\ V$	5.0	7.0	V	1	1,2,3
V_{OL}	Output Voltage LOW	$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0\ V$	−7.0	−5.0	V	1	1,2,3
V_{OH} to V_{OL}	Output Voltage HIGH to Output Voltage LOW Magnitude Matching Error			±10	%	1	1,2,3
I_{OS+}	Positive Output Short Circuit Current	$R_L = 0\ \Omega$, V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8\ V$	−45	−12	mA	1	1,2,3
I_{OS-}	Negative Output Short Circuit Current	$R_L = 0\ \Omega$, $V_{I1} = V_{I2} = V_{INHIBIT} = 2.0\ V$	12	60	mA	1	1,2,3
V_{IH}	Input Voltage HIGH[7]		2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW[7]			0.8	V	1	1,2,3
I_{IH}	Input Current HIGH	$V_{I1} = V_{I2} = 2.4\ V$		40	μA	1	1,2,3
		$V_{I1} = V_{I2} = 5.5\ V$		1.0	mA	1	1,2,3
I_{IL}	Input Current LOW	$V_{I1} = V_{I2} = 0.4\ V$	−1.6		mA	1	1,2,3
I+	Positive Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8\ V$		25	mA	1	1,2,3
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0\ V$		15	mA	1	1,2,3
I−	Negative Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8\ V$	−1.0		mA	1	1,2,3
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0\ V$	−25		mA	1	1,2,3
R_O	Output Resistance, Power Off[8]	$-2.0\ V \leq V_O \leq 0.5\ V$	300		Ω	1	1,2,3
SR+	Positive Slew Rate[9]	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (*See Fig. 1*)	4.0	30	V/μs	1	9
			4.0	30	V/μs	2	10,11
SR−	Negative Slew Rate[9]	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (*See Fig. 1*)	−30	−4.0	V/μs	1	9
			−30	−4.0	V/μs	2	10,11

Primary Burn-In Circuit



Equivalent Circuit (1/3 of circuit)



FAIRCHILD

A Schlumberger Company

μA9622QB
Dual Line Receiver

MIL-STD-883
July 1986—Rev 1[5]

Aerospace and Defense Data Sheet
Linear Products

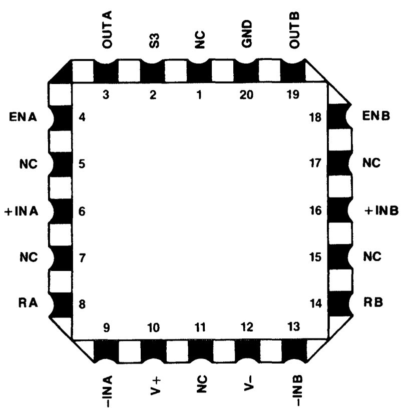
Description

The μA9622QB is a dual line receiver designed to discriminate a worst case logic swing of 2 V from a ±10 V common mode noise signal or ground shift. A 1.5 V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors.

The μA9622QB allows the choice of output states with the input open, without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to 12 V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.[6]

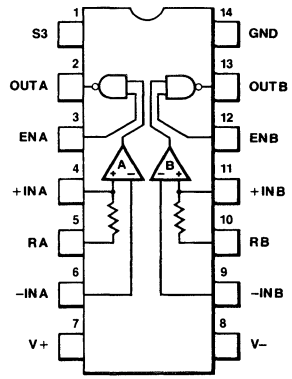
- **TTL Compatible Threshold Voltage**
- **Input Terminating Resistors**
- **Choice Of Output State With Inputs Open**
- **TTL Compatible Output**
- **High Common Mode**
- **Wired-OR Capability**
- **Enable Inputs**
- **Logic Compatible Supply Voltages**

Connection Diagram
20-Terminal CCP
(Top View)



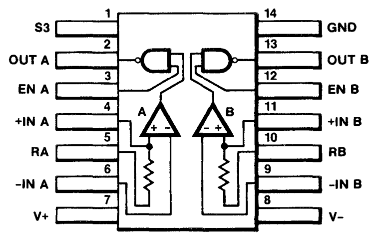
CD01940F

Connection Diagram
14-Lead DIP
(Top View)



CD01930F

Connection Diagram
14-Lead Flatpak
(Top View)



CD02230F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9622DMQB	CA	D-1 14-Lead DIP
μA9622LMQB	2C	C-2 20-Terminal CCP
μA9622FMQB	AA	F-1 14-Lead Flatpak

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
Flatpak	350 mW
DIP and CCP	400 mW
V+ to GND	-0.5 V to +7.0 V
Input Voltage	±15 V
Voltage Applied to Outputs	
for Output High State	-0.5 V to +13.2 V
V- to GND	-0.5 V to -12 V
Enable to GND	-0.5 V to +15 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

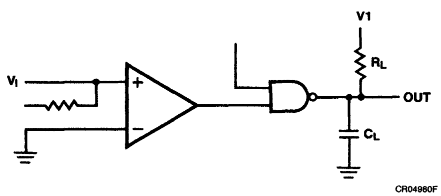
Quality Conformance Inspection: MIL-STD-883, Method 5005

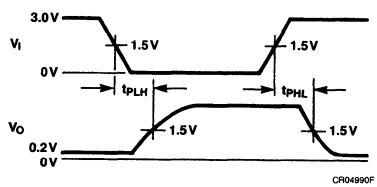
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. When S3 is connected to V-, open inputs cause output to be high. When V+ = 5 V, V- = -10 V and S3 is connected to ground, open inputs cause output to be low.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Flatpak and 120°C/W for the DIP and CCP.

Figure 1 Switching Time Test Circuit and Waveforms



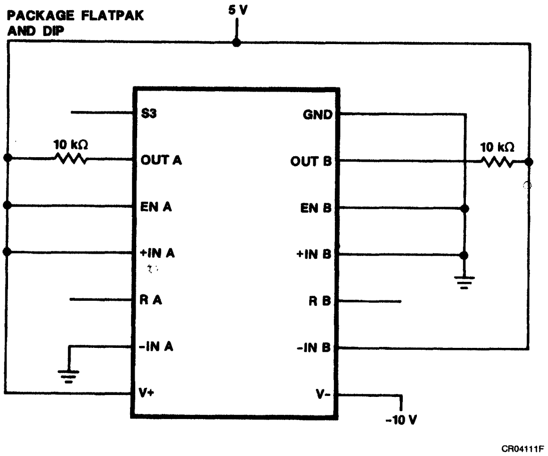


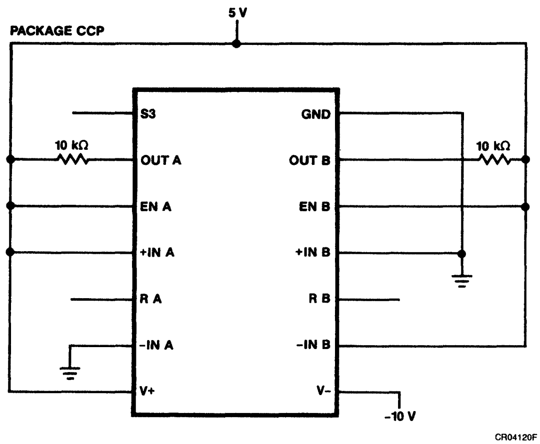
μA9622QB
Electrical Characteristics

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{OL}	Output Voltage LOW	V+ = S3 = 4.5 V, V− = −11 V, V_{DIFF} = 2.0 V, I_{OL} = 12.4 mA, EN = open			0.4	V	1	1,2,3
V_{OH}	Output Voltage HIGH	V+ = 4.5 V, V− = −9.0 V, S3 = 0 V, V_{DIFF} = 1.0 V, I_{OH} = −0.2 mA, EN = open		3.0		V	1	1
				2.9		V	1	2
				2.8		V	1	3
I_{CEX}	Output Leakage Current	V+ = 4.5 V, V− = −11 V, S3 = 0 V, V_{DIFF} = 1.0 V, V_O = 12 V, EN = open			100	μA	1	1
					200	μA	1	2
					50	μA	1	3
I_{OS}	Output Short Circuit Current	V+ = 5.0 V, V− = −10 V, V_{DIFF} = 1.0 V, V_O = S3 = 0 V, EN = open		−3.1	−1.4	mA	1	1
				−3.1	−1.3	mA	1	2,3
I_R(EN)	Enable Input Leakage Current	V+ = S3 = 4.5 V, V− = −11 V, I_N = open, EN = 4.0 V			2.0	μA	1	1
					5.0	μA	1	2
I_F(EN)	Enable Input Forward Current	V+ = 5.5 V, V− = −9.0 V, V_I = open, EN = S3 = 0 V		−1.5		mA	1	1,2,3
I_F(+IN)	+Input Forward Current	V+ = 5.0 V, V− = −10 V, V_I+ = 0 V, V_I− = GND, EN = S3 = open		−2.1		mA	1	1
				−2.0		mA	1	2
				−2.3		mA	1	3
I_F(−IN)	−Input Forward Current	V+ = S3 = 5.0 V, V− = −10 V, V_I+ = GND, V_I− = 0 V, EN = open		−2.4		mA	1	1
				−2.3		mA	1	2
				−2.6		mA	1	3
V_{IL}(EN)	Input Voltage LOW	4.5 V ≤ V+ ≤ 5.5 V, −11 V ≤ V− ≤ −9.0 V, EN = open			1.0	V	1	1
					0.7	V	1	2
					1.3	V	1	3
V_{TH}	Differential Input Threshold Voltage	4.5 V ≤ V+ ≤ 5.5 V, −11 V ≤ V− ≤ −9.0 V, EN = open		1.0	2.0	V	1	1,2,3
V_{CM}	Common Mode Voltage	V+ = 5.0 V, V− = −10 V, 1.0 V ≤ V_{DIFF} ≤ 2.0 V		−10	+10	V	1	1
R_T	Terminating Resistance			91	215	Ω	1	1
I+	Positive Supply Current	V+ = S3 = V_I+ = 5.5 V, V− = 11 V, V_I− = 0 V			22.9	mA	1	1
I−	Negative Supply Current			−11.1		mA	1	1
t_{PLH}	Propagation Delay to High Level	V+ = 5.0 V, V− = −10 V, 0 V ≤ V_I ≤ 3.0 V, C_L = 30 pF (*See Fig. 1*)	R_L = 3.9 kΩ		50	ns	2	9
t_{PHL}	Propagation Delay to Low Level		R_L = 390 Ω		50	ns	2	9

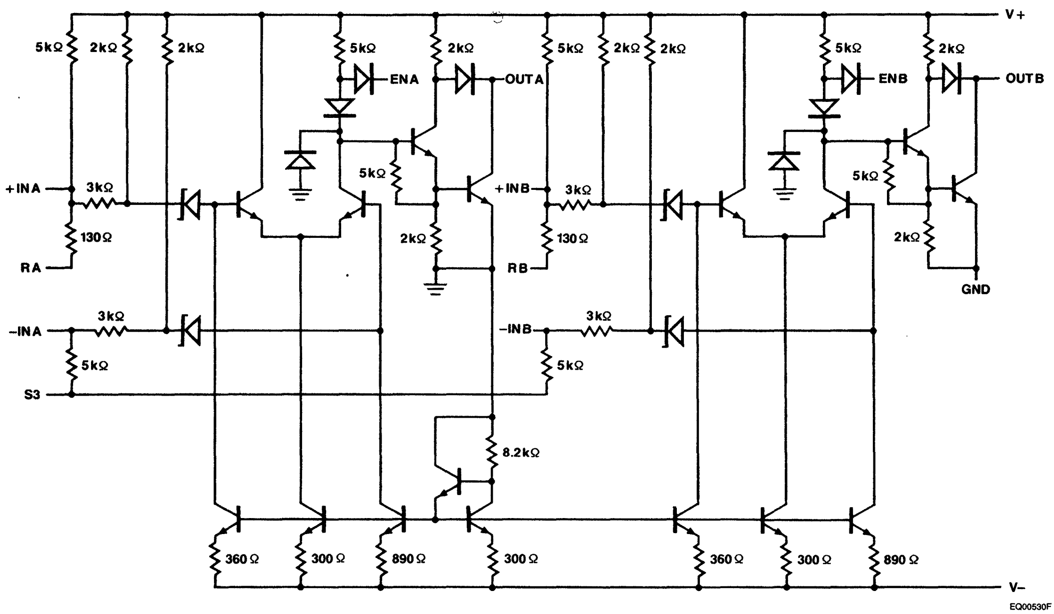
16

Primary Burn-In Circuits





Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA9624QB Dual TTL, MOS Interface Element

Aerospace and Defense Data Sheet
Linear Products

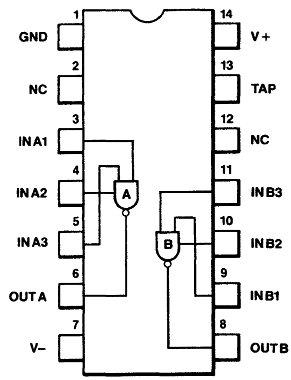
Description

The μA9624QB is a dual two-input TTL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver, or discrete MOS driver. It has an active output for driving medium capacitive loads.

The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the μA9624QB is represented as a NAND gate. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state of "1" or TRUE) the μA9624QB acts as an AND gate.[6]

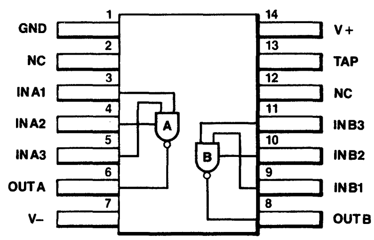
- **TTL Compatible Inputs/Output**
- **MOS Compatible Output/Inputs**
- **Low Power**

Connection Diagram 14-Lead DIP (Top View)



CD01910F

Connection Diagram 14-Lead Flatpak (Top View)



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Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9624FMQB	AA	F-1 14-Lead Flatpak
μA9624DMQB	CA	D-1 14-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Flatpak	350 mW
DIP	400 mW
V+ to GND	V− to +10 V
Voltage Applied to Outputs for High Output State	V− to V+
Input Voltage	−0.5 V to +5.5 V
V− to GND	−30 V to +0.5 V
V− to Tap	−30 V to +0.5 V
V_T	(V+) + (0.5 V)

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

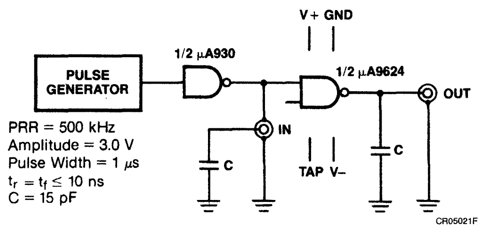
Quality Conformance Inspection: MIL-STD-883, Method 5005

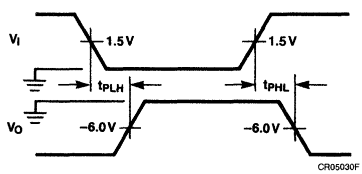
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IH} is guaranteed by the V_{OL} test.
8. V_{IL} is guaranteed by the V_{OH} test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Flatpak and 120°C/W for the DIP.

Figure 1 Switching Time Test Circuit and Waveforms



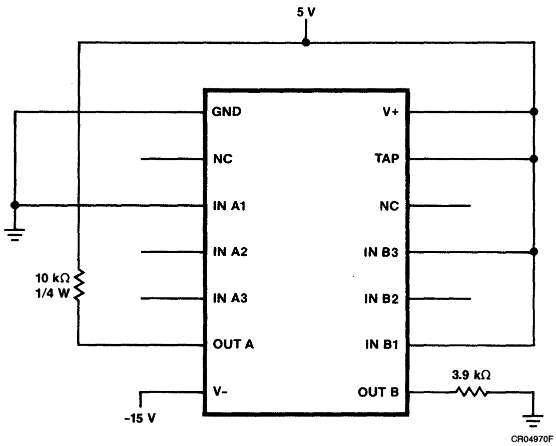


TESTS	CONDITIONS			
t_{PLH}, t_{PHL}	T_A (°C)	V+ (Volts)	V− (Volts)	Tap Voltage
	25	5.0	−13	0

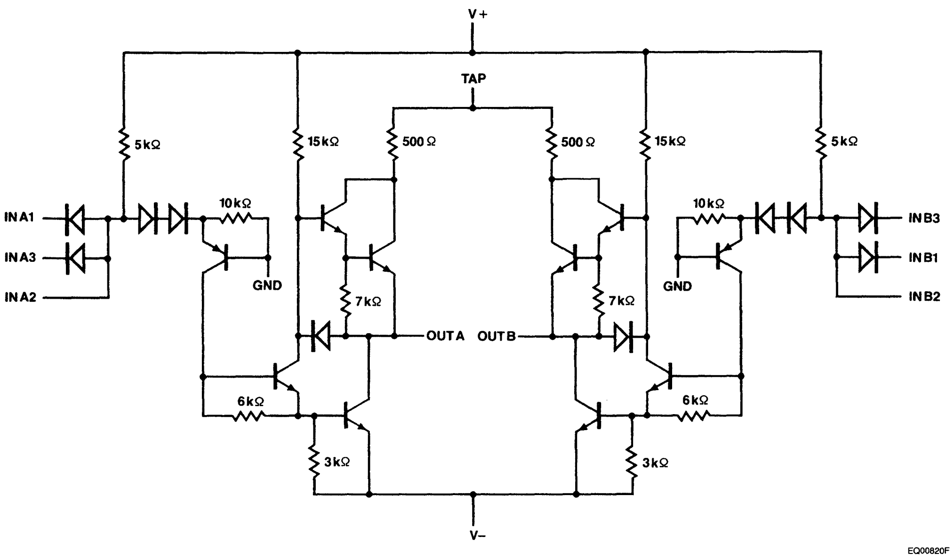
μA9624QB
Electrical Characteristics

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{OH1}	Output Voltage HIGH	V+ = 4.5 V, V− = −28 V, V_T = 0 V, I_{OH} = −10 μA		−1.0		V	1	1,2,3
V_{OH2}	Output Voltage HIGH	V+ = V_T = 5.5 V, V− = −20 V, I_{OH} = −10 μA		3.5		V	1	1,2,3
V_{OL}	Output Voltage LOW	V+ = V_T = 5.0 V, I_{OL} = 10 mA	V− = −15 V		−14 V	V	1	1,2,3
			V− = −28 V		−27 V	V	1	1,2,3
V_{IH}	Input Voltage HIGH[7]			1.9		V	1	1
				1.7		V	1	2
				2.1		V	1	3
V_{IL}	Input Voltage LOW[8]				1.1	V	1	1
					0.8	V	1	2
					1.1	V	1	3
I_F	Input Load Current	V+ = 5.5 V, −28 V ≤ V− ≤ −11 V, V_F = 0.4 V		−1.25		mA	1	1
				−1.13		mA	1	2
				−1.4		mA	1	3
I_R	Input Leakage Current	V+ = 5.5 V, −28 V ≤ V− ≤ −11 V, V_R = 4.0 V			2.0	μA	1	1,3
					5.0	μA	1	2
I_{CEX}	Output Leakage Current	V+ = 5.5 V, V− = −28 V, V_T = 0 V, V_O = 0 V			50	μA	1	1
I_{OS}	Output Short Circuit Current	V+ = 4.5 V, V− = V_O = −11 V, V_T = V_I = 0 V		−32	−14	mA	1	1
				−28	−11	mA	1	2
				−31	−12	mA	1	3
I+	Positive Supply Current	V+ = 5.5 V, V− = −15 V, V_T = 0 V, Inputs Open			6.1	mA	1	1
I_{Max}	Current Max	V+ = 10 V, V− = −30 V, V_T = 0 V, Inputs Open			10	mA	1	1
t_{PLH}	Propagation Delay to High Level	V+ = 5.0 V, V− = −13 V, V_T = 0 V (*See Fig. 1*)			250	ns	2	9
t_{PHL}	Propagation Delay to Low Level				100	ns	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA9625QB Dual TTL, MOS Interface Element

Aerospace and Defense Data Sheet
Linear Products

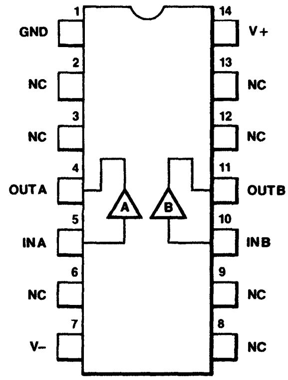
Description

The μA9625QB is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The μA9625QB features a high input impedance which allows preservation of the driving MOS logic level.

The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the μA9625QB is represented as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state of "1" or TRUE), the μA9625QB acts as an inverter.[6]

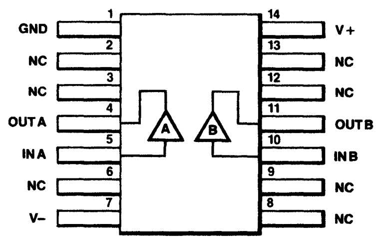
- **TTL Compatible Inputs/Output**
- **MOS Compatible Output/Inputs**
- **Low Power**

Connection Diagram 14-Lead DIP (Top View)



CD01890F

Connection Diagram 14-Lead Flatpak (Top View)



CD01900F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9625FMQB	AA	F-1 14-Lead Flatpak
μA9625DMQB	CA	D-1 14-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Flatpak	350 mW
DIP	400 mW
V+ to GND	V− to +10 V
Voltage Applied to Outputs for High Output State	−0.5 V to V+
Input Voltage	V+ to V−
V− to GND	−30 V to +0.5 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

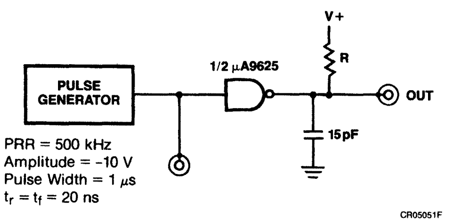
Quality Conformance Inspection: MIL-STD-883, Method 5005

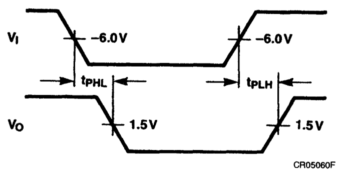
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. V_{IH} is guaranteed by the V_{OH} test.
8. V_{IL} is guaranteed by the V_{OL} test.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Flatpak and 120°C/W for the DIP.

Figure 1 Switching Time Test Circuit and Waveforms



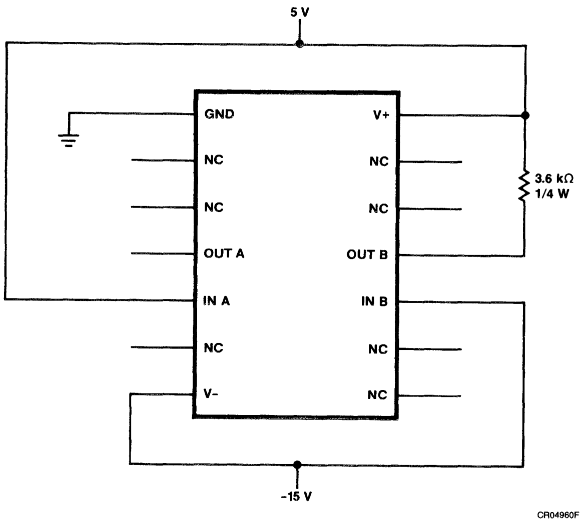


TESTS	CONDITIONS			
t_{PLH}, t_{PHL}	T_A (°C)	V+ (Volts)	V− (Volts)	R (kΩ)
	25	5.0	−13	3.75

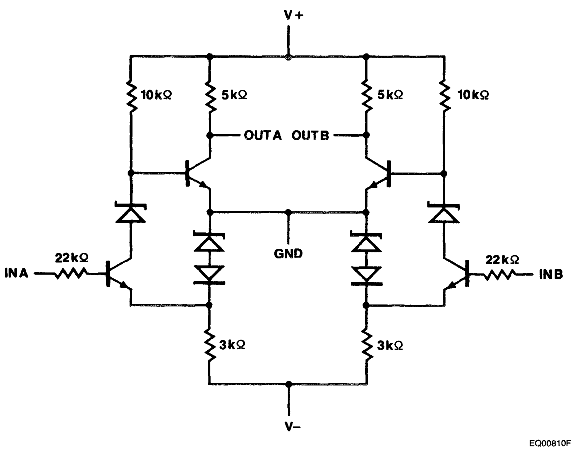
μA9625QB
Electrical Characteristics

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{OH}	Output Voltage HIGH	V+ = 4.5 V, V− = −11 V, I_{OH} = −60 μA	2.6		V	1	1
			2.5		V	1	2,3
V_{OL}	Output Voltage LOW	V+ = 5.5 V, V− = −11 V, I_{OL} = 1.5 mA		0.5	V	1	1,2,3
		V+ = 4.5 V, V− = −11 V, I_{OL} = 1.2 mA		0.5	V	1	1,2,3
V_{IH}	Input Voltage HIGH[7]			−3.0	V	1	1,2,3
V_{IL}	Input Voltage LOW[8]		−9.0		V	1	1,2,3
I_F	Input Load Current	V+ = 5.0 V, V− = −13 V, V_F = −3.0 V		210	μA	1	1,2,3
I_{CEX}	Output Leakage Current	V+ = V_{CEX} = 4.5 V, V− = −13 V		50	μA	1	1
$I+_L$	Positive Supply Current LOW	V+ = 5.5 V, V− = −15 V, V_I = −10 V		4.8	mA	1	1
$I+_H$	Positive Supply Current HIGH	V+ = 5.5 V, V− = −15 V, V_I = 0 V		2.1	mA	1	1
I−	Negative Supply Current	V+ = 5.5 V, V− = −15 V, Input Open or Gnd	−9.0		mA	1	1
$I-_{Max}$	Negative Supply Current Maximum	V+ = 8.0 V, V− = −20 V, V_I = 0 V	−25		mA	1	1
t_{PLH}	Propagation Delay to High Level	V+ = 5.0 V, V− = −13 V, (*See Fig. 1*)		100	ns	2	9
t_{PHL}	Propagation Delay to Low Level			150	ns	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD
A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA9627QB
Dual Line Receiver

Aerospace and Defense Data Sheet
Linear Products

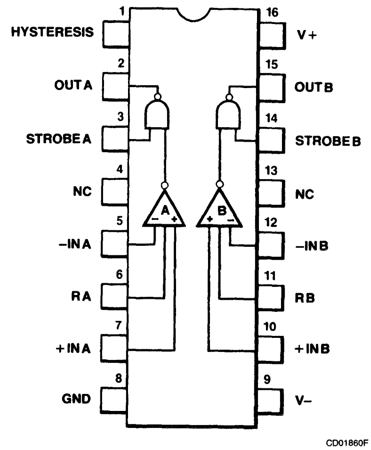
Description

The μA9627QB is a dual line receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accomodates ±25 V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The μA9627QB provides both a selectable hysteresis range and selectable receiver input resistance. When lead 1 is tied to V–, the typical switching points are at 2.6 V and –2.6 V, thus meeting RS-232-C requirements. When lead 1 is open, the typical switching points are at 50 μA and –50 μA, thus satisfying the requirements of MIL-STD-188C LOW level interface. Connecting the R lead to the (–) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving R unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wired-OR function. A TTL/DTL strobe is also provided for each receiver.[6]

- **EIA RS-232-C Input Standards**
- **MIL-STD-188C Input Standards**
- **Variable Hysteresis Control**
- **High Common Mode Rejection**
- **R Control (5 kΩ Or 10 kΩ)**
- **Wired-OR Capability**
- **Choice Of Inverting And Non-Inverting Inputs**
- **Outputs And Strobe TTL Compatible**

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9627DMQB	EA	D-2 16-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[7]	
DIP	400 mW
V+ to GND	0 V to +15 V
V− to GND	0 V to −15 V
Input Voltage Referred to GND	±25 V
Strobe to GND	−0.5 V to +5.5 V
Applied Output Voltage	−0.5 V to +15 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

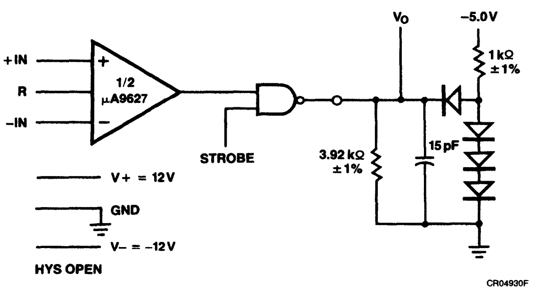
Quality Conformance Inspection: MIL-STD-883, Method 5005

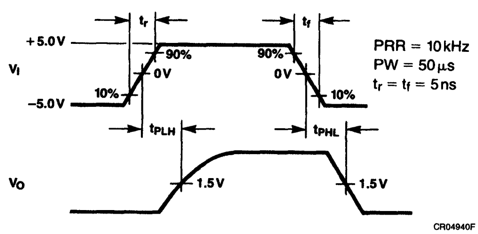
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Figure 1 Switching Time Test Circuit and Waveforms





15 pF includes jig capacitance.
All diodes are FD777 or equivalent.

μA9627QB

Electrical Characteristics Hysteresis, −IN A, −IN B, RA, and RB Open for MIL-STD-188C, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{OL}	Output Voltage LOW	$V+ = 10.8$ V, $V- = -13.2$ V, $V_I+ = 0.6$ V, $I_{OL} = 6.4$ mA			0.4	V	1	1,2,3
V_{OH}	Output Voltage HIGH	$V+ = 10.8$ V, $V- = -13.2$ V, $V_I+ = 0.6$ V, $I_{OH} = -0.5$ mA		2.4		V	1	1,2,3
I_{OS}	Output Short Circuit Current	$V+ = 13.2$ V, $V- = -10.8$ V, $V_I+ = 0.6$ V, Outputs Grounded		−3.0		mA	1	1,2,3
I_{IH}(ST)	Input Current HIGH (Strobe)	$V+ = 10.8$ V, $V- = -13.2$ V, $V_I+ = 0.6$ V	$V_{ST} = 2.4$ V		40	μA	1	1,2,3
			$V_{ST} = 5.5$ V		1.0	mA	1	1,2,3
R_I	Input Resistance	$V+ = 13.2$ V, $V- = -13.2$ V, $-3.0\ V \leqslant V_I+ \leqslant 3.0$ V		6.0		kΩ	1	1,2,3
I_{TH+}	Positive Threshold Current	$\pm 10.8\ V \leq V_{CC} \leq \pm 13.2$ V, $V_O = 2.4$ V			100	μA	1	1,2,3
I_{TH-}	Negative Threshold Current	$\pm 10.8\ V \leqslant V_{CC} \leqslant \pm 13.2$ V, $V_O = 0.4$ V		−100		μA	1	1,2,3
V_{IL}(ST)	Input Voltage LOW (Strobe)	$V_I+ = -0.6$ V			0.8	V	1	1,2,3
V_{IH}(ST)	Input Voltage HIGH (Strobe)	$V+ = 13.2$ V, $V- = -10.8$ V, $V_I+ = -0.6$ V		2.0		V	1	1,2,3
I+	Positive Supply Current	$\pm 10.8\ V \leqslant V_{CC} \leqslant \pm 13.2$ V $V_I+ = -0.6$ V			18	mA	1	1,3
					12.4	mA	1	2
I−	Negative Supply Current	$\pm 10.8\ V \leqslant V_{CC} \leqslant \pm 13.2$ V $V_I+ = 0.6$ V		−16		mA	1	1,3
				−11.4		mA	1	2

Electrical Characteristics +IN A and −IN B connected to ground, RA and RB connected to −IN A and −IN B, and Hysteresis connected to V− for RS-232C, unless otherwise specified.

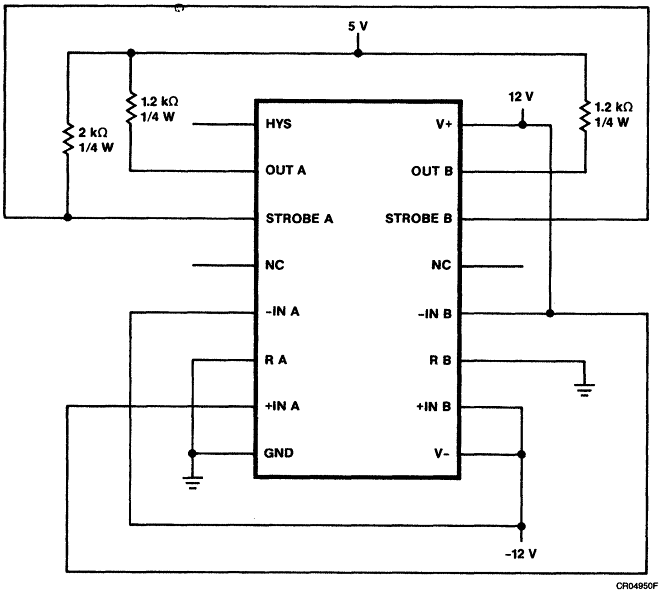
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
R_I	Input Resistance	$3.0\ V \leqslant V_I \leqslant 25$ V	3.0	7.0	kΩ	1	1,2,3
		$-3.0\ V \leqslant V_I \leqslant -25$ V	3.0	7.0	kΩ	1	1,2,3
V_I	Input Voltage		−2.0	2.0	V	1	1,2,3
V_{TH+}	Positive Threshold Voltage			3.0	V	1	1,2,3
V_{TH-}	Negative Threshold Voltage		−3.0		V	1	1,2,3

Electrical Characteristics $V_{CC} = \pm 12$ V for MIL-STD-188C and RS-232C

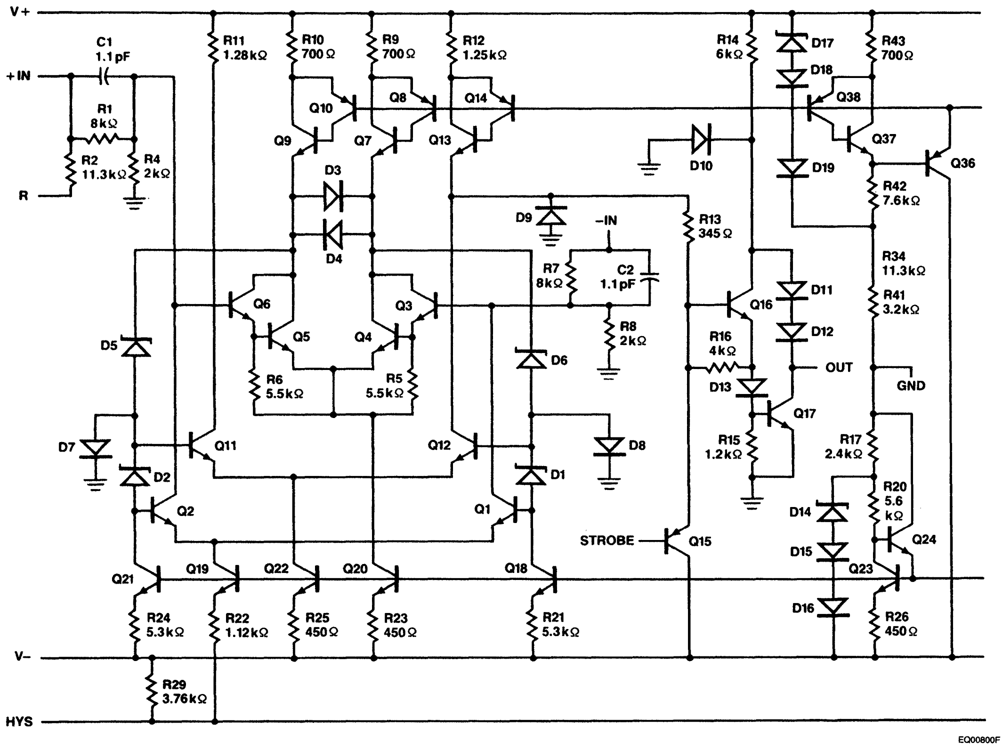
Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
t_{PLH}	Propagation Delay to High Level	(*See Fig. 1*)		250	ns	2	9
t_{PHL}	Propagation Delay to Low Level	(*See Fig. 1*)		250	ns	2	9

16

Primary Burn-In Circuit



Equivalent Circuit (1/2 of circuit)



FAIRCHILD

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MIL-STD-883
July 1986—Rev 1[5]

μA9636AQB Dual Programmable Slew Rate Line Driver

Aerospace and Defense Data Sheet
Linear Products

Description

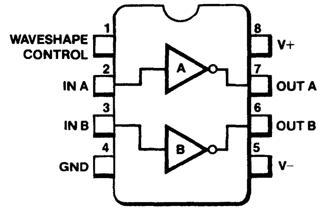
The μA9636AQB is a TTL/CMOS compatible, dual, single ended, line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The μA9636AQB is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current limiting is provided in both output states. The μA9636AQB is designed for nominal power supplies of ±12 V.

Inputs are TTL compatible with input current loading low enough (1/10 UL) to be compatible with CMOS logic also. Clamp diodes are provided on the inputs to limit transients below ground.[6]

- **Programmable Slew Rate Limiting**
- **Meets EIA RS-423 Requirements**
- **Output Short Circuit Protection**
- **TTL And CMOS Compatible Inputs**

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9636ARMQB	PA	D-4 8-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[10]	
DIP	400 mW
V+ to GND	V− to +15 V
V− to GND	0.5 V to −15 V
V+ to V−	0 to +30 V
Output to GND	±15 V
Output Source Current	−150 mA
Output Sink Current	150 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

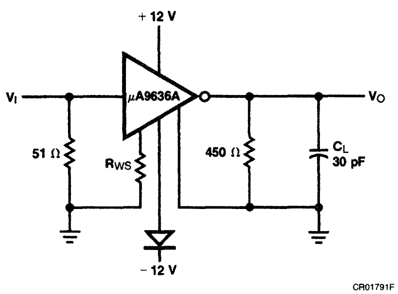
Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

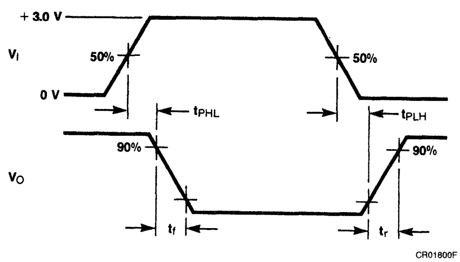
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Only one output shorted at a time.
8. V_{IH} is guaranteed by the V_{OH} test.
9. V_{IL} is guaranteed by the V_{OL} test.
10. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Figure 1 Switching Time Test Circuit and Waveforms



C_L includes jig and probe capacitance

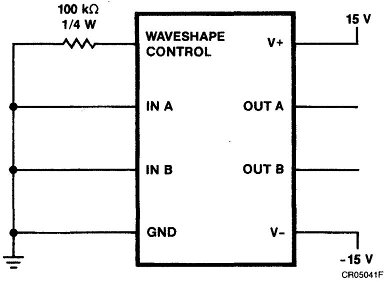


V_I
Amplitude = 3.0 V
Offset = 0 V
Pulse Width = 500 μs
PRR = 1 kHz
$t_r = t_f = 10$ ns

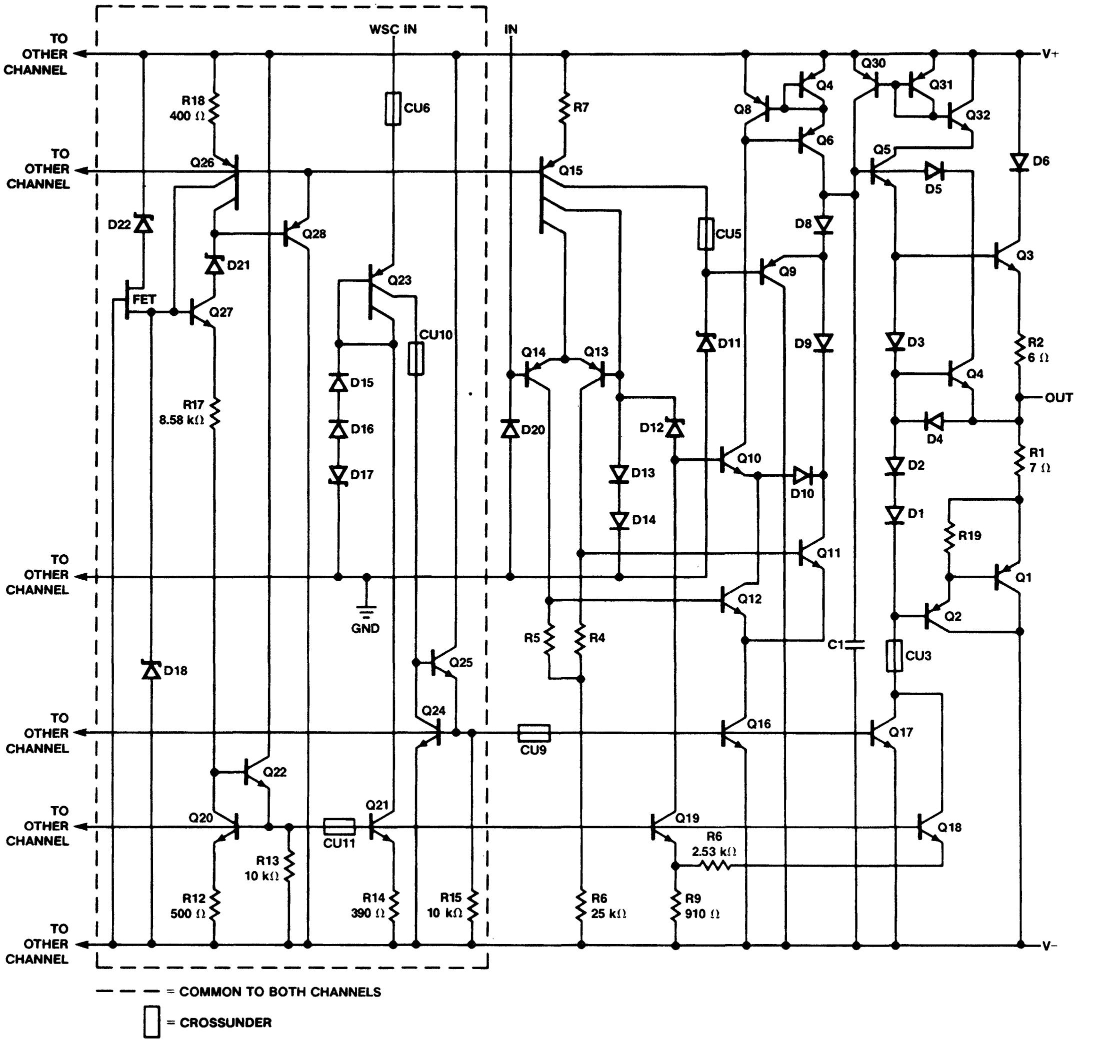
μA9636AQB
Electrical Characteristics 10.8 V ⩽ V+ ⩽ 13.2 V, −13.2 V ⩽ V− ⩽ −10.8 V, and 10 kΩ ⩽ R_{WS} ⩽ 500 kΩ, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
V_{OH1}	Output Voltage HIGH	R_L to GND ($R_L = \infty$)	5.0	6.0	V	1	1,2,3
V_{OH2}	Output Voltage HIGH	R_L to GND (R_L = 3.0 kΩ)	5.0	6.0	V	1	1,2,3
V_{OH3}	Output Voltage HIGH	R_L to GND (R_L = 450 Ω)	4.0	6.0	V	1	1,2,3
V_{OL1}	Output Voltage LOW	R_L to GND ($R_L = \infty$)	−6.0	−5.0	V	1	1,2,3
V_{OL2}	Output Voltage LOW	R_L to GND (R_L = 3.0 kΩ)	−6.0	−5.0	V	1	1,2,3
V_{OL3}	Output Voltage LOW	R_L to GND (R_L = 450 Ω)	−6.0	−4.0	V	1	1,2,3
R_O	Output Resistance	R_L = 450 Ω		50	Ω	1	1,2,3
I_{OS+}	Positive Output Short Circuit Current[7]	V_O = 0 V, V_I = 0 V, R_{ws} = 10 kΩ	−150	−15	mA	1	1,2,3
I_{OS-}	Negative Output Short Circuit Current[7]	V_O = 0 V, V_I = 2.0 V, R_{ws} = 10 kΩ	15	150	mA	1	1,2,3
I_{CEX}	Output Leakage Current	V_{CC} = 0 V, V_O = ± 6.0 V, R_{ws} = 10 kΩ	−100	100	μA	1	1,2,3
V_{IH}	Input Voltage HIGH[8]		2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW[9]			0.8	V	1	1,2,3
V_{IC}	Input Clamp Diode Voltage	I_I = 15 mA	−1.5		V	1	1,2,3
I_{IL}	Input Current LOW	V_I = 0.4 V	−80		μA	1	1,2,3
I_{IH}	Input Current HIGH	V_I = 2.4 V		10	μA	1	1,2,3
		V_I = 5.5 V		100	μA	1	1,2,3
I+	Positive Supply Current	V+ = 12 V, V− = −12 V, $R_L = \infty$, R_{ws} = 100 kΩ, V_I = 0 V		18	mA	1	1,2,3
I−	Negative Supply Current	V+ = 12 V, V− = −12 V, $R_L = \infty$, R_{ws} = 100 kΩ, V_I = 0 V	−18		mA	1	1,2,3
t_r	Rise Time	R_{ws} = 10 kΩ	0.8	1.4	μs	1	9
	(*See Fig. 1*)	R_{ws} = 100 kΩ	8.0	14	μs	1	9
		R_{ws} = 500 kΩ	40	70	μs	1	9
		R_{ws} = 1000 kΩ	80	140	μs	1	9
t_f	Fall Time	R_{ws} = 10 kΩ	0.8	1.4	μs	1	9
	(*See Fig. 1*)	R_{ws} = 100 kΩ	8.0	14	μs	1	9
		R_{ws} = 500 kΩ	40	70	μs	1	9
		R_{ws} = 1 MΩ	80	140	μs	1	9

Primary Burn-In Circuit



Equivalent Circuit



MIL-STD-883
July 1986—Rev 1[5]

μA9637AQB Dual Differential Line Receiver

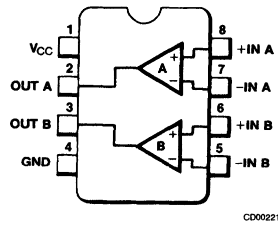
Aerospace and Defense Data Sheet
Linear Products

Description

The μA9637AQB is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the μA9637AQB satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The μA9637AQB is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5 V power supply and has Schottky TTL compatible outputs. The μA9637AQB has an operational input common mode range ±7 V either differentially or to ground.[6]

- **Dual Channels**
- **Single 5 V Supply**
- **Satisfies EIA Standards RS-422 and RS-423**
- **Built In ±35 mV Hysteresis**
- **High Common Mode Range**
- **High Input Impedance**
- **TTL Compatible Output**
- **Schottky Technology**

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9637ARMQB	PA	D-4 8-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Supply Voltage	-0.5 V to +7.0 V
Input Voltage	±15 V
Differential Input Voltage	±15 V
Output Voltage	-0.5 V to +5.5 V
Output Sink Current	50 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

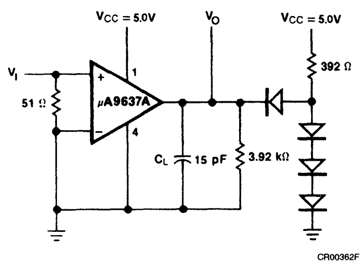
Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
9. AC tests at 25°C

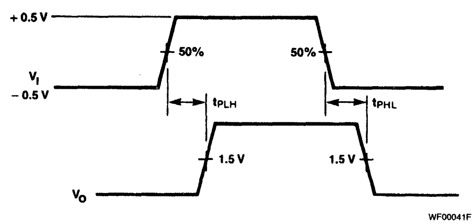
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Only one output should be shorted at a time.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Figure 1 Switching Time Test Circuit and Waveforms



C_L includes jig and probe capacitance.
All diodes are FD700 or equivalent

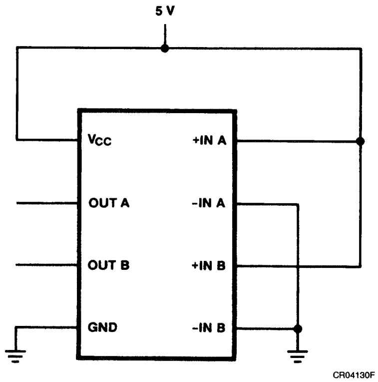


V_I
Amplitude = 1.0 V
Offset = 0.5 V
Pulse Width = 100 ns
PRR = 5.0 MHz
$t_r = t_f = 5.0$ ns

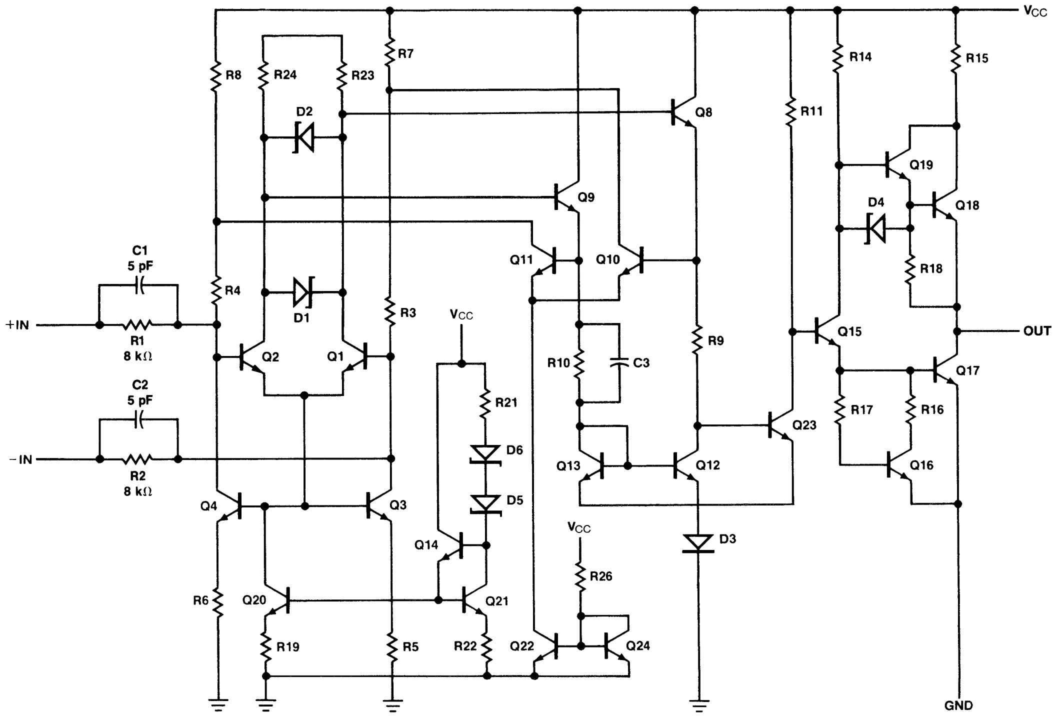
μA9637AQB
Electrical Characteristics 4.5 V $\leqslant V_{CC} \leqslant$ 5.5 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{TH}	Differential Input Threshold Voltage	$V_{CM} = \pm 7.0$ V		−0.2	0.2	V	1	1,2,3
$V_{TH(R)}$	Differential Input Threshold Voltage Resistor	$V_{CM} = \pm 7.0$ V		−0.4	0.4	V	1	1,2,3
I_I	Input Current	0 V $\leqslant V_{CC} \leqslant$ 5.5 V	V_I+ = 10 V		3.25	mA	1	1,2,3
			V_I+ = −10 V	−3.25		mA	1	1,2,3
V_{OL}	Output Voltage LOW	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.5	V	1	1,2,3
V_{OH}	Output Voltage HIGH	V_{CC} = 4.5 V, I_{OH} = −1.0 mA		2.5		V	1	1,2,3
I_{OS}	Output Short Circuit Current[7]	V_{CC} = 5.5 V, V_O = 0 V		−100	−40	mA	1	1,2,3
I_{CC}	Supply Current	V_{CC} = 5.5 V, V_I+ = 0.5 V, V_I- = GND			50	mA	1	1,2,3
t_{PLH}	Propagation Delay to High Level	V_{CC} = 5.0 V (*See Fig. 1*)			25	ns	2	9
t_{PHL}	Propagation Delay to Low Level				25	ns	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA9638QB Dual High Speed Differential Line Driver

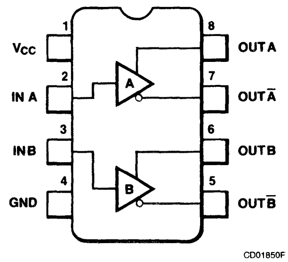
Aerospace and Defense Data Sheet
Linear Products

Description

The μA9638QB is a Schottky, TTL compatible dual differential line driver. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem-pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50 Ω transmission lines at high speed. The 8-Lead DIP provides high package density.[6]

- **Single 5 V Supply**
- **Schottky Technology**
- **TTL And CMOS Compatible Inputs**
- **Output Short Circuit Protection**
- **Input Clamp Diodes**
- **Complementary Outputs**
- **Fast Propagation Delay**
- **"Glitchless" Differential Output**
- **Delay Time Stable With V_{CC} And Temperature Variations**

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9638RMQB	PA	D-4 8-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[7]	
DIP	400 mW
Supply Voltage	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +7.0 V

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
8. Guaranteed by V_{OL} and V_{OH} tests.
9. Guaranteed by maximum V_{CC}.
10. Guaranteed by $V_T - \bar{V}_T$ output balance.

Figure 1 Terminated Output Voltage and Output Balance

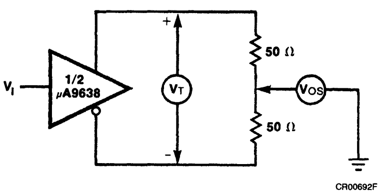
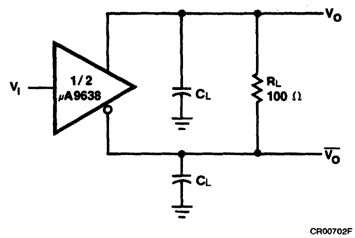
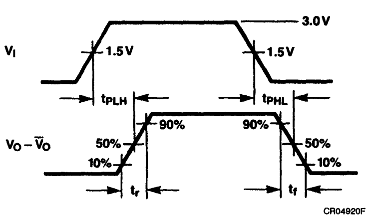


Figure 2 Switching Time Test Circuit and Waveforms





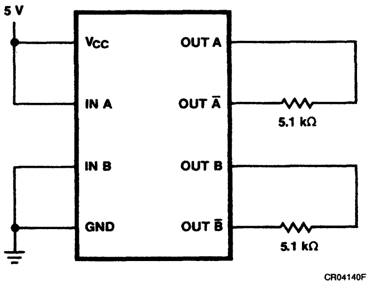
The pulse generator has the following characteristcs:
$Z_O = 50\ \Omega$, PRR = 500 kHz
$t_W = 100$ ns, $t_r \leq 5.0$ ns
C_L includes probe and jig capacitance.

μA9638QB
Electrical Characteristics 4.5 V ≤ V_{CC} ≤ 5.5 V, unless otherwise specified.

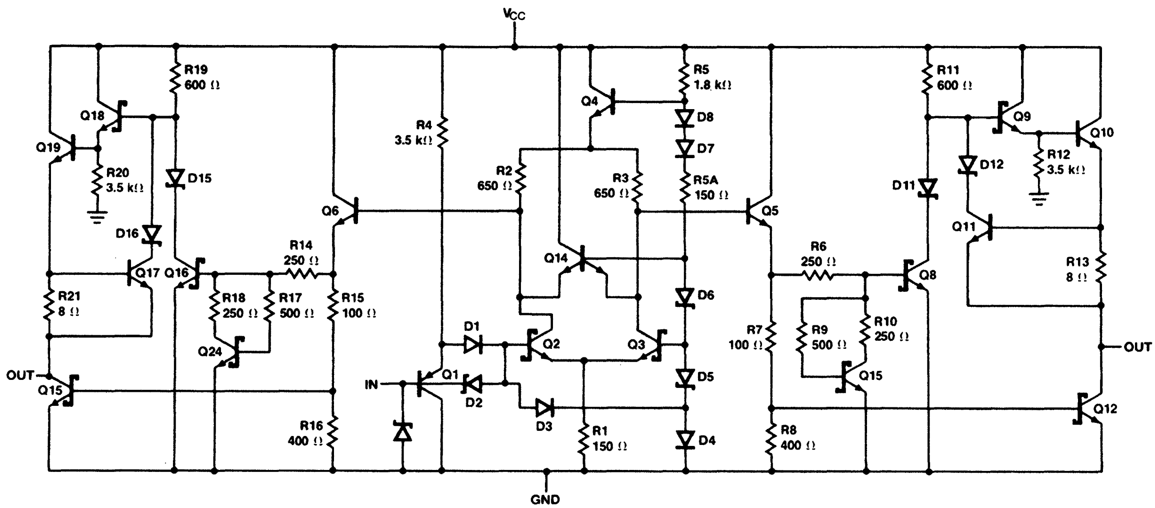
Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{IH}	Input Voltage HIGH[8]			2.0		V	1	1,2,3
V_{IL}	Input Voltage LOW[8]				0.5	V	1	1,2,3
V_{IC}	Clamped Input Voltage	$I_I = -18$ mA		-1.2		V	1	1,2,3
V_{OH}	Output Voltage HIGH	$V_{CC} = 4.5$ V, $V_{IH} = 2.0$ V, $V_{IL} = 0.5$ V	$I_{OH} = -10$ mA	2.5		V	1	1,2,3
			$I_{OH} = -40$ mA	2.0		V	1	1,2,3
V_{OL}	Output Voltage LOW	$V_{IH} = 2.0$ V, $V_{IL} = 0.5$ V, $I_{OL} = 30$ mA			0.5	V	1	1,2,3
$I_{I\ Max}$	Input Current at Maximum Input Voltage	$V_{CC} = 5.5$ V, $V_I = 5.5$ V			50	μA	1	1,2,3
I_{IH}	Input Current HIGH	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V			25	μA	1	1,2,3
I_{IL}	Input Current LOW	$V_{CC} = 5.5$ V, $V_{IL} = 0.5$ V		-200		μA	1	1,2,3
I_{OS}	Short Circuit Output Current	$V_{CC} = 5.5$ V, $V_O = 0$ V		-150	-50	mA	1	1,2,3
V_T, $\bar{V}_T$	Terminated Output Voltage	*(See Fig. 1)*		2.0		V	1	1,2,3
$V_T - \bar{V}_T$	Output Balance				0.4	V	1	1,2,3
V_{OS}, $\bar{V}_{OS}$	Output Offset Voltage[9]				3.0	V	1	1,2,3
$V_{OS} - \bar{V}_{OS}$	Output Offset Balance[10]				0.4	V	1	1
I_{CEX}	Output Leakage Current	$V_{CC} = 0$ V, -0.25 V ≤ V_{CEX} ≤ 5.5 V		-150	150	μA	1	1,2,3
I_{CC}	Supply Current (Total)	$V_{CC} = 5.5$ V, no load; All inputs at 0 V			75	mA	1	1,2,3
t_{PLH}	Propagation Delay to High Level	$C_L = 15$ pF, $R_L = 100\ \Omega$, $V_{CC} = 5.0$ V *(See Fig. 2)*			20	ns	1	9
t_{PHL}	Propagation Delay to Low Level				20	ns	1	9
t_f	Fall Time, 90% – 10%				20	ns	1	9
t_r	Rise Time, 10% – 90%				20	ns	1	9

16

Primary Burn-In Circuit



Equivalent Circuit (1/2 of circuit)



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MIL-STD-883
July 1986—Rev 1[5]

μA9639AQB Dual Differential Line Receiver

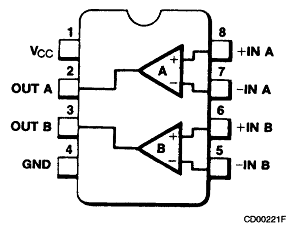
Aerospace and Defense Data Sheet
Linear Products

Description

The μA9639AQB is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422, RS-423, and RS-232C. In addition, the μA9639AQB satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The μA9639AQB is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5 V power supply and has Schottky TTL compatible outputs. The μA9639AQB has an operational input common mode range of ±7 V either differentially or to ground.[6]

- **Dual Channels**
- **Single 5 V Supply**
- **Satisfies EIA Standards RS-422, RS-423, and RS-232C**
- **Built-In ±35 mV Hysteresis**
- **High Common Mode Range**
- **High Input Impedance**
- **TTL Compatible Output**
- **Schottky Technology**

Connection Diagram
8-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9639ARMQB	PA	D-4 8-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Supply Voltage	−0.5 V to +7.0 V
Input Voltage	±15 V
Differential Input Voltage	±15 V
Output Voltage	−0.5 V to +5.5 V
Output Sink Current	50 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

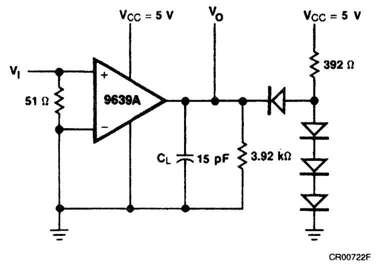
Quality Conformance Inspection: MIL-STD-883, Method 5005

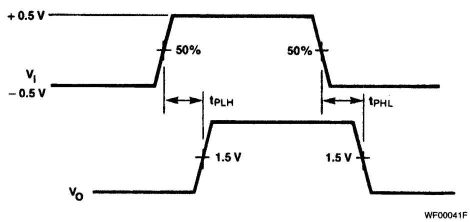
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Only one output should be shorted at a time.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Figure 1 Switching Time Test Circuit and Waveforms





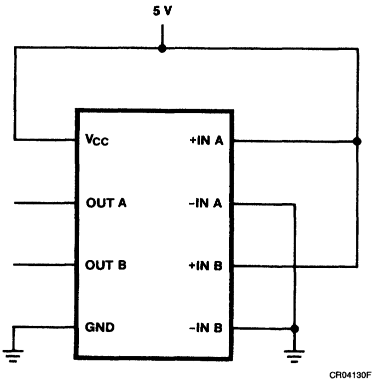
C_L includes jig and probe capacitance.
All diodes are FD700 or equivalent.

V_I
Amplitude = 1.0 V
Offset = 0.5 V
Pulse Width = 100 ns
PRR = 5.0 MHz
$t_r = t_f = \leqslant 5.0$ ns

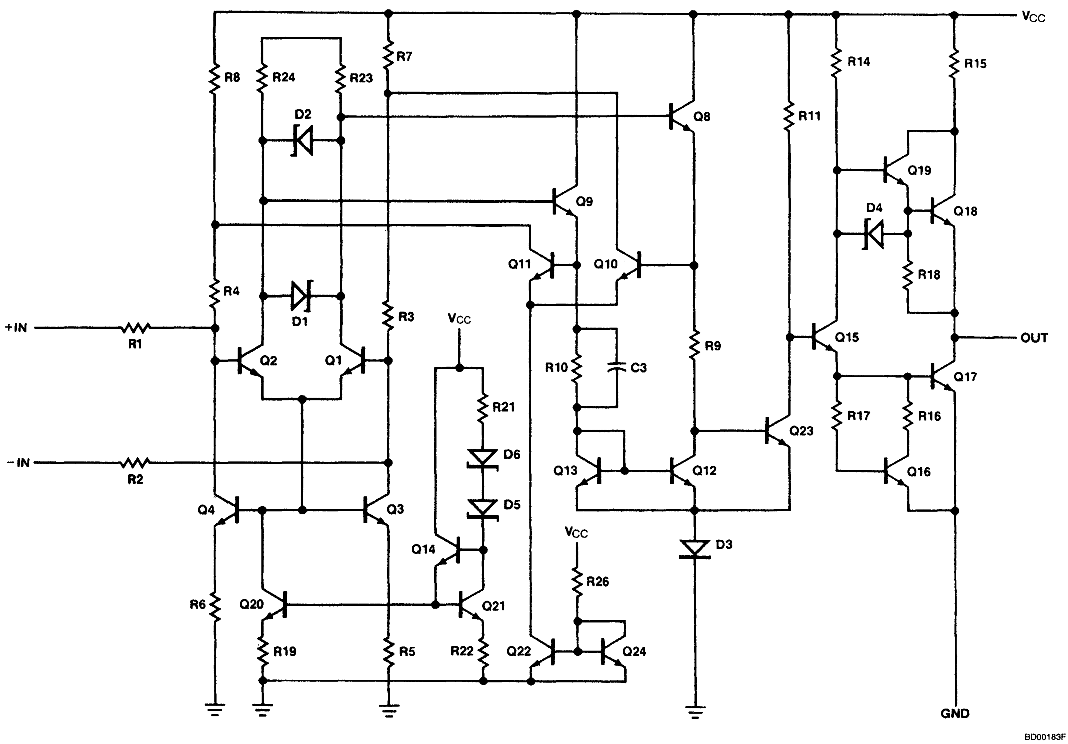
μA9639AQB
Electrical Characteristics 4.5 V $\leqslant V_{CC} \leqslant$ 5.5 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 7.0 V		−0.2	0.2	V	1	1,2,3
$V_{TH}(R)$	Differential Input Threshold Voltage Resistor	V_{CM} = 7.0 V		−0.4	0.4	V	1	1,2,3
I_I	Input Current	0 V $\leqslant V_{CC} \leqslant$ 5.5 V	V_I+ = 10 V		3.25	mA	1	1,2,3
			V_I+ = −10 V	−3.25		mA	1	1,2,3
V_{OL}	Output Voltage LOW	V_{CC} = 4.5 V, I_{OL} = 20 mA			0.5	V	1	1,2,3
V_{OH}	Output Voltage HIGH	V_{CC} = 4.5 V, I_{OH} = −1.0 mA		2.5		V	1	1,2,3
I_{OS}	Output Short Circuit Current[7]	V_{CC} = 5.5 V, V_O = 0 V		−100	−40	mA	1	1,2,3
I_{CC}	Supply Current	V_{CC} = 5.5 V, V_I+ = 0.5 V, V_I− = GND			50	mA	1	1,2,3
t_{PLH}	Propagation Delay to High Level	V_{CC} = 5.0 V (*See Fig. 1*)			85	ns	2	9
t_{PHL}	Propagation Delay to Low Level				85	ns	2	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 1[5]

μA9667QB High Current/Voltage Darlington Driver

Aerospace and Defense Data Sheet

Linear Products

Description

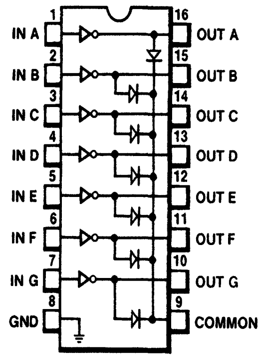
The μA9667QB is comprised of seven high voltage, high current NPN Darlington transistor pairs. It features common emitter, open collector outputs. To maximize its effectiveness, this unit contains suppression diodes for inductive loads and an appropriate emitter base resistor for leakage.

The μA9667QB offers solutions to a great many interface needs including solenoids, relays, lamps, small motors and LEDs.

Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.[6]

- **Seven High Gain Darlington Pairs**
- **High Output Voltage**
- **High Output Current**
- **DTL, TTL, PMOS, CMOS Compatible**
- **Suppression Diodes For Inductive Loads**

Connection Diagram 16-Lead DIP (Top View)



CD00940F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA9667DMQB	EA	D-2 16-Lead DIP

16

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
DIP	400 mW
Output Voltage	55 V
Input Voltage	30 V
Emitter-Base Voltage	6.0 V
Continuous Collector Current	500 mA
Continuous Base Current	25 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

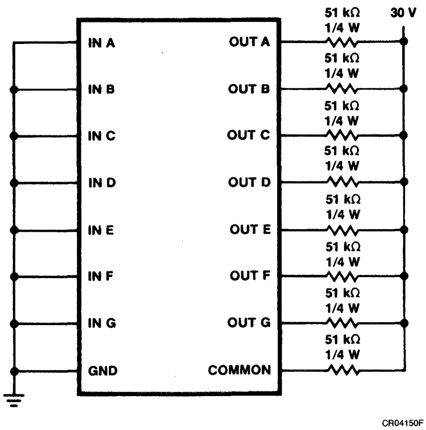
Group C and D Endpoints: Group A, Subgroup 1

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. $I_{I(OFF)}$ current limit is guaranteed against partial turn-on of the output.
8. $V_{I(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

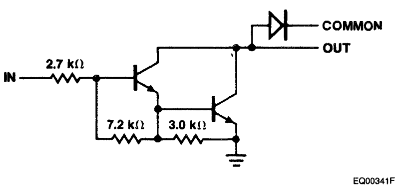
μA9667QB
Electrical Characteristics ± 10.8 V $\leqslant V_{CC} \leqslant \pm 13.2$ V, $R_L = 3.0$ kΩ, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
I_{CEX}	Output Leakage Current	$V_{CE} = 50$ V			100	μA	1	1,2,3
$V_{CE}(SAT)$	Collector-Emitter Saturation Voltage	$I_C = 350$ mA	$I_B = 500$ μA		1.6	V	1	1,2
			$I_B = 600$ μA		1.6	V		3
		$I_C = 200$ mA	$I_B = 350$ μA		1.3	V	1	1,2
			$I_B = 400$ μA		1.3	V		3
		$I_C = 100$ mA	$I_B = 250$ μA		1.1	V	1	1,2
			$I_B = 300$ μA		1.1	V		3
$I_I(ON)$	Input Current	$V_I = 3.85$ V			1.35	mA	1	1,2,3
$I_I(OFF)$	Input Current[7]	$I_C = 500$ μA		50		μA	1	1,3
				35		μA	1	2
$V_I(ON)$	Input Voltage[8]	$V_{CE} = 2.0$ V, $I_C = 200$ mA			2.4	V	1	1,2
					2.6	V	1	3
		$V_{CE} = 2.0$ V, $I_C = 250$ mA			2.7	V	1	1,2
					2.9	V	1	3
		$V_{CE} = 2.0$ V, $I_C = 300$ mA			3.0	V	1	1,2
					3.2	V	1	3
I_R	Clamp Diode Leakage Current	$V_R = 50$ V			50	μA	1	1,2,3
V_F	Clamp Diode Forward Voltage	$I_F = 350$ mA			2.0	V	1	1,2,3
h_{FE}	DC Forward Current Transfer Ratio	$V_{CE} = 2.0$ V, $I_C = 350$ mA		1000			1	1,2,3
t_{PLH}	Propagation Delay to High Level	0.5 V_I to 0.5 V_O			5.0	μs	4	9
t_{PHL}	Propagation Delay to Low Level				5.0	μs	4	9

Primary Burn-In Circuit



Equivalent Circuit



FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 0[1]

Advance Information

μA26LS31QB Quad High Speed Differential Line Driver

Aerospace and Defense Data Sheet

Linear Products

Description

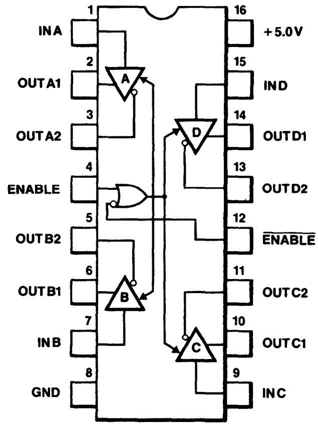
The μA26LS31QB is a quad differential line driver designed for digital data transmission over balanced lines. The μA26LS31QB meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or paralled-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The μA26LS31QB features three-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load. The μA26LS31QB offers optimum performance when used with the μA26LS32QB Quad Differential Line Receiver.[2]

- **Low Output Skew**
- **Low Input To Output Delay**
- **Operation From Single 5.0 V Supply**
- **Output Will Not Load Line When $V_{CC} = 0$**
- **Four Line Drivers In One Package For Maximum Package Density**
- **Output Short Circuit Protection**
- **Complementary Outputs**
- **Meets The Requirements Of EIA Standard RS-422**
- **High Output Drive Capability For 100 Ω Terminated Transmission Lines**

Notes

1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

Connection Diagram 16-Lead DIP (Top View)

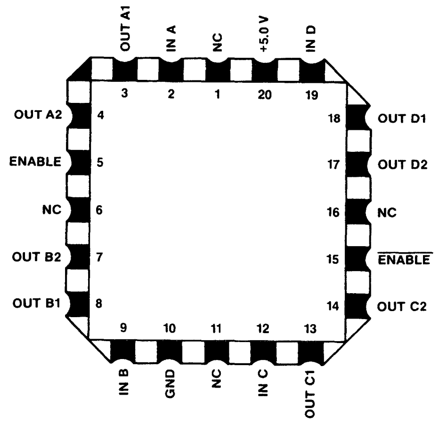


CD02170F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA26LS31DMQB	EA	D-2 16-Lead DIP

Connection Diagram 20 Terminal CCP (Top View)



CD02250F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA26LS31LMQB	2C	C-2 20-Terminal CCP

16

FAIRCHILD

A Schlumberger Company

MIL-STD-883

July 1986—Rev 0[1]

Advance Information

μA26LS32QB Quad Differential Line Receiver

Aerospace and Defense Data Sheet

Linear Products

Description

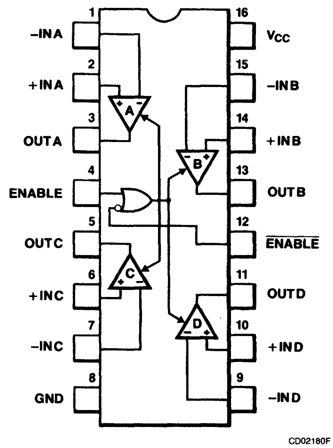
The μA26LS32QB is a quad line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission. The device features an input sensitivity of 200 mV over the input range of ±7.0 V. The μA26LS32QB provides an enable and disable function common to all four receivers and three-state outputs with 8.0 mA sink capability and incorporates a fail safe input/output relationship which keeps the outputs high when the inputs are open. The μA26LS32QB offers optimum performance when used with the μA26LS31QB Quad Differential Line Driver.[2]

- **Input Voltage Range Of ±7.0 V (Differential Or Common Mode) ±0.2 V Sensitivity Over The Input Voltage Range**
- **Meets All The Requirements Of EIA Standards RS-422 And RS-423**
- **High Input Impedance**
- **30 mV Input Hysteresis**
- **Operation From Single 5.0 V Supply**
- **Fail Safe Input/Output Relationship With Output Always High When Inputs Are Open.**
- **Three-State Drive, With Choice Of Complementary Output Enables, For Receiving Directly Onto A Data Bus.**
- **Low Propagation Delay**
- **Advanced Low Power Schottky Processing**

Notes

1. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
2. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.

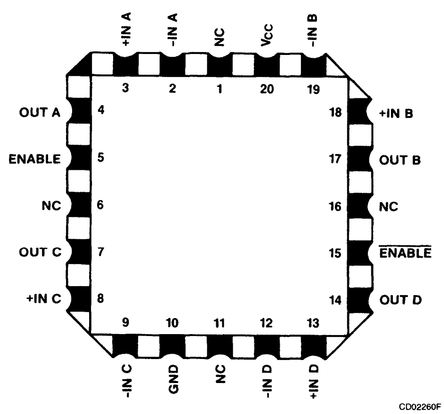
Connection Diagram 16-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA26LS32DMQB	EA	D-2 16-Lead DIP

Connection Diagram 20-Terminal CCP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA26LS32LMQB	2C	C-2 20-Terminal CCP

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A Schlumberger Company

μA571SQB Analog to Digital Converter

MIL-STD-883
July 1986—Rev 1[5]

Aerospace and Defense Data Sheet
Linear Products

Description

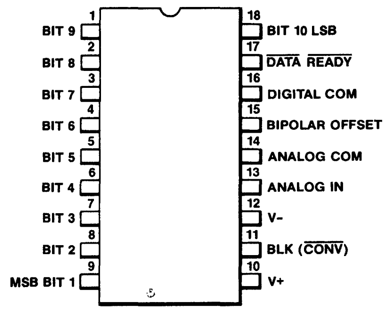
The μA571SQB is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers — all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25 μs.

The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.

Operating on supplies of 5 V to ±15 V, the μA571SQB will accept analog inputs of 0 V to 10 V unipolar, or ±5 V bipolar, externally selectable. The device will also operate with a −12 V supply. As the BLANK and CONVERT input is driven LOW, the 3-state outputs will be open and a conversion starts. Upon completion of the conversion, the DATA READY line will go LOW and the data will appear at the output. Pulling the BLANK and CONVERT input HIGH blanks the outputs and readies the device for the next conversion. The μA571SQB executes a true 10-bit conversion with no missing codes in approximately 25 μs.

- **Complete A/D Converter With Reference And Clock**
- **Fast Successive Approximation Conversion**
- **No Missing Codes Over Full Temperature Range**
- **Digital Multiplexing — 3-State Outputs**
- **Low Cost Monolithic Construction**

Connection Diagram
18-Lead DIP
(Top View)



CD01171F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA571SDMQB	VC	D-6 (18-Lead DIP)

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Absolute Maximum Ratings

Storage Temperature Range	-65°C to +175°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[12]	
DIP	400 mW
Supply Voltage Range	V+ = 4.5 V to 5.5 V
	V− = −12 V to −16.5 V
V+ to Digital Common	0 V to 7 V
V− to Digital Common	0 V to −16.5 V
Analog Common to Digital Common	±1 V
Analog Input to Analog Common	±15 V
Contol Inputs	0 V to V+
Digital Outputs (Blank Mode)	0 V to V+

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. EA is defined as the deviation of the code transition points from the ideal transfer point on a straight line from zero to the full scale of the device.
8. VFS is guaranteed trimmable to zero with an external 50 Ω potentiometer in place of the 15 Ω fixed resistor. Full scale is defined as 10 V minus 1 LSB, or 9.990 V.
9. TC_{VZSU} is guaranteed by the V_{ZSU} tests.
10. TC_{VZSB} is guaranteed by the V_{ZSB} tests.
11. The data output lines have active pull-ups to source 0.5 mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6.0 kΩ internal pull-up resistor.
12. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

μA571SQB
Electrical Characteristics V+ = 5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
RESO	Resolution			10	Bits	4	1
E_A	Relative Accuracy[7]			±1.0	LSB	1	1,2,3
V_{FS}	Full Scale Calibration[8]	With 15 Ω Resistor in Series with Analog Input		±3.0	LSB	1	1
V_{ZS}	Unipolar Offset			±1.0	LSB	1	1,2,3
	Bipolar Offset			±1.0	LSB	1	1,2,3
DNL	Differential Nonlinearity			10	Bits	4	1
TC_{VZS}	Temperature Coefficient of Unipolar Offset[9]	$25°C \leq T_A \leq 125°C$		±2.0	LSB	1	2
				20	ppm/°C	1	2
		$-55°C \leq T_A \leq 25°C$		±2.0	LSB	1	3
				20	ppm/°C	1	3
	Temperature Coefficient of Bipolar Offset[10]	$25°C \leq T_A \leq 125°C$		±2.0	LSB	1	2
				20	ppm/°C	1	2
		$-55°C \leq T_A \leq 25°C$		±2.0	LSB	1	3
				20	ppm/°C	1	3
TC_{VFS}	Temperature Coefficient of Full Scale Calibration	R = 15 Ω, $25°C \leq T_A \leq 125°C$		±5.0	LSB	1	2
				50	ppm/°C	1	2
		R = 15 Ω, $-55°C \leq T_A \leq 25°C$		±5.0	LSB	1	3
				50	ppm/°C	1	3
PSRR	Power Supply Rejection Ratio	$4.5\ V \leq V+ \leq 5.5\ V$		±2.0	LSB	1	1
		$-16.5\ V \leq V- \leq -13.5\ V$		±2.0	LSB	1	1
Z_I	Analog Input Resistance		3.0	7.0	kΩ	1	1
V_{IR}	Analog Input Ranges — Unipolar		0	10	V	1	1
	Bipolar			±5.0	V	1	1
OC	Output Coding — Unipolar		Positive True Binary			1	1
	Bipolar		Positive True Offset Binary			1	1
I_{OL}	Output Sink Current	$V_O = 0.4\ V$	3.2		mA	1	2,3
I_{OH}	Output Source Current (Bit Outputs)[11]	$V_O = 2.4\ V$		−0.5	mA	1	2,3
$\overline{BC}$ IIH	Output Leakage When Blanked			±40	μA	1	1
$\overline{BC}$ IIL	Blank and Convert Input			±40	μA	1	1
V_{IH}	Blank-Logic "1"		2.0		V	1	1
V_{IL}	Convert-Logic "0"			0.8	V	1	1

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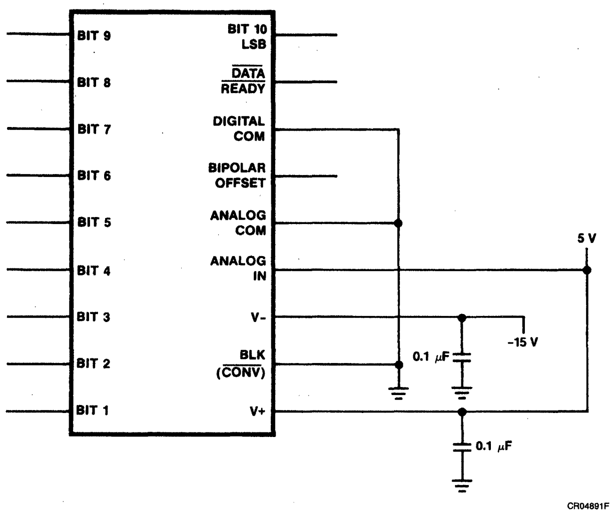
μA571SQB (Cont.)
Electrical Characteristics V+ = 5.0 V, V− = −15 V, all voltages measured with respect to digital common, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
I_{BLK}	Operating Current-Blank Mode	V+ = 5.0 V		10	mA	1	1
		V+ = 15 V		10	mA	1	1
		V− = −15 V		15	mA	1	1
I_{CONV}	Operating Current-Convert Mode	V+ = 5.0 V		10	mA	4	1
		V+ = 15 V		20	mA	4	1
		V− = −15 V		20	mA	4	1
t_{CONV}	Conversion Time		15	40	μs	1	9

Primary Burn-In Circuit



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MIL-STD-883
July 1986—Rev 1[5]

μA3045QB General Purpose Transistor Array

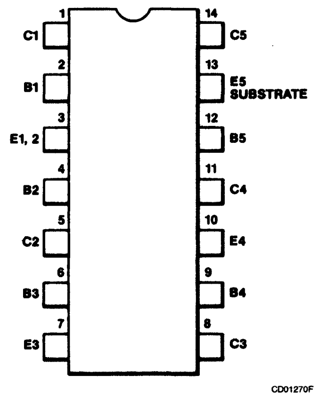
Aerospace and Defense Data Sheet
Linear Products

Description

The μA3045QB is a general purpose transistor array that contains a differentially connected pair and three individually isolated transistors. The part is designed for general purpose, low power applications for consumer and industrial applications.[6]

- **Low Input Offset Voltage**
- **Wideband Operation**
- **Low Noise**
- **Matched Differential Amplifier**

Connection Diagram
14-Lead DIP
(Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA3045DMQB	CA	D-1 (14-Lead DIP)

JAN Product Available

10802	BCA	D-1 (14-Lead DIP)
10802	BCB	D-1 (14-Lead DIP)

18

Absolute Maximum Ratings

Storage Temperature Range	−65°C to 175°C
Operating Temperature Range	−55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[8]	
DIP	400 mW
Collector-to-Emitter Voltage, V_{CEO}[9,10]	15 V
Collector-to-Base Voltage, V_{CBO}[9,10]	20 V
Collector-to-Substrate Voltage, V_{CIO}[9,11]	20 V
Emitter-to-Base Voltage, V_{EBO}[9,10]	5 V
Collector Current, I_C[9, 10]	50 mA

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Low Frequency, Small-Signal Equivalent Circuit Characteristic.
8. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.
9. The collector of each transistor except Q5 is isolated from the substrate by an integral diode. The substrate must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
10. Rating applies to each transistor within the array.
11. Rating applies to each transistor within the array except Q5; refer to V_{CEO} rating.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

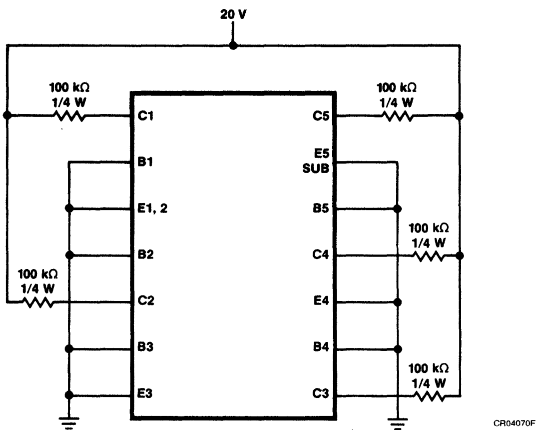
μA3045QB
Electrical Characteristics

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0\ \mu A$		20		V	1	1
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	$I_C = 1.0$ mA, $I_B = 0\ \mu A$		15		V	1	1
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$I_C = 10\ \mu A$, $I_C = 0\ \mu A$		20		V	1	1
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage	$I_E = 10\ \mu A$, $I_C = 0\ \mu A$		5.0		V	1	1
I_{CBO}	Collector Cutoff Current	$V_{CB} = 10$ V, $I_E = 0\ \mu A$			40	nA	1	1
		$V_{CB} = 35$ V, $I_E = 0\ \mu A$			0.2	μA	4	2
					10	nA	4	3
I_{CEO}	Collector Cutoff Current	$V_{CE} = 3.0$ V, $I_B = 0\ \mu A$			0.5	μA	1	1
		$V_{CE} = 10$ V, $I_B = 0\ \mu A$			1.0	μA	4	2
					0.2	μA	4	3
V_{BE}	Base Emitter Voltage (Unsaturated)	$V_{CE} = 3.0$ V, $I_E = -1.0$ mA		0.6	0.8	V	4	1
				0.45	0.65	V	4	2
				0.75	0.95	V	4	3
V_{BE}	Base Emitter Voltage (Unsaturated)	$V_{CE} = 3.0$ V $I_E = -10$ mA			0.9	V	4	1
					0.75	V	4	2
					1.0	V	4	3
h_{FE}	Static Forward Current-Transfer Ratio (Static Beta)	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA		40			1	1
$\|I_{IO1} - I_{IO2}\|$	Input Offset Current for Matched Pair Q1 and Q2 $\|I_{IO1} - I_{IO2}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			2.0	μA	1	1
$V_{BE(SAT)}$	Base-to-Emitter Voltage	$V_{CE} = 3.0$ V	$I_E = 1.0$ mA		1.0	V	4	1,2
			$I_E = 10$ mA		1.1	V	4	3
$\|V_{BEQ1} - V_{BEQ2}\|$	Input Offset Voltage for Differential Pair $\|V_{BE1} - V_{BE2}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			5.0	mV	1	1
					7.0	mV	4	2,3
$\|V_{BEQA} - V_{BEQB}\|$	Input Offset Voltage for Isolated Transistors $\|V_{BE3} - V_{BE4}\|$, $\|V_{BE4} - V_{BE5}\|$, $\|V_{BE5} - V_{BE3}\|$	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA			5.0	mV	1	1
					8.0	mV	4	2,3
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base-to-Emitter Voltage	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA		-2.2	-1.0	mV/°C	4	2,3
$V_{CE(SAT)}$	Collector-to-Emitter Saturation Voltage	$I_B = 1.0$ mA, $I_C = 10$ mA			0.4	V	4	1,3
					0.6	V	4	2

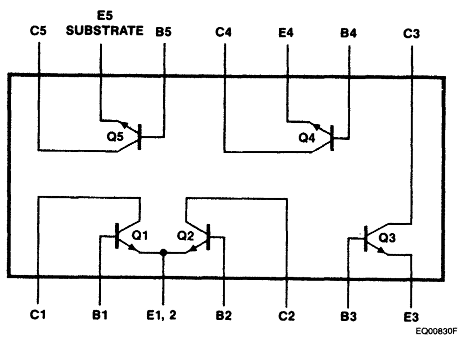
μA3045QB (Cont.)
Electrical Characteristics

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
$\|\Delta V_{IO}\|/\Delta T$	Input Offset Voltage Temperature Sensitivity	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA		15	μV/°C	4	2,3
I_{CIO}	Collector-to-Substrate Cutoff Current	$V_{CI} = 40$ V		10	nA	4	1,3
				200	nA	4	2
I_{EBO}	Emitter-to-Base Cutoff Current	$V_{EB} = 4.0$ V, $I_C = 0$ μA		10	nA	4	1,3
				200	nA	4	2
h_{FEQA}/h_{FEQB}	Magnitude of Static Beta Ratio for Any Two Isolated Transistors	$V_{CE} = 3.0$ V	0.9	1.1		4	1
		$I_C = 1.0$ mA	0.85	1.15		4	2,3
h_{fe}	Forward Current — Transfer Ratio[7]	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA	60			4	4,5
			35			4	6
f_T	Gain-Bandwidth Product	$V_{CE} = 3.0$ V, $I_C = 1.0$ mA	300		MHz	4	4
t_D	Delay Time			100	ns	3	9
				160	ns	3	10,11
t_r	Rise Time			50	ns	3	9
				80	ns	3	10,11
t_s	Storage Time			200	ns	3	9
				300	ns	3	10,11
t_f	Fall Time			80	ns	3	9
				125	ns	3	10,11
CS	Channel Separation		80		dB	3	9

Primary Burn-In Circuit
(38510/10802 may be used by FSC as an alternate)



Equivalent Circuit



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A Schlumberger Company

MIL-STD-883
July 1986—Rev 1[5]

μA555QB
Single Timing Circuit

Aerospace and Defense Data Sheet
Linear Products

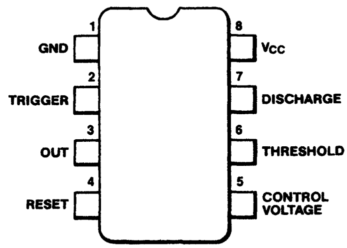
Description

The μA555QB Timing Circuit is a very stable controller for producing accurate time delays or oscillations. In the time delay mode, the delay time is precisely controlled by one external resistor and one capacitor; in the oscillator mode, the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor. By applying a trigger signal, the timing cycle is started and an internal flip-flop is set, immunizing the circuit from any further trigger signals. To interrupt the timing cycle a reset signal is applied ending the time-out.

The output is compatible with TTL circuits and can drive relays or indicator lamps.[6]

- **Timing Control, μs To Hours**
- **Astable Or Monostable Operating Modes**
- **Adjustable Duty Cycle**
- **High Sink Or Source Output Current**
- **TTL Output Drive Capability**
- **Low Temperature Stability**
- **Normally ON Or Normally OFF Output**

Connection Diagram 8-Lead DIP (Top View)



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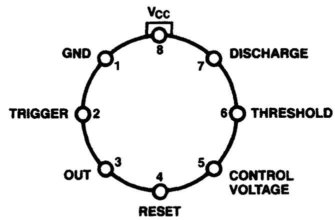
Connection Diagram 8-Lead Can (Top View)



CD01510F

Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA555HMQB	GC	A-1 (8-Lead Can)
μA555RMQB	PA	D-4 (8-Lead DIP)

JAN Product Available

10901	BGC	A-1 (8-Lead Can)
10901	BPA	D-4 (8-Lead DIP)
10901	BPB	D-4 (8-Lead DIP)

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Absolute Maximum Ratings

Storage Temperature Range	−65°C to 175°C
Operating Temperature Range	−55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[7]	
Can	330 mW
DIP	400 mW
Supply Voltage	± 18 V
Discharge Current	200 mA
Output Sink Current	200 mA
Output Source Current	−200 mA

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

Group A Electrical Tests Subgroups:

1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at −55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at −55°C
9. AC tests at 25°C
10. AC tests at 125°C
11. AC tests at −55°C

Group C and D Endpoints: Group A, Subgroup 1

Notes

1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 150°C/W for the Can and 120°C/W for the DIP.

μA555QB

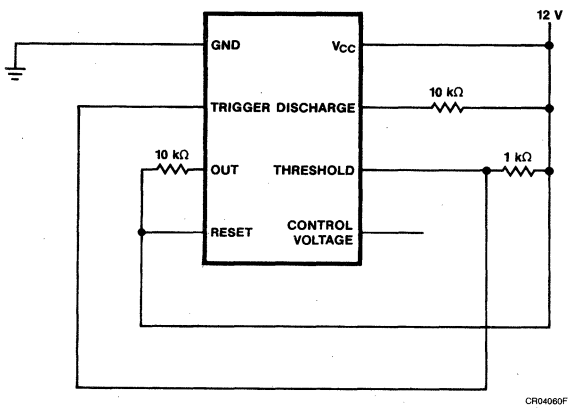
Electrical Characteristics 4.5 V $\leq V_{CC} \leq$ 16.5 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
I_{CC}	Supply Current	V_{CC} = 15 V, $R_L = \infty$			12	mA	1	1,2,3
		V_{CC} = 5.0 V, $R_L = \infty$			5.0	mA	1	1,2,3
V_{TH}	Threshold Voltage	V_{CC} = 15 V		9.7	10.3	V	1	1,2,3
		V_{CC} = 5.0 V		3.0	3.6	V	1	1,2,3
V_{TR}	Trigger Voltage	V_{CC} = 15 V		4.8	5.2	V	1	1,2,3
		V_{CC} = 5.0 V		1.45	1.9	V	1	1,2,3
I_{TR}	Trigger Current	V_{CC} = 15 V		−5.0		μA	1	1,2,3
V_R	Reset Voltage	5.0 V $\leq V_{CC} \leq$ 15 V		0.1	1.0	V	1	1,2,3
I_R	Reset Current	V_{CC} = 15 V		−1.6	0	mA	1	1,2,3
I_{TH}	Threshold Current	V_{CC} = 15 V			0.25	μA	1	1,2
					2.5	μA	1	3
V_{CV}	Control Voltage Level	V_{CC} = 15 V		9.6	10.4	V	1	1
		V_{CC} = 5.0 V		2.9	3.8	V	1	1
V_{OL}	Output Voltage LOW	V_{CC} = 15 V	I_{OL} = 10 mA		0.15	V	1	1,3
					0.25	V	1	2
			I_{OL} = 50 mA		0.5	V	1	1,3
					0.7	V	1	2
			I_{OL} = 100 mA		2.2	V	1	1
					2.8	V	1	2,3
			I_{OL} = 200 mA		3.5	V	1	1
		V_{CC} = 5.0 V	I_{OL} = 8.0 mA		0.25	V	1	1
					0.35	V	1	2,3
V_{OH}	Output Voltage HIGH	V_{CC} = 15 V	I_{OH} = −200 mA	11		V	1	1
			I_{OH} = −100 mA	13		V	1	1,2,3
		V_{CC} = 5.0 V	I_{OH} = −100 mA	3.0		V	1	1,2
				2.0		V	1	3
I_{CEX}	Discharge Leakage Current	V_{CC} = 15 V, V_D = 15 V			95	nA	1	1,3
					5.0	μA	1	2
V_{SAT}	Discharge Saturation Voltage	V_{CC} = 5.0 V, I_{OL} = 5.0 mA			0.25	V	1	1,3
					0.4	V	1	2
t_{PLH}	Propagation Delay to High Level (Monostable)	R_T = 1.0 kΩ, C_T = 0.1 μF			900	ns	3	10
					800	ns	3	9, 11
t_{TLH}	Transition Time to High Level (Monostable)	R_T = 1.0 kΩ, C_T = 0.1 μF			300	ns	3	9, 10, 11
t_{THL}	Transition Time to Low Level (Monostable)				300	ns	3	9, 10, 11
t_D(OH)	Time Delay High (Monostable)	R_T = 1.0 kΩ, C_T = 0.1 μF		106.7	113.3	μs	3	9, 10, 11
		R_T = 100 kΩ, C_T = 0.1 μF		10.67	11.33	ms	3	9, 10, 11
Δt_D(OH)/ ΔV_{CC}	Drift in Time Delay vs. Change in Supply Voltage (Monostable)	ΔV_{CC} = 12 V, R_T = 1.0 kΩ, C_T = 0.1 μF		−220	220	ns/V	4	9

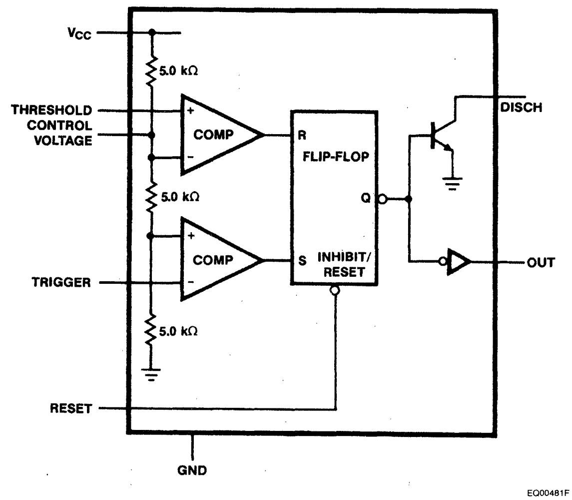
μA555QB (Cont.)
Electrical Characteristics 4.5 V $\leqslant V_{CC} \leqslant$ 16.5 V, unless otherwise specified.

Symbol	Characteristic	Condition		Min	Max	Unit	Note	Subgrp
t_{PHL}	Propagation Delay Time (Threshold to Output) (Monostable)	$R_T = 1.0$ kΩ, $C_T = 0.1$ μF			12	μs	3	9, 10, 11
$\Delta t_{PH}(OH)/\Delta T$	Temperature Coefficient of Time Delay (Monostable)	$V_{CC} = 16.5$ V	25°C $\leqslant T_A \leqslant$ 125°C	−11	11	ns/°C	3	10
			−55°C $\leqslant T_A \leqslant$ 25°C	−11	11	ns/°C	3	11
t_{CH}	Capacitor Charge Time (Astable)	$C_T = 0.1$ μF	$R_{TA} = R_{TB} = 1.0$ kΩ	120	156	μs	3	9, 10, 11
			$R_{TA} = R_{TB} = 100$ kΩ	11.3	15	ms	3	9, 10, 11
t_{DIS}	Capacitor Discharge Time (Astable)	$C_T = 0.1$ μF	$R_{TA} = R_{TB} = 1.0$ kΩ	57.5	80	μs	3	9, 10, 11
			$R_{TA} = R_{TB} = 100$ kΩ	5.4	7.7	ms	3	9, 10, 11
$\Delta t_{CH}/\Delta V_{CC}$	Drift in Capacitor Charge Time vs Change in Supply Voltage (Astable)	$\Delta V_{CC} = 12$ V, $R_{TA} = R_{TB} = 1.0$ kΩ, $C_T = 0.1$ μF		−820	820	ns/V	4	9
$t_{CH}/\Delta T$	Temperature Coefficient of Capacitor Charge Time	$V_{CC} = 16.5$ V $R_{TA} = R_{TB}$ = 1.0 kΩ, $C_T = 0.1$ μF	25°C $\leqslant T_A \leqslant$ 125°C	−68	68	ns/°C	3	10
			−55°C $\leqslant T_A \leqslant$ 25°C	−68	68	ns/°C	3	11
t_{res}	Reset Time	$V_{CC} = 16.5$ V, $R_{TA} = R_{TB} = 1.0$ kΩ $C_T = 0.1$ μF			2.0	μs	3	10
					1.5	μs	3	9, 11

Primary Burn-In Circuit
(38510/10901 may be used by FSC as an alternate)



Block Diagram



FAIRCHILD
A Schlumberger Company

MIL-STD-883
July 1986—Rev 2[5]

μA733QB Differential Video Amplifier

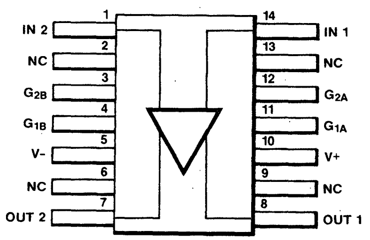
Aerospace and Defense Data Sheet
Linear Products

Description

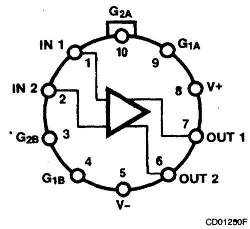
The μA733QB is a monolithic two-stage differential input, differential output video amplifier constructed using the Fairchild Planar Epitaxial process. Internal series shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.[6]

- **Wide Bandwidth**
- **High Input Resistance**
- **Selectable Gains Of 10, 100, And 400**
- **No Frequency Compensation Required**

Connection Diagram 14-Lead Flatpak (Top View)

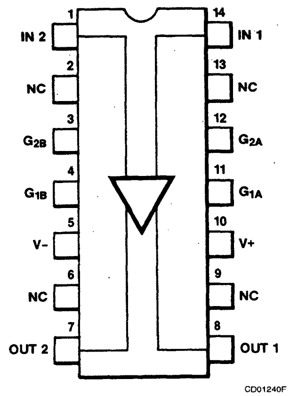


Connection Diagram 10-Lead Can (Top View)



Lead 5 connected to case.

Connection Diagram 14-Lead DIP (Top View)



Order Information

Part No.	Case/ Finish	Package Code Mil-M-38510, Appendix C
μA733DMQB	CA	D-1 14-Lead DIP
μA733HMQB	IC	A-2 10-Lead Can
μA733FMQB	AA	F-1 14-Lead Flatpak

18

Absolute Maximum Ratings

Storage Temperature Range	-65°C to 175°C
Operating Temperature Range	-55°C to 125°C
Lead Temperature (soldering, 60 s)	300°C
Internal Power Dissipation[9]	
Can and Flatpak	330 mW
DIP	400 W
Supply Voltage	±8 V
Differential Input Voltage	±5 V
Input Voltage	±6 V
Output Current	10 mA

Notes
1. 100% Test and Group A
2. Group A
3. Periodic tests, Group C
4. Guaranteed but not tested
5. When changes occur, FSC will make data sheet revisions available. Contact local sales representative for the latest revision.
6. For more information on device function, refer to the Fairchild Linear Data Book Commercial Section.
7. VIR is guaranteed by the CMR test.
8. Gain Select leads G1A and G1B are connected together for Gain 1, Gain Select leads G2A and G2B are connected together for Gain 2, and all Gain Select leads are left open for Gain 3.
9. Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 140°C/W for the Can, 150°C/W for the Flatpak, 120°C/W for the DIP.

Processing: MIL-STD-883, Method 5004

Burn-In: Method 1015, Condition A, PDA calculated using Method 5005, Subgroup 1

Quality Conformance Inspection: MIL-STD-883, Method 5005

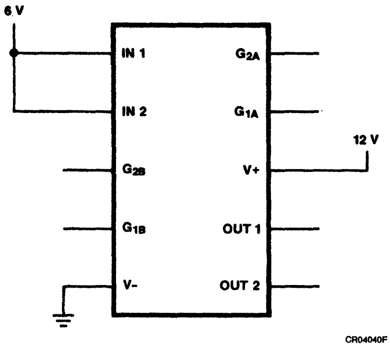
Group A Electrical Tests Subgroups:
1. Static tests at 25°C
2. Static tests at 125°C
3. Static tests at -55°C
4. Dynamic tests at 25°C
5. Dynamic tests at 125°C
6. Dynamic tests at -55°C
9. AC tests at 25°C

Group C and D Endpoints: Group A, Subgroup 1

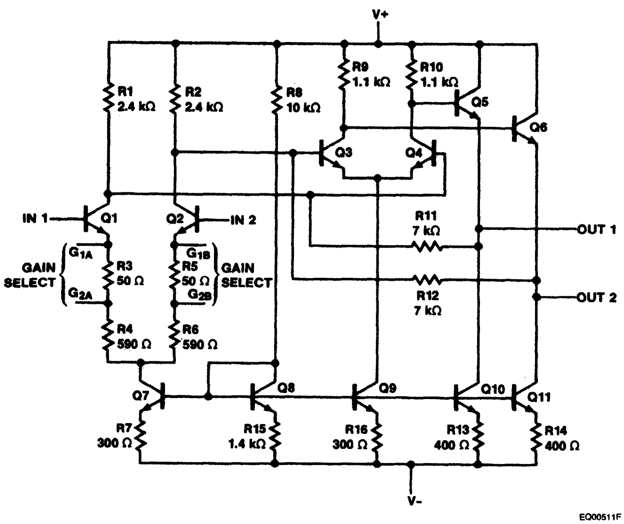
Electrical Characteristics $V_{CC} = \pm 6.0$ V, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit	Note	Subgrp
I_{IO}	Input Offset Current			3.0	μA	1	1
				5.0	μA	1	2,3
I_{IB}	Input Bias Current			20	μA	1	1
				40	μA	1	2,3
Z_I	Input Impedance	Gain 2	20		kΩ	1	1
			8.0		kΩ	1	2,3
I_{CC}	Supply Current			24	mA	1	1
				27	mA	1	2,3
CMR	Common Mode Rejection	$V_{CM} = \pm 1.0$ V, Gain 2	60		dB	1	1
			50		dB	1	2,3
V_{IR}	Input Voltage Range[7]		±1.0		V	1	1,2,3
PSRR	Power Supply Rejection Ratio	5.5 V $\leqslant$ V+ $\leqslant$ 6.5 V, V− = −6.0 V, Gain 2	50		dB	1	1,2,3
V_{OS}	Output Offset Voltage	Gain 1		1.5	V	1	1,2,3
		Gain 2, 3		1.0	V	1	1
				1.2	V	1	2,3
V_{CMO}	Output Common Mode Voltage		2.4	3.4	V	1	1
I_{O-}	Output Sink Current		2.5		mA	1	1
			2.2		mA	1	2,3
A	Differential Voltage Gain[8]	Gain 1	300	500	V/V	1	4
			200	600	V/V	1	5,6
		Gain 2	90	110	V/V	1	4
			80	120	V/V	1	5,6
		Gain 3	9.0	11	V/V	1	4
			8.0	12	V/V	1	5,6
V_{OP}	Output Voltage Swing		3.0		V_{p-p}	1	4
			2.5		V_{p-p}	1	5,6
t_R	Risetime	$R_S = 50$ Ω, $V_O = 1$ V_{p-p}, Gain 2		10	ns	2	9
t_{PD}	Propagation Delay	$R_S = 50$ Ω, $V_O = 1$ V_{p-p}, Gain 2		10	ns	2	9

Primary Burn-In Circuit

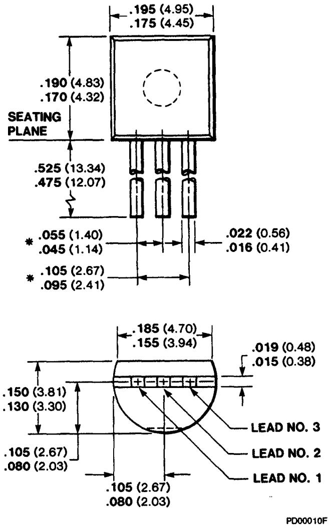


Equivalent Circuit



Package Outlines

3 Lead Molded Package In Accordance with JEDEC TO-92



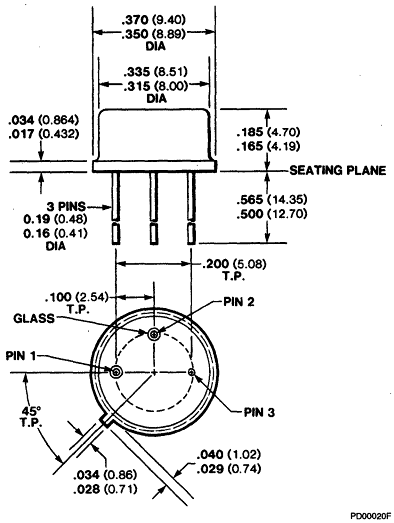
EI

Notes

Leads are solder dipped copper alloy.
Lead No. 2 connected to die pad.
Package material is plastic.
Package weight is 0.19 gram.

Dimensions $\frac{.055}{.045}\left(\frac{1.40}{1.14}\right)$ and $\frac{.105}{.095}\left(\frac{2.67}{2.41}\right)$ are measured at the body of package.

3 Lead Metal Package In Accordance with JEDEC TO-39



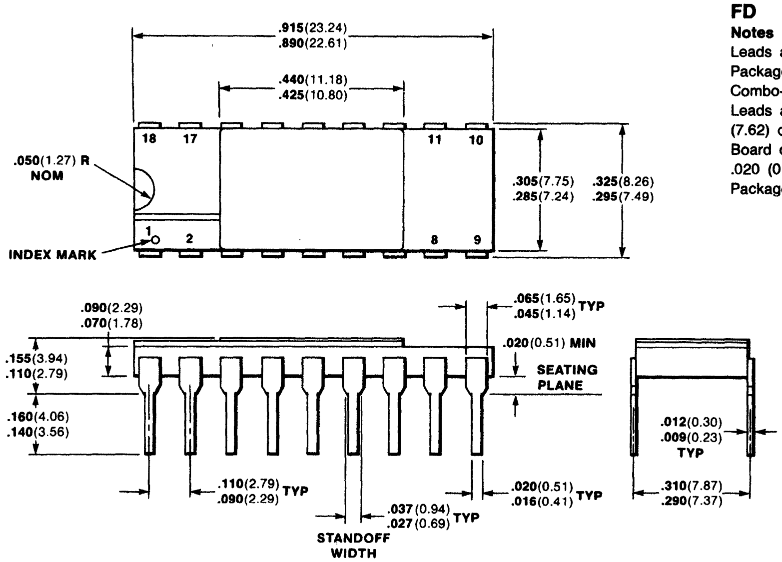
FC

Notes

Leads are gold plated kovar.
Leads 1 and 2 are electrically isolated with glass.
Lead No. 3 connected to case.
Eyelet is gold plated kovar.
Can is Grade A nickel.
Package weight is 1.23 grams.

All dimensions in inches (bold) and millimeters (parentheses)

18 Lead Ceramic DIP Side Brazed Package

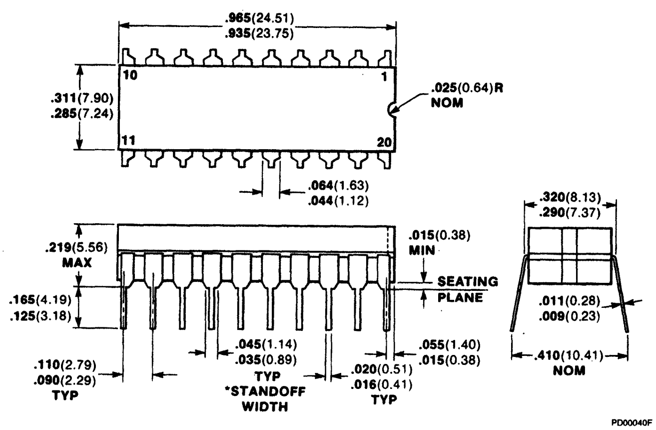


FD

Notes

Leads are nickel and gold plated alloy 42 or kovar.
Package material is alumina.
Combo-lid is gold plated kovar or alloy 42.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
Board drilling dimensions should equal your practice for .020 (0.51) diameter leads.
Package weight is 1.5 grams.

20 Lead Ceramic DIP



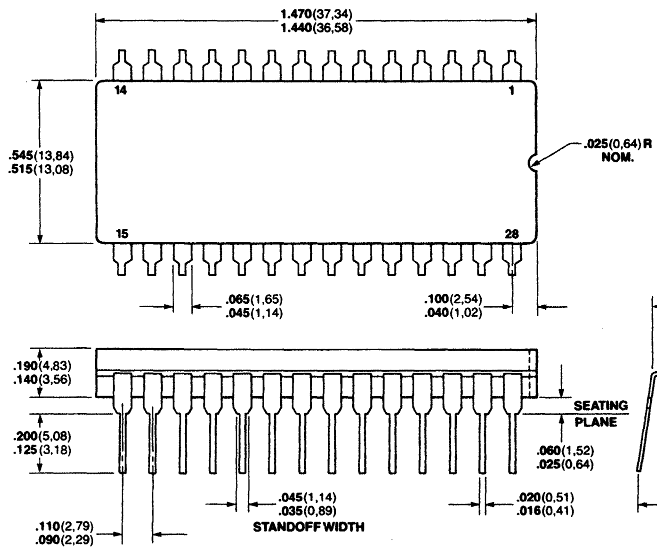
FL

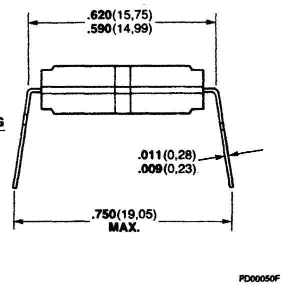
Notes

Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
*The .035-.045 (0.89-1.14) dimension does not apply to the corner leads.
Package weight is 2.8 grams.

All dimensions in inches (bold) and millimeters (parentheses)

28 Lead Ceramic DIP



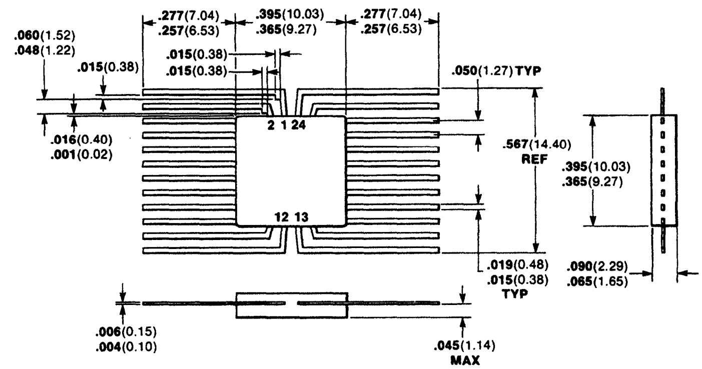


FM

Notes

Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on .600 (15, 24) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for .020 (0, 51) diameter lead.
Hermetically sealed alumina package.
Package weight is 8.32 grams.

24 Lead Cerpak



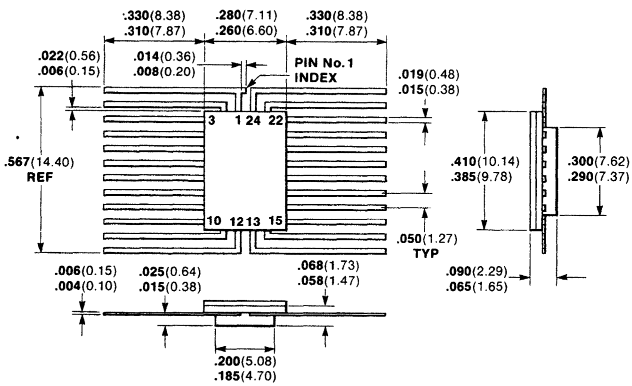
FN

Notes

Leads are tin-plated alloy 42.
Increase maximum limits by .003 (0,08) if leads are solder dipped.
Package weight is 0.68 grams.

All dimensions in inches (bold) and millimeters (parentheses)

24 Lead Flatpak



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FR

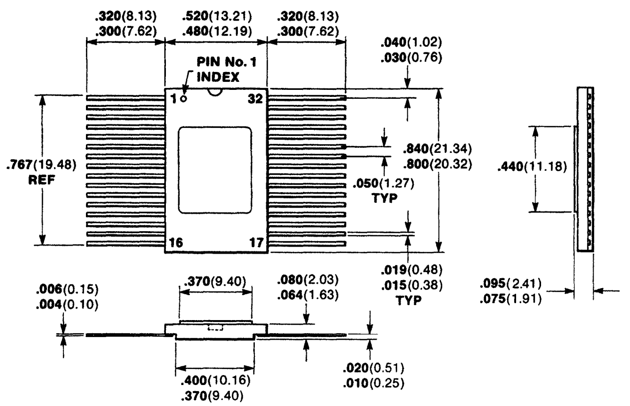
Notes

Leads are gold plated alloy 42.

If solder-dipped leads are used, the maximum limits for these dimensions may be increased by .003 (0,08).

Package weight is 0.53 grams.

32 Lead Flatpak



PD00080F

FS

Notes

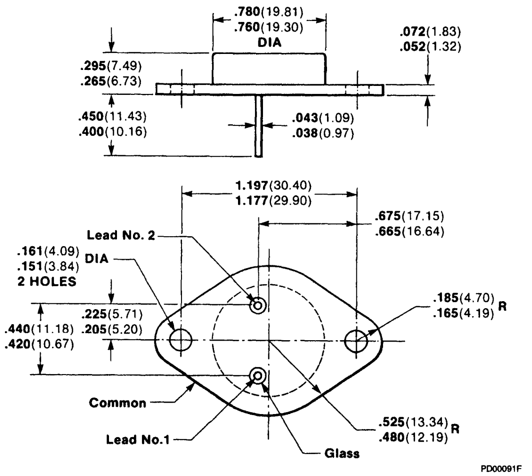
Leads are gold plated alloy 42.

If solder-dipped leads are used, the maximum limits for these dimensions may be increased by .003 (0,08).

Package weight is 1.97 grams.

All dimensions in inches (bold) and millimeters (parentheses)

2 Lead Metal TO-3 with Moly-Pad

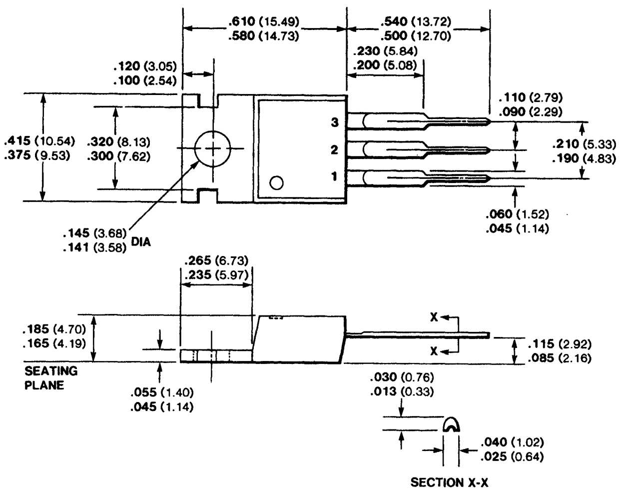


FT

Notes

Base is nickel plated steel.
Can is nickel plated steel.
Leads are solder dipped over nickel plated alloy 52.
Leads 1 and 2 electrically isolated from case with glass.
Case is third electrical connection.
Package weight is 12.3 grams.

3 Lead Molded Package In Accordance with JEDEC TO-220



GH

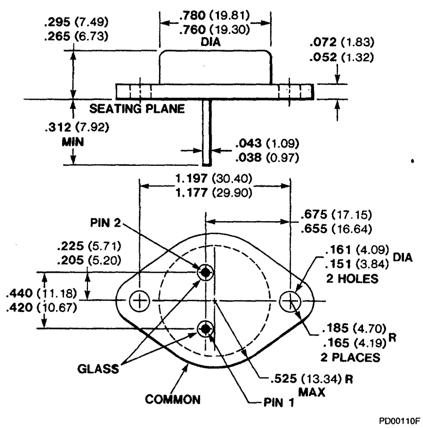
Notes

Leads are solder dipped over nickel plated copper alloy.
Lead No. 2 is electrical contact with the mounting tab.
Mounting tab is nickel plated copper alloy.
Package material is plastic.
Package weight is 2.0 grams.

19

All dimensions in inches (bold) and millimeters (parentheses)

2 Lead Metal Package In Accordance with JEDEC TO-3

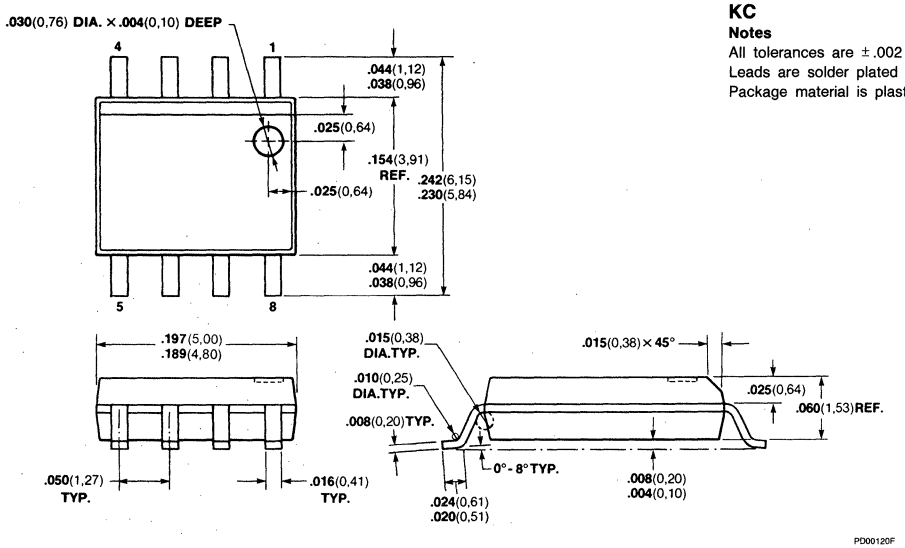


HJ

Notes

Base is nickel plated steel.
Can is nickel plated steel.
Leads are solder dipped over nickel plated alloy 52.
Leads 1 and 2 electrically isolated from case with glass.
Case is third electrical connection.
Package weight is 12.3 grams.

8 Lead Plastic SOIC



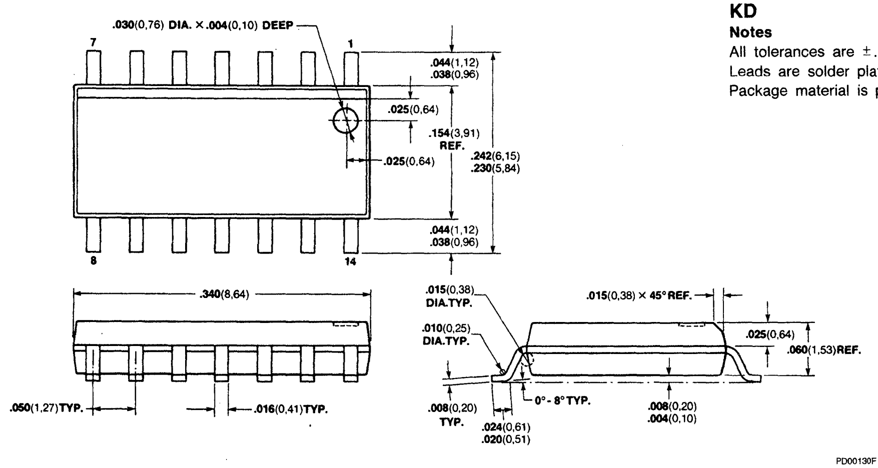
KC

Notes

All tolerances are ±.002 (0.05) unless noted.
Leads are solder plated (90Sn/10Pb).
Package material is plastic.

All dimensions in inches (bold) and millimeters (parentheses)

14 Lead Plastic SOIC

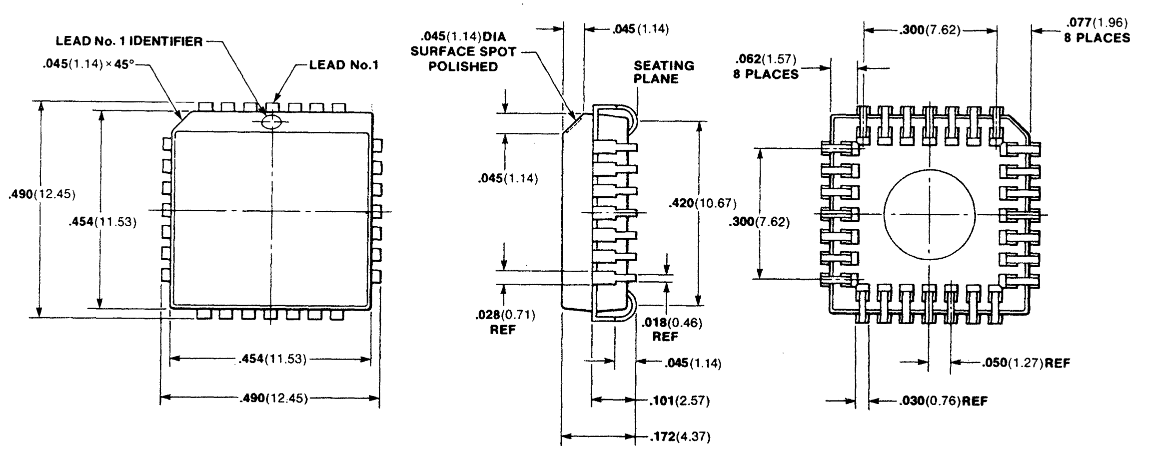


KD

Notes

All tolerances are ±.002 (0.05) unless noted.
Leads are solder plated (90Sn/10 Pb).
Package material is plastic.

28 Lead PLCC



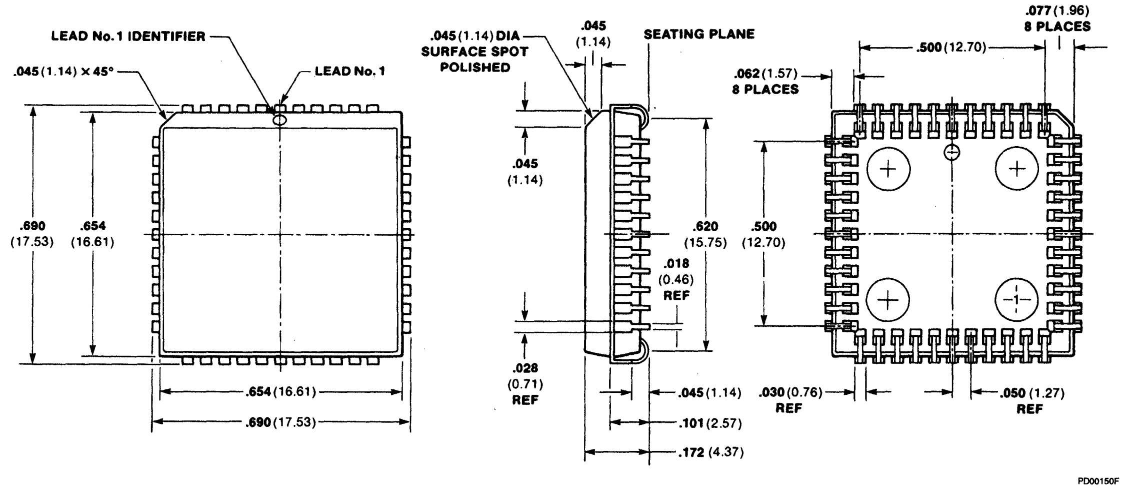
KH

Notes

All tolerances are ±.003 unless otherwise noted.
The leads are solder dipped or solder plated copper alloy.
Package material is plastic.

All dimensions in inches (bold) and millimeters (parentheses)

44 Lead PLCC

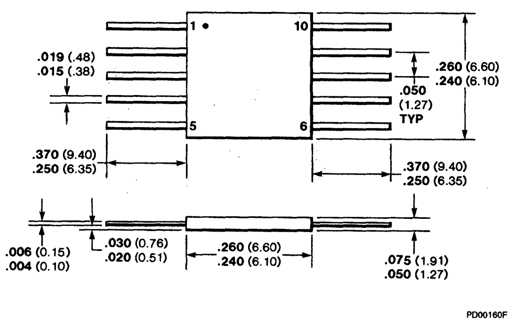


KI

Notes

All tolerances are ±.003 unless otherwise noted.
The leads are solder dipped or solder plated copper alloy.
Package material is plastic.

10 Lead Cerpak



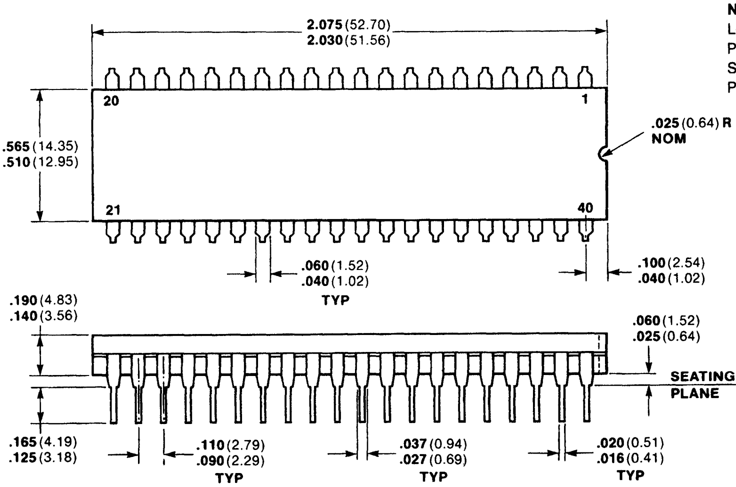
3F

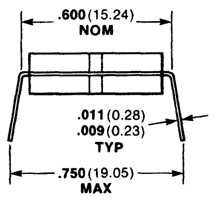
Notes

Leads are tin-plated/gold plated alloy 42.
If solder-dipped leads are used, the maximum limits for these dimensions may be increased by .003 (0.08).
Package weight is 0.26 grams.

All dimensions in inches (bold) and millimeters (parentheses)

40 Lead Ceramic DIP

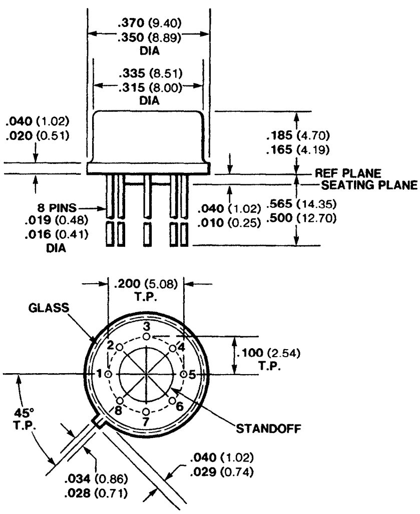




PD00280F

Notes
Lead material is Kovar.
Package material is alumina.
Sealing material is vitreous glass.
Package weight is 12 grams.

8 Lead Metal Package In Accordance with JEDEC TO-99



PD00270F

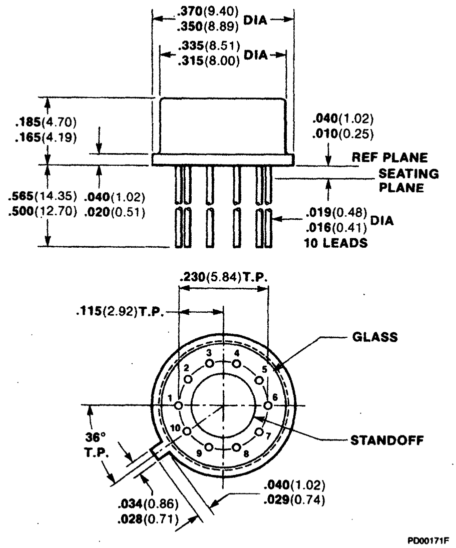
5W

Notes
Leads are tin-plated over nickel plated kovar.
Seven leads thru, lead No. 4 connected to case.
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface.
Can is Grade A nickel, tin plated outside surface.
Package weight is 1.22 grams.

19

All dimensions in inches (bold) and millimeters (parentheses)

10 Lead Metal Package
In Accordance with JEDEC TO-100



5X

Notes

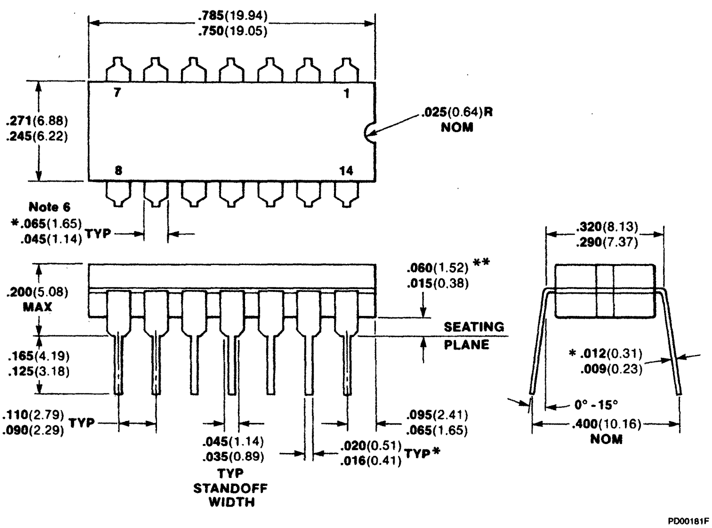
Leads are tin plated over nickel plated kovar.
Nine leads thru, lead 5 is connected to case.
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface.
Can is Grade A nickel, tin plated outside surface.
Package weight is 1.32 grams.

5Y

Notes

Leads are tin plated over nickel plated Kovar.
Ten leads thru.
Eyelet is nickel plated kovar, glass filled with ceramic standoff, tin plated outside metal surface.
Can is Grade A nickel, tin plated outside surface.
Package weight is 1.32 grams.

14 Lead Ceramic DIP



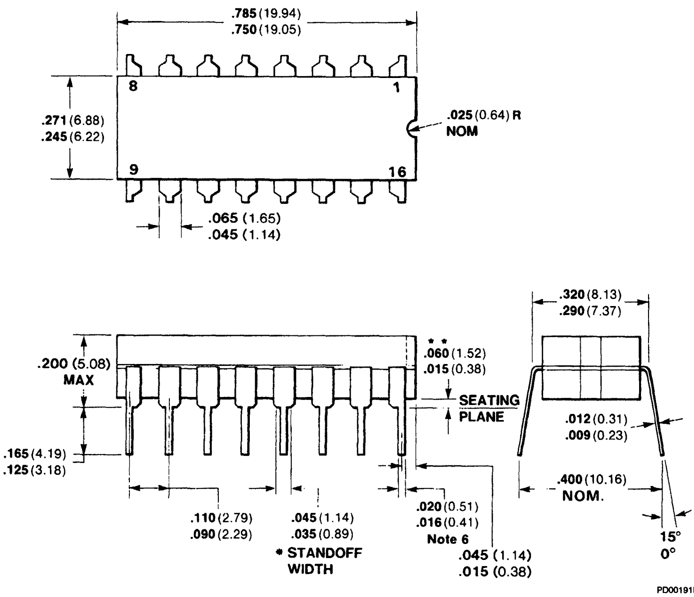
6A

Notes

Leads are tin-plated alloy 42 or equivalent.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
*Increase maximum limit by .003 (0.08) if leads are solder dipped.
Package weight is 2.0 grams.
**Maximum does not apply for Std Rel.

All dimensions in inches (bold) and millimeters (parentheses)

16 Lead Ceramic DIP

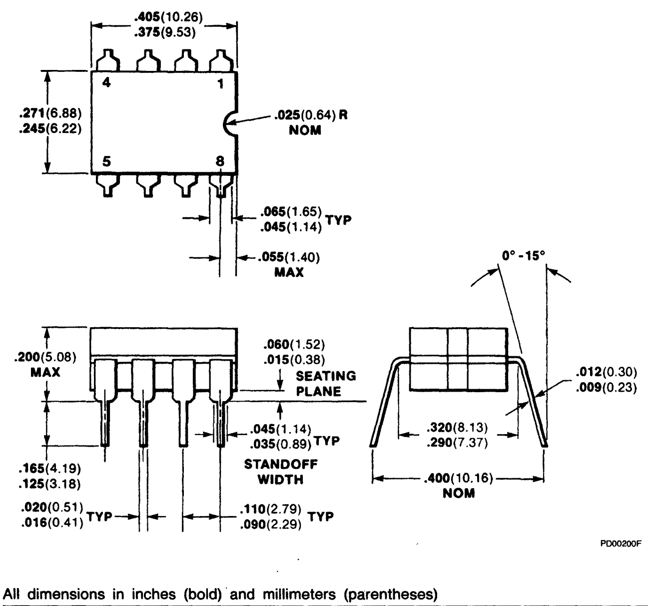


6B

Notes

Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
Increase maximum limit by .003 (0.08) if leads are solder dipped.
*The .035-.045 (0.89-1.14) dimension does not apply to the corner leads.
Package weight is 2.0 grams.
**Maximum does not apply for Std Rel.

8 Lead Ceramic DIP



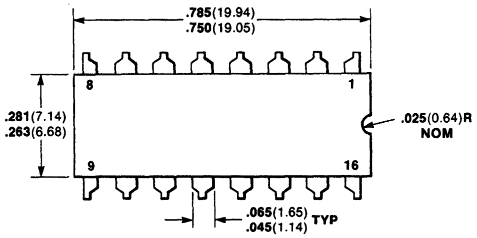
6T

Notes

Leads are tin plated alloy 42.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with a "positive" misalignment to facilitate insertion.
Hermetically sealed alumina package.
Package weight is 1.0 gram.

All dimensions in inches (bold) and millimeters (parentheses)

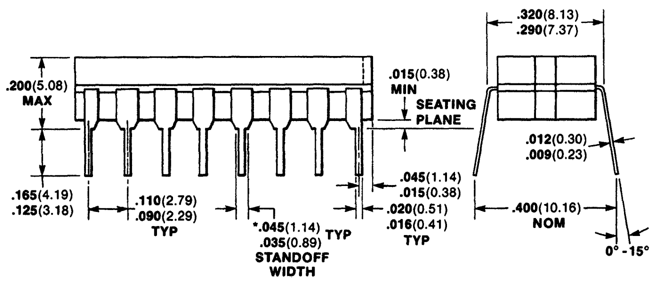
16 Lead Ceramic DIP



7B

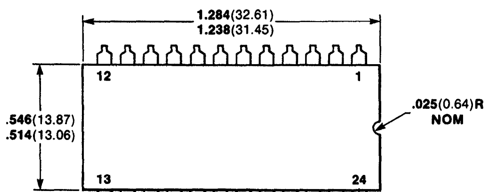
Notes

Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows in .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
*The .035-.045 (0.89-1.14) dimension does not apply to the corner leads.
Package weight is 2.2 grams.



PD00210F

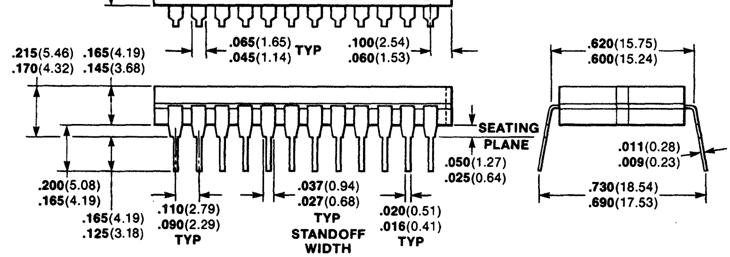
24 Lead Ceramic DIP



7L

Notes

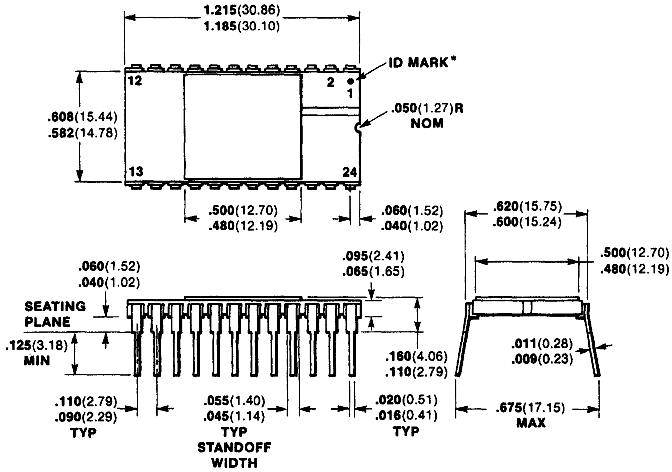
Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on .600 (15.24) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
Base cavity metallization is gold.
Package weight is 7.1 grams.



PD00220F

All dimensions in inches (bold) and millimeters (parentheses)

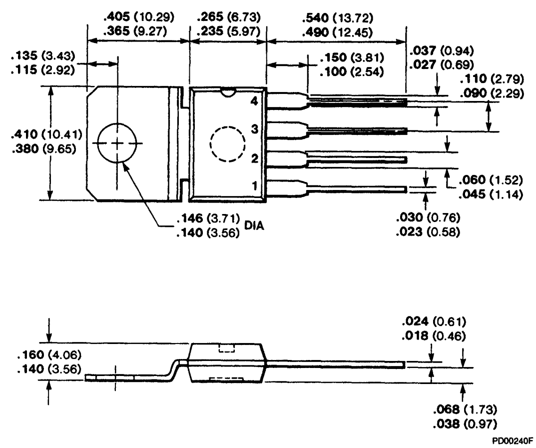
24 Lead Ceramic DIP
Side Brazed



7R
Notes

Leads are nickel-gold plated kovar or alloy 42 or equivalent.
Combo lid is gold plated kovar or alloy 42 or equivalent.
Base is alumina.
Board drilling dimensions should equal your practice. for .020 (0.51) diameter lead.
Leads are intended for insertion in hole rows on .600 (15.24) centers.
Package weight is 3.8 grams.
*ID #0 indicates all leads are electrically floating from base, and the ID placement indicates lead #1.

4 Lead Molded Single Wing

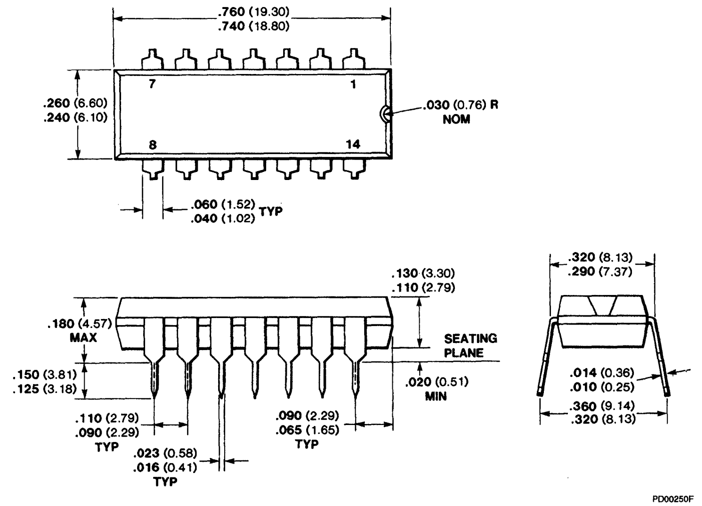


8Z
Notes

Leads are solder dipped over nickel plated copper alloy.
Mounting tab is electrically insulated from leads.
Mounting tab is nickel plated copper alloy.
Board-drilling dimensions should equal your practice for .033 (0.84) diameter leads.
This package is intended to be mounted with the tab flush with the top of the p.c. board or heat sink. A No. 4 screw may be used to secure the package. Thermal compound is recommended.
Package material is plastic.
Package weight is 1.2 grams.

All dimensions in inches (bold) and millimeters (parentheses)

14 Lead Molded Plastic DIP

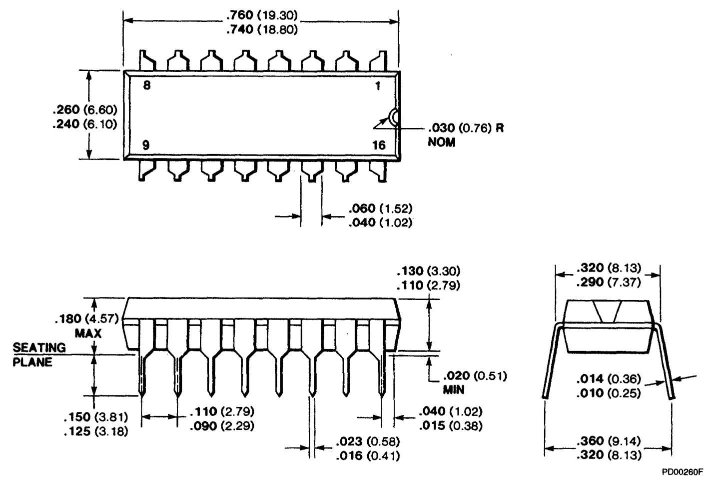


9A

Notes

Leads are solder dipped copper alloy.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Package material is plastic.
Package weight is 0.9 grams.

16 Lead Molded Plastic DIP



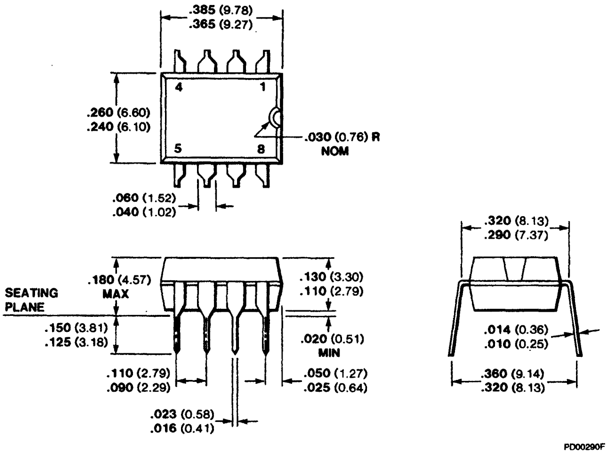
9B

Notes

Leads are solder dipped copper alloy.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Package material is plastic.
Package weight is 1.0 gram.

All dimensions in inches (bold) and millimeters (parentheses)

8 Lead Molded Plastic DIP



9T

Notes

Leads are solder dipped copper alloy.
Leads are intended for insertion in hole rows on .300 (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Package material is plastic.
Package weight is 0.6 gram.

All dimensions in inches (bold) and millimeters (parentheses)

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